

Automotive Single D Flip Flop

NLV18SZ74

The NLV18SZ74 is an automotive-grade high performance, full function Edge triggered D Flip Flop.

Features

- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 2.7 ns t_{PD} at $V_{CC} = 5$ V (typ)
- Inputs/Outputs Overvoltage Tolerant up to 5.5 V
- I_{OFF} Supports Partial Power Down Protection
- Source/Sink 24 mA at 3.0 V
- Available in US8 Package
- Chip Complexity < 100 FETs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

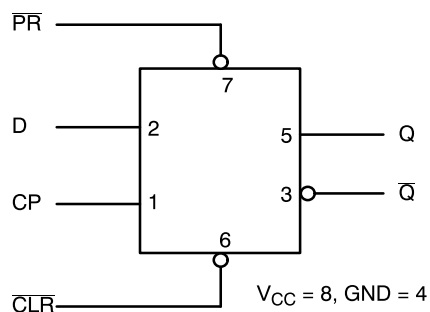


Figure 1. Logic Symbol

PIN ASSIGNMENT

Pin	US8
1	CP
2	D
3	$\bar{Q}$
4	GND
5	Q
6	$\bar{CLR}$
7	PR
8	V_{CC}



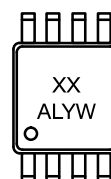
ON Semiconductor®

www.onsemi.com

MARKING DIAGRAMS



US8
US SUFFIX
CASE 493



XX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

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MAXIMUM RATINGS

Symbol	Characteristics	Value	Unit
V _{CC}	DC Supply Voltage	–0.5 to +6.5	V
V _{IN}	DC Input Voltage	–0.5 to +6.5	V
V _{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	–0.5 to V _{CC} + 0.5 –0.5 to +6.5 –0.5 to +6.5	V
I _{IK}	DC Input Diode Current V _{IN} < GND	–50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	–50	mA
I _{OUT}	DC Output Source/Sink Current	±50	mA
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	–65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	250	°C/W
P _D	Power Dissipation in Still Air	250	mW
MSL	Moisture Sensitivity	Level 1	–
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	–
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 1000	V
I _{Latchup}	Latchup Performance (Note 4)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 10mm-by-1inch, 2 ounce copper trace no air flow.
3. HBM tested to ANSI/ESDA/JEDEC JS–001–2017. CDM tested to EIA/JESD22–C101–F. JEDEC recommends that ESD qualification to EIA/JESD22–A115–A (Machine Model) be discontinued per JEDEC/JEP172A.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	DC Input Voltage	0	5.5	V
V _{OUT}	DC Output Voltage Active-Mode (High or Low State) Tri-State Mode (Note 1) Power-Down Mode (V _{CC} = 0 V)	0 0 0	V _{CC} 5.5 5.5	
T _A	Operating Temperature Range	–55	+125	°C
t _R , t _F	Input Rise and Fall Time V _{CC} = 1.65 V to 1.95 V V _{CC} = 2.3 V to 2.7 V V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V	0 0 0 0	20 20 10 5	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			–55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65 to 1.95	0.65 V _{CC}	–	–	0.65 V _{CC}	–	V
			2.3 to 5.5	0.70 V _{CC}	–	–	0.70 V _{CC}	–	
V _{IL}	Low-Level Input Voltage		1.65 to 1.95	–	–	0.35 V _{CC}	–	0.35 V _{CC}	V
			2.3 to 5.5	–	–	0.30 V _{CC}	–	0.30 V _{CC}	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-55°C ≤ T _A ≤ 125°C		Units
				Min	Typ	Max	Min	Max	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -100 μA I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V _{CC} - 0.1 1.29 1.9 2.2 2.4 2.7 2.3 3.8	V _{CC} 1.4 2.1 2.4 2.7 2.5 4.0	- - - - - - -	V _{CC} - 0.1 1.29 1.9 2.2 2.4 2.3 3.8	- - - - - - -	V
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	- - - - - - -	0.08 0.2 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55	- - - - - - -	0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I _{IN}	Input Leakage Current	V _{IN} = 5.5 V or GND	1.65 to 5.5	-	-	±0.1	-	±1.0	μA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5 V or V _{OUT} = 5.5 V	0	-	-	1.0	-	10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	-	-	1.0	-	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

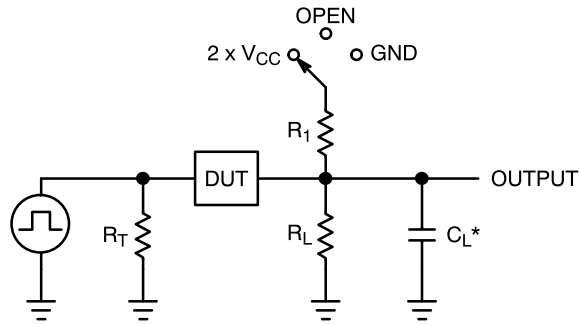
Symbol	Parameter	V_{CC} (V)	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -55$ to 125°C		Units
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	75	–	–	75	–	MHz
		2.5 ± 0.2		150	–	–	150	–	
		3.3 ± 0.3		200	–	–	200	–	
		5.0 ± 0.5		250	–	–	250	–	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	175	–	–	175	–	
		5.0 ± 0.5		200	–	–	200	–	
t_{PLH} , t_{PHL}	Propagation Delay, CP to Q or $\bar{Q}$ (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	–	6.5	12.5	–	13	ns
		2.5 ± 0.2		–	3.8	7.5	–	8.0	
		3.3 ± 0.3		–	2.8	6.5	–	7.0	
		5.0 ± 0.5		–	2.2	4.5	–	5.0	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	–	3.4	7.0	–	7.5	
		5.0 ± 0.5		–	2.6	5.0	–	5.5	
t_{PLH} , t_{PHL}	Propagation Delay, PR or CLR to Q or $\bar{Q}$ (Waveform 2)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	–	6.5	14	–	14.5	ns
		2.5 ± 0.2		–	3.8	9.0	–	9.5	
		3.3 ± 0.3		–	2.8	6.5	–	7.0	
		5.0 ± 0.5		–	2.2	5.0	–	5.5	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	–	3.4	7.0	–	7.5	
		5.0 ± 0.5		–	2.6	5.0	–	5.5	
t_S	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	6.5	–	–	6.5	–	ns
		2.5 ± 0.2		3.5	–	–	3.5	–	
		3.3 ± 0.3		2.0	–	–	2.0	–	
		5.0 ± 0.5		1.5	–	–	1.5	–	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	2.0	–	–	2.0	–	
		5.0 ± 0.5		1.5	–	–	1.5	–	
t_H	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	0.5	–	–	0.5	–	ns
		2.5 ± 0.2		0.5	–	–	0.5	–	
		3.3 ± 0.3		0.5	–	–	0.5	–	
		5.0 ± 0.5		0.5	–	–	0.5	–	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	0.5	–	–	0.5	–	
		5.0 ± 0.5		0.5	–	–	0.5	–	
t_W	Pulse Width, CP, CLR, PR (Waveform 3)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	6.0	–	–	6.0	–	ns
		2.5 ± 0.2		4.0	–	–	4.0	–	
		3.3 ± 0.3		3.0	–	–	3.0	–	
		5.0 ± 0.5		2.0	–	–	2.0	–	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	3.0	–	–	3.0	–	
		5.0 ± 0.5		2.0	–	–	2.0	–	
t_{REC}	Recover Time PR; CLR to CP (Waveform 3)	1.8 ± 0.15	$C_L = 15$ pF $R_D = 1$ M Ω $S_1 = \text{Open}$	8.0	–	–	8.0	–	ns
		2.5 ± 0.2		4.5	–	–	4.5	–	
		3.3 ± 0.3		3.0	–	–	3.0	–	
		5.0 ± 0.5		3.0	–	–	3.0	–	
		3.3 ± 0.3	$C_L = 50$ pF, $R_D = 500$ Ω , $S_1 = \text{Open}$	3.0	–	–	3.0	–	
		5.0 ± 0.5		3.0	–	–	3.0	–	

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/2$ (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

CAPACITIVE CHARACTERISTICS ($t_R = t_F = 3.0 \text{ ns}$)

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{OUT}	Output Capacitance	$V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC} 10 MHz, $V_{CC} = 5.5 \text{ V}$, $V_{IN} = 0 \text{ V}$ or V_{CC}	9 11	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50Ω)
 $f = 1 \text{ MHz}$

Figure 2. Test Circuit

Test	Switch Position	C_L , pF	R_L , Ω	R_1 , Ω
t_{PLH} / t_{PHL}	Open	See AC Characteristics Table		
t_{PLZ} / t_{PZL}	$2 \times V_{CC}$	50	500	500
t_{PHZ} / t_{PZH}	GND	50	500	500

X = Don't Care

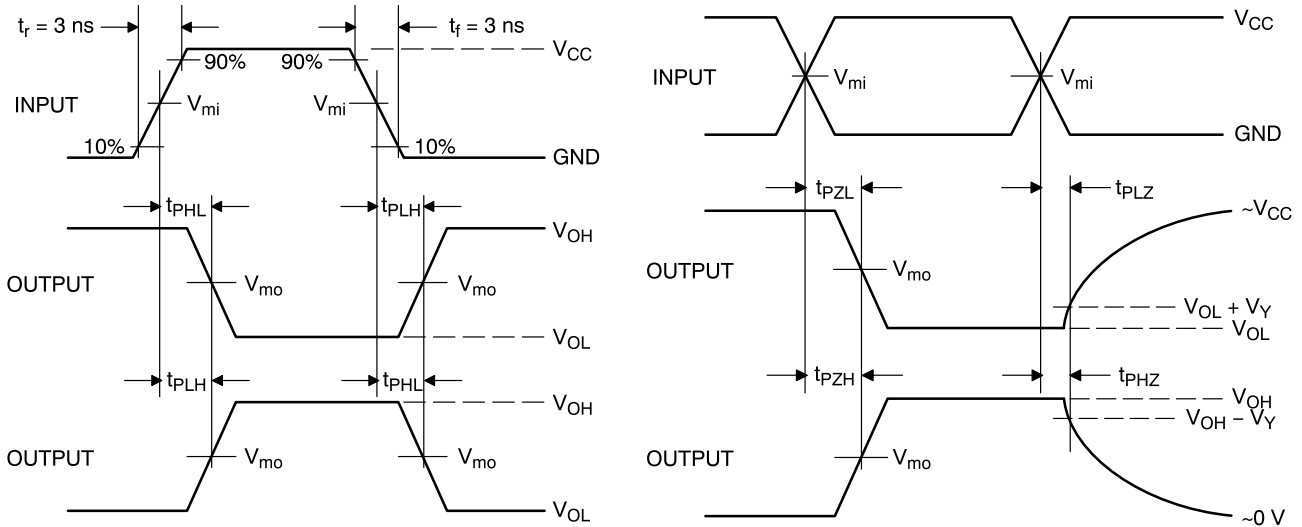


Figure 3. Switching Waveforms

NLV18SZ74

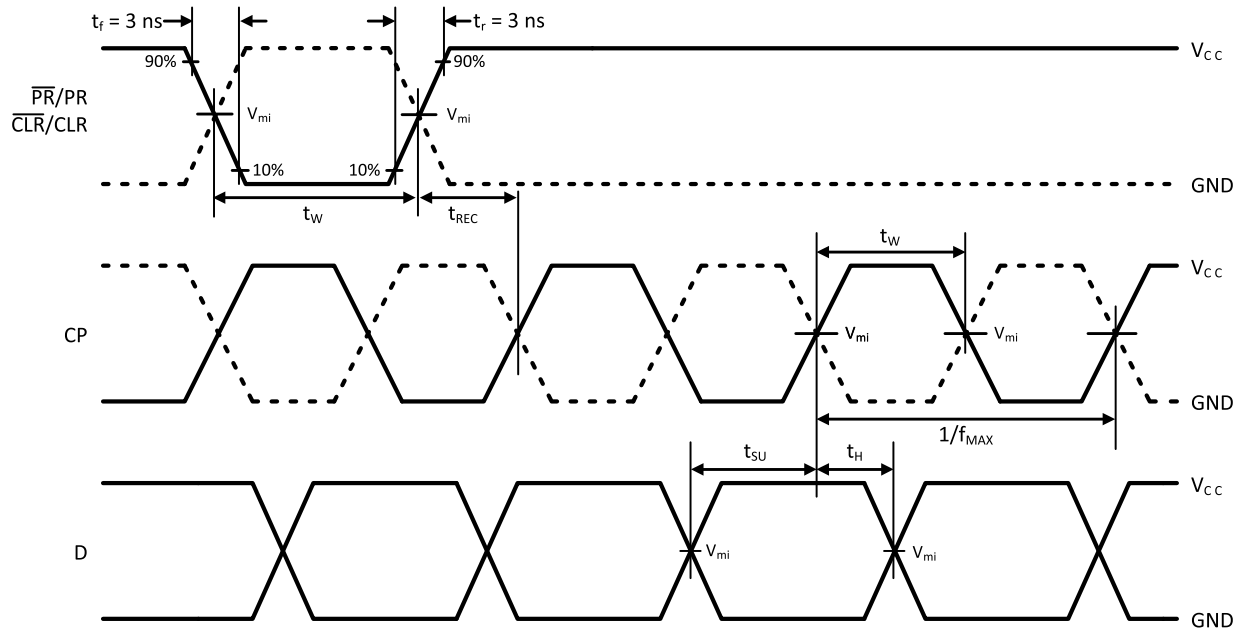


Figure 4. Setup, Hold and Recovery Time Waveforms

V_{CC}, V	V_{mi}, V	V_{mo}, V		V_Y, V
		t_{PLH}, t_{PHL}	$t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}$	
1.65 to 1.95	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.15
2.3 to 2.7	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.15
3.0 to 3.6	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.3
4.5 to 5.5	$V_{CC}/2$	$(V_{OH} - V_{OL})/2$	$V_{CC}/2$	0.3

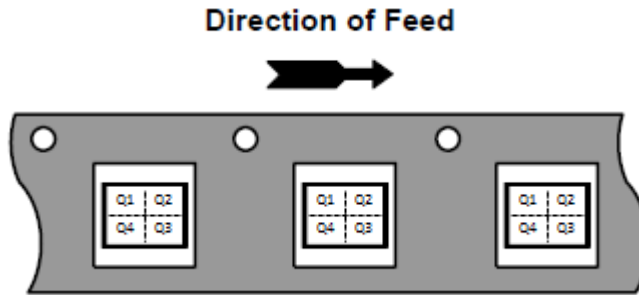
DEVICE ORDERING INFORMATION

Device	Packages	Marking	Pin 1 Orientation (See below)	Shipping [†]
NLV18SZ74USG	US8	MH	Q4	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

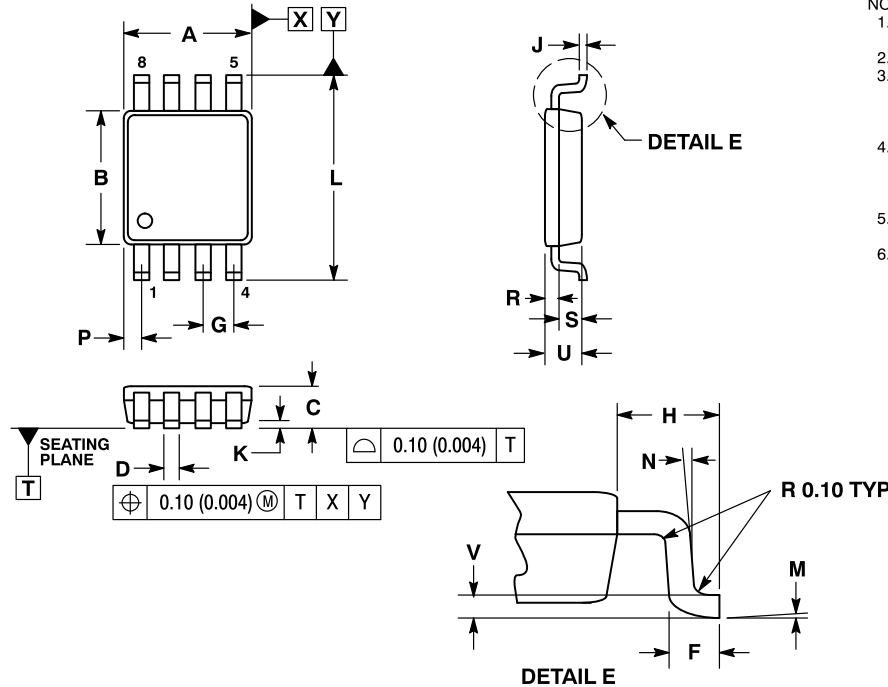
Pin 1 Orientation in Tape and Reel



NLV18SZ74

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE D

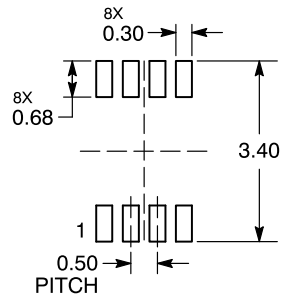


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.14MM (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203MM (0.003-0.008").
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED $\pm 0.0508\text{MM}$ (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.128
M	0°	6°	0°	6°
N	0°	10°	0°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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