

3.2Gbps, 1:2 Port Switch, SATA2/SAS ReDriver™

Features

- → Two 3.2Gbps differential signal
- → Adjustable Receiver Equalization
- → 100-Ohm Differential CML I/O's
- → Independent output level control
- → Input signal level detect and squelch for each channel
- → OOB support
- → Low Power (100mW per Channel)
- → Stand-by Mode Power Down State
- → V_{DD} Operating Range: 1.5V to 1.8V
- → Industrial Operating Temperature Range: -40°C to 85°C
- → Packaging: 28-TQFN (3.5x 5.5mm)

Description

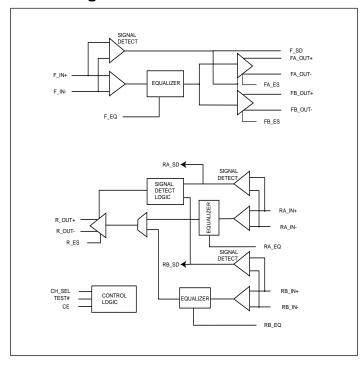
Pericom Semiconductor's PI2EQX3421 is a low power, signal ReDriver. The device provides programmable equalization, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference. PI2EQX3421 supports two 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal input to ReDriver.

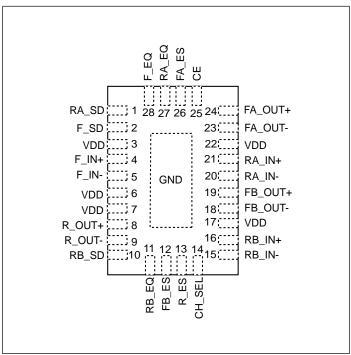
A low-level input signal detection and output squelch function is provided for each channel. Each channel operates fully independently. When the channels are enabled (CE=1) and operating, that channels input signal level (on XIN+/-) determines whether the output is enabled. If the input signal level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to signal conditioning, Pericom's PI2EQX3421 also provides power management Stand-by mode operated by the Chip Enable (CE) pin.

Block Diagram



Pin Description (Top Side View)



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Pin Description

Pin#	Pin Name	Type	Description	
25	СЕ	Input	Chip Enable "high" provides normal operation. "Low" for power down mode. With internal 50K-Ohm pull-up resistor.	
14	CH_SEL	Input	Channel Select "high" selects path A. "Low" selects path B. With internal 50K-Ohm pull-up resistor.	
28	F_EQ	Input	Selection pin for equalizer of Fin. "Low" means 2.5dB, "high" means 6.5dB. With internal 50K-Ohm pull-up resistor.	
4 5	F_IN+ F_IN-	Input	CML input channel F with internal 50-Ohm pull down.	
2	F_SD	Output	Channel Fin Signal detector output. Provides "high" when a signal is detected.	
26	FA_ES	Input	"High" means FA_OUT operates to the SATA i/m standard. "Low" means FA_OUT support SATAx standard. With internal 50K-Ohm pull-up resistor.	
24 23	FA_OUT+ FA_OUT-	Output	CML output channel FA with internal 50-Ohm pull up.	
12	FB_ES	Input	"High" means FB_OUT operates to the SATA i/m standard. "Low" means FB_OUT support SATAx standard. With internal 50K-Ohm pull-up resistor.	
19 18	FB_OUT+ FB_OUT-	Output	CML output channel FB with internal 50-Ohm pull up.	
Center Pad	GND	GND	Supply ground.	
13	R_ES	Input	"High" means Rout operates to the SATA i/m standard. "Low" means Rout support SATAx standard. With internal 50K-Ohm pull-up resistor.	
27	RA_EQ	Input	Selection pin for equalizer of RA_IN. "Low" means 2.5dB, "high" means 6.5dB. With internal 50K-Ohm pull-up resistor.	
21 20	RA_IN+ RA_IN-	Input	CML input channel RA with internal 50-Ohm pull down.	
1	RA_SD	Output	Signal detector for Channel RA_IN. Provides "high" when signal is detected.	
11	RB_EQ	Input	Selection pin for equalizer of RB_IN. "Low" means 2.5dB, "high" means 6.5dB. With internal 50K-Ohm pull-up resistor.	
16	RB_IN+	T	CML input channel RB with internal 50-Ohm pull down.	
15	RB_IN-	Input		
10	RB_SD	Output	Signal detector for Channel RB_IN. Provides "high" when signal is detected.	
8 9	R_OUT+ R_OUT-	Output	CML output channel R with internal 50-Ohm pull up.	
3,6,7,17,22	VDD	Power	Positive Supply Voltage, 1.5V to 1.8V (±0.1V)	

12/18/12



Equalizer Selection

x_EQ	Compliance Channel @ 1.6 GHz	
0	1.5dB ± 1.0dB	
1	5.5dB ± 1.0dB	

Output CML Buffer

CE	CH_SEL	X_ES	FA_OUT	FB_OUT	R_OUT
0	X	X	VDD	VDD	VDD
1	0	0	VDD	VDD-0.6V	VDD-0.6V
1	0	1	VDD	VDD-0.3V	VDD-0.3V
1	1	0	VDD-0.6V	VDD	VDD-0.6V
1	1	1	VDD-0.3V	VDD	VDD-0.3V



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	65°C to +150°C
Supply Voltage to Ground Potential	0.5V to +2.5V
DC SIG Voltage	0.5V to VDD +0.5V
Current Output	25mA to +25mA
Power Dissipation Continous	500mW
Operating Temperature	40 to +85°C

Note:

Stresses greater than those listed under MAXIMUM RAT-INGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics ($V_{DD} = 1.4V \text{ to } 1.9V$)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
P _{STANDBY}	Supply Power	CE = LVCMOS Low			1	mW
P _{ACTIVE}	Active Supply Power	CE = LVCMOS High			0.25	W
T _{pd}	Latency	Input to Output		1.0		ns
T_{SW}	Switch time, idle to active	CH_Sel toggles		50		ns
CML Receive	er Input					
V _{RX-DIFFP-P}	Differential Input Peak-to- peak Voltage		0.200			V
V _{RX-CM-ACP}	AC Peak Common Mode Input Voltage				150	mV
Z _{RX-DC}	DC Input Impedance		40	50	60	
Z _{RX-DIFF-DC}	DC Differential Input Impedance		85	100	115	Ohm
Equalization						
J _{RS}	Residual Jitter ^(1,2)	Total Jitter			0.3	Ulp-p
J_{RM}	Random Jitter ^(1,2)			1.5		psrms
Signal Detecto	r Performance					
V_{TH}	Threshold	CE = 1	65 ⁽³⁾		200 (3)	mVppd
T _{EN}	Enable/disable time				16	ns

Notes

- 1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
- 2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.
- 3. Using Compliance test at 1.5Gbps and 3Gbps. Also using OOB (OOB is formed by ALIGNp primitive or D24.3) test patterns at 1.5Gbps. The ALIGN primitive (K28.5+D10.2+D27.3=0011111010+010101011+0010011100). The D24.3 = 00110011001100110011

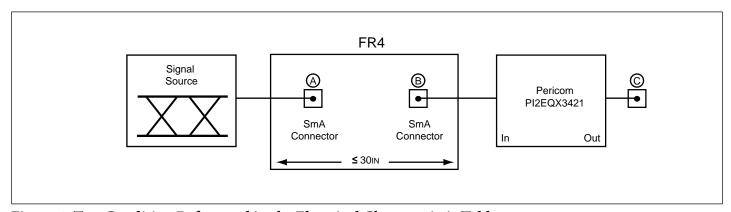


AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
CML Transmi	itter Output (100-Ohm differentia	al)	·				
V _{TX-DIFFP-P}	Differential Peak-to-peak Output Voltage ⁽¹⁾ V _{TX-DIFFP-P}	x_ES=1	400		750	mVppd	
	$= 2* V_{TX-D+} - V_{TX-D-} $	x_ES=0	800		1300		
1 7	Common-Mode Voltage ⁽¹⁾	x_ES=1		V _{DD} -0.6		mV	
V _{TX-C}	$ V_{TX-D+} + V_{TX-D-} / 2$	x_ES=0		V _{DD} -0.3			
t _F , t _R	Transition Time	20% to 80%			150	ps	
t_F - t_R / t_F + t_R	Transition Mismatch Time	20% to 80%			20	%	
Z _{OUT}	Output resistance	Single ended		50		Ohm	
Z _{TX-DIFF-DC}	DC Differential TX Impedance		80	100	120	Ohm	
C_{TX}	AC Coupling Capacitor		0.3	4.7	12	nF	
LVCMOS Con	ntrol Pins						
V_{IH}	Input High Voltage		0.65 × V _{DD}			- V	
V_{IL}	Input Low Voltage				$0.35 \times V_{\mathrm{DD}}$	V	
I_{IH}	Input High Current				250	」∧	
$I_{\rm IL}$	Input Low Current				500	μA	
V _{OH}	DC Output Logic High	$I_{OH} = 4mA$	V _{DD} - 0.45			V	
V_{OL}	DC Output Logic Low	$I_{OL} = 4mA$			0.4		

Note:

^{1.} When x_ES=0, select SATAx standard. When x_ES=1, select SATAI/m standard.

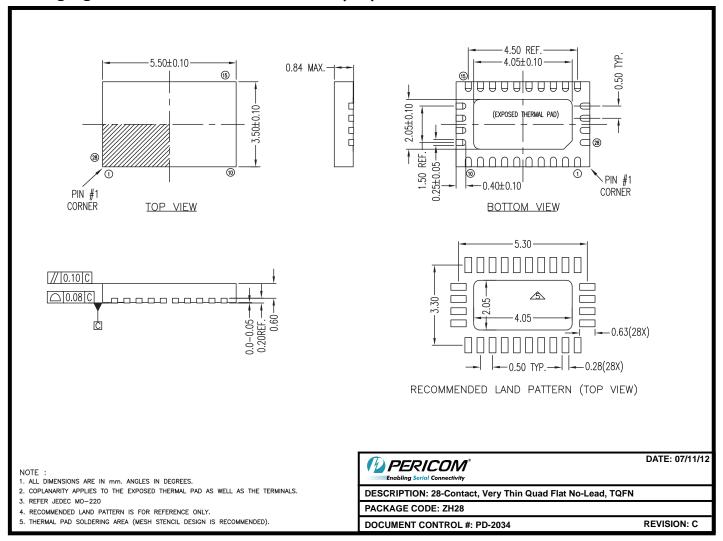


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Figure 1. Test Condition Referenced in the Electrical Characteristic Table



Packaging Mechanical: 28-contact TQFN (ZH)



12-0419 Note: For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3421ZHE	ZH	Pb-Free and Green 28-contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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