

NTE858M NTE858SM Integrated Circuit Dual, Low-Noise JFET-Input Operational Amplifier

Description:

The NTE858M and NTE858SM are dual, low-noise JFET input operational amplifiers combining two state-of-the-art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, these devices exhibit low-noise and low harmonic distortion making them ideal for use in high-fidelity audio amplifier applications.

Features:

- Available in Two Different Package Types:
8-Lead Mini DIP (NTE858M)
SOIC-8 Surface Mount (NTE858SM)
- Low Input Noise Voltage: $18\text{nV}/\sqrt{\text{Hz}}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: $10^{12}\Omega$ Typ
- High Slew Rate: $13\text{V}/\mu\text{s}$ Typ
- Wide Gain Bandwidth: 4MHz Typ
- Low Supply Current: 1.4mA per Amp

Absolute Maximum Ratings:

Supply Voltage

V_{CC}	+18V
V_{EE}	-18V

Differential Input Voltage, V_{ID} $\pm 30\text{V}$

Input Voltage Range (Note 1), V_{IDR} $\pm 15\text{V}$

Output Short-Circuit Duration (Note 2), t_S Continuous

Power Dissipation, P_D 680mW
Derate Above $T_A = +47^\circ\text{C}$ $10\text{mW}/^\circ\text{C}$

Operating Ambient Temperature Range, T_A 0° to $+70^\circ\text{C}$

Storage Temperature Range, T_{stg} -65° to $+150^\circ\text{C}$

Note 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15V, whichever is less.

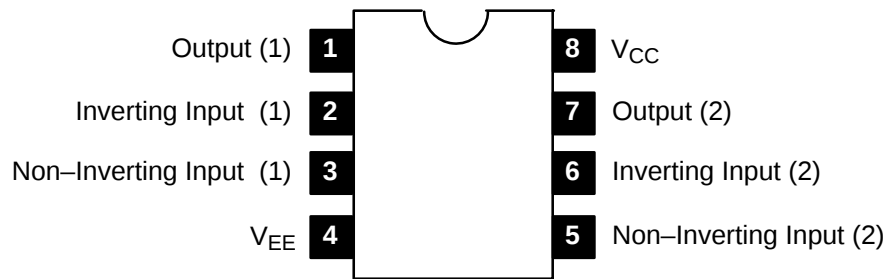
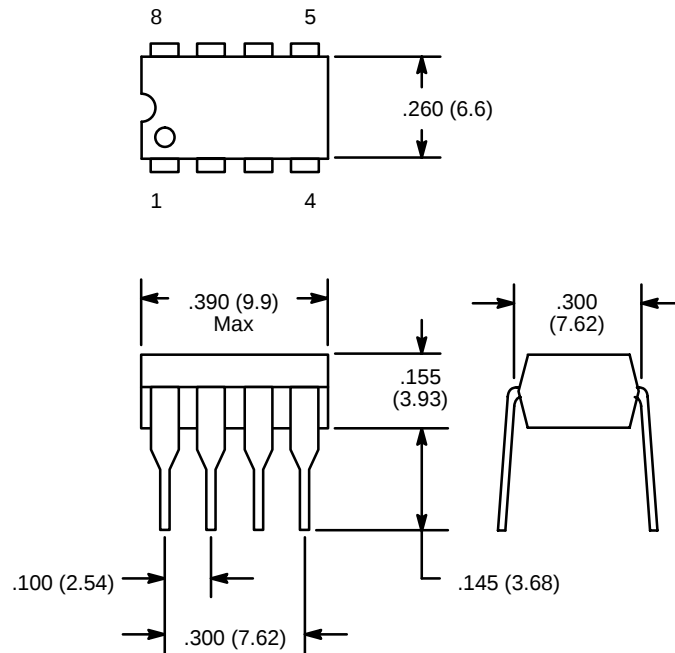
Note 2. The output may be shorted to GND or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

Electrical Characteristics: ($V_{CC} = +15V$, $V_{EE} = -15V$, $T_A = +25^{\circ}C$ unless otherwise specified)

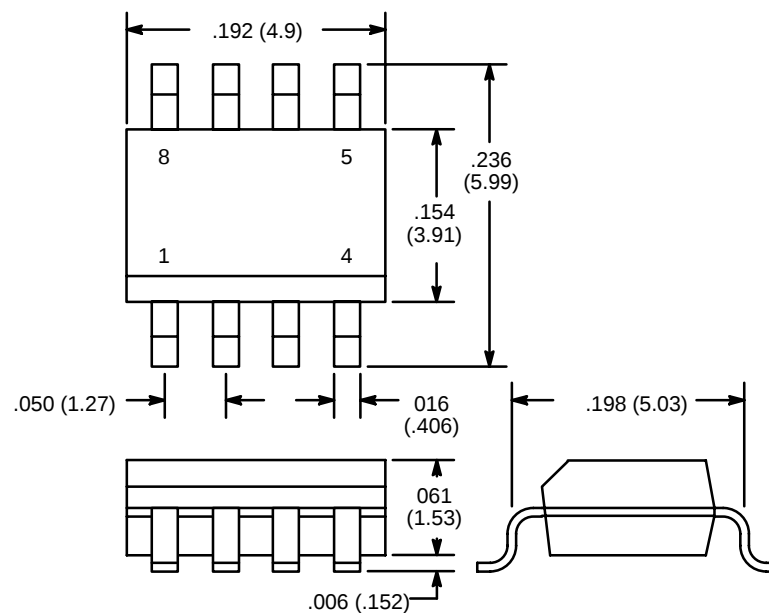
Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V _{IO}	R _S ≤ 10k, V _{CM} = 0		–	3	10	mV
			T _A = 0 to +70°C	–	–	13	mV
Average Temperature Coefficient of Input Offset Voltage	ΔV _{IO} /ΔT	T _A = 0 to +70°C		–	10	–	μV/°C
Input Offset Current	I _{IO}	V _{CM} = 0, Note 3		–	5	50	pA
			T _A = 0 to +70°C	–	–	2	nA
Input Bias Current	I _{IB}	V _{CM} = 0, Note 3		–	30	200	pA
			T _A = 0 to +70°C	–	–	7	nA
Input Resistance	r _i			–	10 ¹²	–	Ω
Common Mode Input Voltage Range	V _{ICR}			±10	+15, –12	–	V
Large–Signal Voltage Gain	A _{VOL}	V _O = ±10V, R _L ≤ 2k		25	150	–	V/mV
			T _A = 0 to +70°C	15	–	–	V/mV
Output Voltage Swing (Peak–to–Peak)	V _O	R _L = 10k	T _A = 0 to +70°C	24	28	–	V
		R _L ≥ 10k		24	–	–	V
		R _L ≥ 2k		20	–	–	V
Common Mode Rejection Ratio	CMRR	R _S ≤ 10k		70	100	–	dB
Supply Voltage Rejection Ratio	PSRR	R _S ≤ 10k		70	100	–	dB
Supply Current (Each Amplifier)	I _D			–	1.4	2.5	mA
Unity Gain Bandwidth	BW			–	4	–	MHz
Slew Rate	SR	V _{IN} = 10V, R _L = 2k, C _L = 100pF		–	13	–	V/μs
Rise Time	t _r			–	0.1	–	μs
Overshoot Factor		V _{IN} = 20mV, R _L = 2k, C _L = 100pF		–	10	–	%
Equivalent Input Noise Voltage	e _n	R _S = 100Ω, f = 1000Hz		–	18	–	nV/√Hz
Equivalent Input Noise Current	i _n	R _S = 100Ω, f = 1000Hz		–	0.01	–	pA/√Hz
Total Harmonic Distortion	THD	V _{O(RMS)} = 10V, R _S ≤ 1k, R _L ≥ 2k, f = 1000Hz		–	0.01	–	%
Channel Separation		A _V = 100		–	120	–	dB

Note 3. Input Bias currents of JFET input operational amplifiers approximately double for every $10^{\circ}C$ rise in Junction Temperature. To maintain Junction Temperature as close to Ambient Temperature as possible, pulse techniques must be used during test.

Pin Connection Diagram

**NTE858M**

NTE858SM



NOTE: Pin1 on Beveled Edge