Quad 2-Input AND Gate

The MC74VHCT08A is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5 V CMOS level output swings.

The VHCT08A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 4.3 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max) at $T_A = 25^{\circ}C$
- TTL-Compatible Inputs: $V_{IL} = 0.8 \text{ V}$; $V_{IH} = 2.0 \text{ V}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 24 FETs or 6 Equivalent Gates
- These devices are manufactured with a Pb-Free external lead finish only.

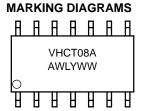


ON Semiconductor®

http://onsemi.com



SOIC-14 **D SUFFIX** CASE 751A





TSSOP-14 **DT SUFFIX CASE 948G**



 Π Π Π Π Π Π



VHCT08A **AWLYWW**

SOFIAJ-14 **M SUFFIX CASE 965**

> VHCT08A = Specific Device Code = Assembly Location

= Wafer Lot WL = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†]	
MC74VHCT08ADR2	SOIC-14	2500 / Tape & Reel	
MC74VHCT08ADTR2	TSSOP-14 (Pb-Free)	2500 / Tape & Reel	
MC74VHCT08AM	SOEIAJ-14 (Pb-Free)	50 Units / Rail	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

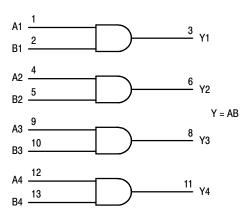


Figure 1. Logic Diagram

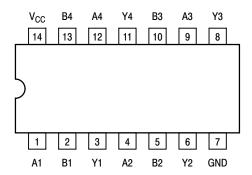


Figure 2. Pinout: 14-Lead Packages (Top View)

FUNCTION TABLE

Inp	uts	Output
Α	В	Y
L	L	L
L	Н	L
Н	L	L
Н	Н	н
l	l	l .

MAXIMUM RATINGS*

Symbol	Paramete	7	Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
V _{in}	DC Input Voltage	-0.5 to +7.0	V	
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V	
I _{IK}	Input Diode Current	-20	mA	
I _{OK}	Output Diode Current		±20	mA
I _{out}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and G	ND Pins	±50	mA
P _D	Power Dissipation in Still Air,	SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature		-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature	-40	+ 85	°C
t _r , t _f	Input Rise and Fall Time $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	20	ns/V

DC ELECTRICAL CHARACTERISTICS

			V _{CC} T _A =		T _A = 25°C		T _A = 25°C		$T_{A} \le 85^{\circ}C$		$T_A \le 125^{\circ}C$		
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit		
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V		
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V		
V _{OH}	Minimum High-Level Output Voltage $V_{IN} = V_{IH}$ or V_{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V		
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66				
V _{OL}		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu A$	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V		
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52			
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ		
Icc	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			2.0		20		40	μΑ		
I _{CCT}	Quiescent Supply Current	Input: V _{IN} = 3.4 V	5.5			1.35		1.50		1.65	mA		
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0			0.5		5.0		10	μΑ		

^{*} Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

[†]Derating – SOIC Packages: – 7 mW/°C from 65° to 125°C TSSOP Package: – 6.1 mW/°C from 65° to 125°C

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

			Т	A = 25°	С	T _A ≤	85°C	T _A ≤ '	125°C	
Symbol	Parameter	Test Conditions	Min	Тур	Max	Min	Max	Max	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A or B to Y	$V_{CC} = 3.0 \pm 0.3 V$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		6.2 8.7	8.8 12.3		10.5 14.0		14.0 17.5	ns
		$V_{CC} = 5.0 \pm 0.5 V$ $C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		4.3 5.8	5.9 7.9		7.0 9.0		9.0 11.0	
C _{in}	Maximum Input Capacitance			4	10		10		10	pF

		Typical @ 25°C, V _{CC} = 5.0V	
C _{PD}	Power Dissipation Capacitance (Note 1)	20	pF

^{1.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per gate). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.7

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

		T _A = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

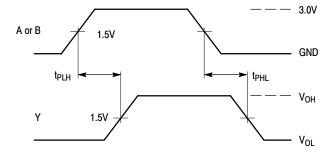
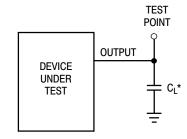


Figure 3. Switching Waveforms

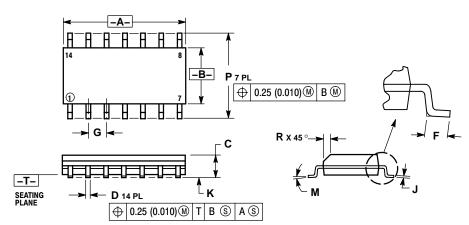


*Includes all probe and jig capacitance

Figure 4. Test Circuit

PACKAGE DIMENSIONS

SOIC-14 **D SUFFIX** CASE 751A-03 ISSUE G



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 114.5M, 1982.

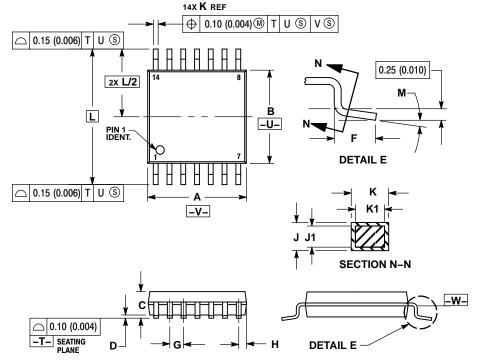
 CONTROLLING DIMENSION: MILLIMETER.

 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- 4. MAXIMUM MOLD PHOTHUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES			
DIM	MIN	MAX	MIN	MAX			
Α	8.55	8.75	0.337	0.344			
В	3.80	4.00	0.150	0.157			
С	1.35	1.75	0.054	0.068			
D	0.35	0.49	0.014	0.019			
F	0.40	1.25	0.016	0.049			
G	1.27 BSC		0.050	BSC			
J	0.19	0.25	0.008	0.009			
K	0.10	0.25	0.004	0.009			
M	0°	7°	0°	7°			
Р	5.80	6.20	0.228	0.244			
R	0.25	0.50	0.010	0.019			

TSSOP-14 **D SUFFIX** CASE 948G-01 ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI DIMENSION Y14.5M, 1982.
- 114.3/M, 1962.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD
- FLASH OR GATE BURRS UN GAILE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED
- EXCEED
 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	6 BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40	BSC	0.252 BSC		
M	0°	8°	0°	8°	

PACKAGE DIMENSIONS

SOEIAJ-14 **M SUFFIX** CASE 965-01 **ISSUE O** Ε HE **DETAIL P** VIEW P е 0.13 (0.005) M 0.10 (0.004)

NOTES:

- 1. DIMENU. Y14.5M, 1982. DIMENSIONING AND TOLERANCING PER ANSI
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS D AND E DO NOT INCLUDE
 MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
- THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH
 DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α		2.05		0.081		
A ₁	0.05	0.20	0.002	0.008		
q	0.35	0.50	0.014	0.020		
O	0.18	0.27	0.007	0.011		
D	9.90	10.50	0.390	0.413		
Е	5.10	5.45	0.201	0.215		
е	1.27	BSC	0.050	BSC		
HE	7.40	8.20	0.291	0.323		
0.50	0.50	0.85	0.020	0.033		
F	1.10	1.50	0.043	0.059		
М	0 °	10°	0 °	10°		
Q1	0.70	0.90	0.028	0.035		
Z		1.42		0.056		

ON Semiconductor and un are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 61312, Phoenix, Arizona 85082-1312 USA Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Japan: ON Semiconductor, Japan Customer Focus Center 2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051 Phone: 81-3-5773-3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.