Rochester Electronics®

Datasheet

87C196KR

16-Bit CHMOS Microcontrollers

The 87C196KR, JV, JT, JR, and CA devices represent the fourth generation of MCS® 96 microcontroller products implemented on Intel's advanced 1 micron process technology. These products are based on the 80C196KB device with improvements for automotive applications. The instruction set is a true super set of 80C196KB. The 87C196JR, JT, and JV are 52-pin versions of the 87C196KR device.

The 87C196JV and JT devices are memory scalars of the 87C196JR and are designed for strict functional and electrical compatibility. The JT has 32 Kbytes of on-chip EPROM, 1.0 Kbytes of Register RAM and 512 bytes of Code RAM. The JV has 48 Kbytes of onchip EPROM, 1.5 Kbytes of Register RAM and 512 bytes of Code RAM.

The 87C196CA device is a memory scalar of the 87C196KR in a 68-pin package with 32 Kbytes of on-chip EPROM, 1.0 Kbytes of register RAM, and 256 bytes of code RAM. In addition, the CA contains an extra peripheral for serial communications protocol CAN 2.0.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

FOR REFERENCE ONLY

87C196KR, 87C196JV, 87C196JT, 87C196JR, and 87C196CA Advanced 16-Bit CHMOS Microcontrollers

Automotive

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Product Features

- –40°C to +125°C Ambient
- High Performance CHMOS 16-Bit CPU
- Up to 48 Kbytes of On-Chip EPROM
- Up to 1.5 Kbytes of On-Chip Register RAM
- Up to 512 Bytes of Additional RAM (Code RAM)
- Register-Register Architecture
- Up to Eight Channel/10-Bit A/D with Sample/Hold
- Up to 37 Prioritized Interrupt Sources
- Up to Seven 8-Bit (56) I/O Ports
- Full Duplex Serial I/O Port
- Dedicated Baud Rate Generator
- Interprocessor Communication Slave Port
- High Speed Peripheral Transaction Server (PTS)
- Two 16-Bit Software Timers
- Up to 10 High Speed Capture/Compare (EPA)
- Full Duplex Synchronous Serial I/O Port (SSIO)
- Two Flexible 16-Bit Timer/Counters
- Quadrature Counting Inputs
- Flexible 8-/16-Bit External Bus
- Programmable Bus (HLD/HLDA)
- 1.75 µs 16 x 16 Multiply
- 3 µs 32/16 Divide
- 68-Pin and 52-Pin PLCC Packages
- Supports CAN (Controller Area Network) Specification 2.0 (CA only)

Order Number: 270827-008
August 2004

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1.0 Introduction

The MCS 96 microcontroller family members are all high performance microcontrollers with a 16-bit CPU.

The 87C196Kx and Jx family members are composed of the high-speed (16 MHz) core as well as the following peripherals:

- Up to 48 Kbytes of Programmable EPROM
- Up to 1.5 Kbytes of register RAM and 512 bytes of code RAM (16-bit addressing modes) with the ability to execute from this RAM space
- Up to eight channels–10-Bit/ ± 3 LSB analog to digital converter with programmable S/H times with conversion times < 5 µs at 16 MHz
- An asynchronous/synchronous serial I/O port (8096 compatible) with a dedicated 16-bit baud rate generator
- Interprocessor communication slave port
- Synchronous serial I/O port with full duplex master/slave transceivers
- A flexible timer/counter structure with prescaler, cascading, and quadrature capabilities
- Up to ten modularized multiplexed high speed I/O for capture and compare (called Event Processor Array) with 250 ns resolution and double buffered inputs
- A sophisticated prioritized interrupt structure with programmable Peripheral Transaction Server (PTS). The PTS has several channel modes, including single/ burst block transfers from any memory location to any memory location, a PWM and PWM toggle mode to be used in conjunction with the EPA, and an A/D scan mode.
- Serial communications protocol CAN 2.0 with 15 message objects of 8 bytes data length (CA only)

The 87C196KR, JV, JT, JR, and CA devices represent the fourth generation of MCS® 96 microcontroller products implemented on Intel's advanced 1 micron process technology. These products are based on the 80C196KB device with improvements for automotive applications. The instruction set is a true super set of 80C196KB. The 87C196JR, JT, and JV are 52-pin versions of the 87C196KR device.

The 87C196JV and JT devices are memory scalars of the 87C196JR and are designed for strict functional and electrical compatibility. The JT has 32 Kbytes of on-chip EPROM, 1.0 Kbytes of Register RAM and 512 bytes of Code RAM. The JV has 48 Kbytes of on-chip EPROM, 1.5 Kbytes of Register RAM and 512 bytes of Code RAM.

The 87C196CA device is a memory scalar of the 87C196KR in a 68-pin package with 32 Kbytes of on-chip EPROM, 1.0 Kbytes of register RAM, and 256 bytes of code RAM. In addition, the CA contains an extra peripheral for serial communications protocol CAN 2.0.

Table 1 summarizes the features of the 87C196Kx, Jx, and CA devices.

Table 1. 87C196Kx and Jx Features Summary

Device	Pins/Package	EPROM	Reg RAM	Code RAM	I/O	EPA	SIO	SSIO	A/D
87C196KR	68-Pin PLCC	16 K	512	256	56	10	Y	Y	8
87C196JV	52-Pin PLCC	48 K	1.5 K	512	41	6	Y	Y	6
87C196JT	52-Pin PLCC	32 K	1.0 K	512	41	6	Y	Y	6
87C196JR	52-Pin PLCC	16 K	512	256	41	6	Y	Y	6
87C196CA	68-Pin PLCC	32 K	1.0 K	256	38	6	Y	Y	6

Refer to the following datasheets for higher frequency versions of devices contained within this datasheet:

- *87C196JT 20 MHz Advanced 16-Bit CHMOS Microcontroller* datasheet, order #272529
- *87C196JV 20 MHz Advanced 16-Bit CHMOS Microcontroller* datasheet, order #272580.

2.0 Architecture

The 87C196KR, JV, JT, JR, and CA are members of the MCS 96 microcontroller family, have the same architecture and use the same instruction set as the 80C196KB/KC. Many new features have been added including:

2.1 CPU Features

- Powerdown and Idle Modes
- 16 MHz Operating Frequency
- A High Performance Peripheral Transaction Server (PTS)
- Up to 37 Interrupt Vectors
- Up to 512 Bytes of Code RAM
- Up to 1.5 Kbytes of Register RAM
- “Windowing” Allows 8-Bit Addressing to Some 16-Bit Addresses
- 1.75 µs 16 x 16 Multiply
- 3 µs 32/16 Divide
- Oscillator Fail Detect

2.2 Peripheral Features

- Programmable A/D Conversion and S/H Times
- Up to 10 Capture/Compare I/O with 2 Flexible Timers

- Synchronous Serial I/O Port for Full Duplex Serial I/O
- Total Utilization of ALL Available Pins (I/O Mux'd with Control)
- Two 16-Bit Timers with Prescale, Cascading and Quadrature Counting Capabilities
- Up to 12 Externally Triggered Interrupts

2.3 New Instructions

2.3.1 XCH/XCHB

Exchange the contents of two locations, either Word or Byte is supported.

2.3.2 BMOVi

Interruptable Block Move Instruction, allows the user to be interrupted during long executing Block Moves.

2.3.3 TIJMP

Table Indirect JUMP. This instruction incorporates a way to do complex CASE level branches through one instruction. An example of such code savings: several interrupt sources and only one interrupt vector. The TIJMP instruction will sort through the sources and branch to the appropriate sub-code level in one instruction. This instruction was added especially for the EPA structure, but has other code saving advantages.

2.3.4 EPTS/DPTS

Enable and Disable PTS Interrupts (Works like EI and DI).

2.4 SFR Operation

An additional 256 bytes of SFR registers were added to the 8XC196Kx, Jx, and CA devices. These locations were added to support the wide range of on-chip peripherals that these devices have. This memory space (1F00–1FFFH) has the ability to be addressed as direct 8-bit addresses through the “windowing” technique. Any 32-, 64- or 128-byte section can be relocated in the upper 32, 64 or 128 bytes of the internal register RAM (080–FFH) address space. The CA contains an additional 256 bytes of SFR registers for CAN functions located in memory space IE00-1EFFh.

Figure 1. Block Diagram

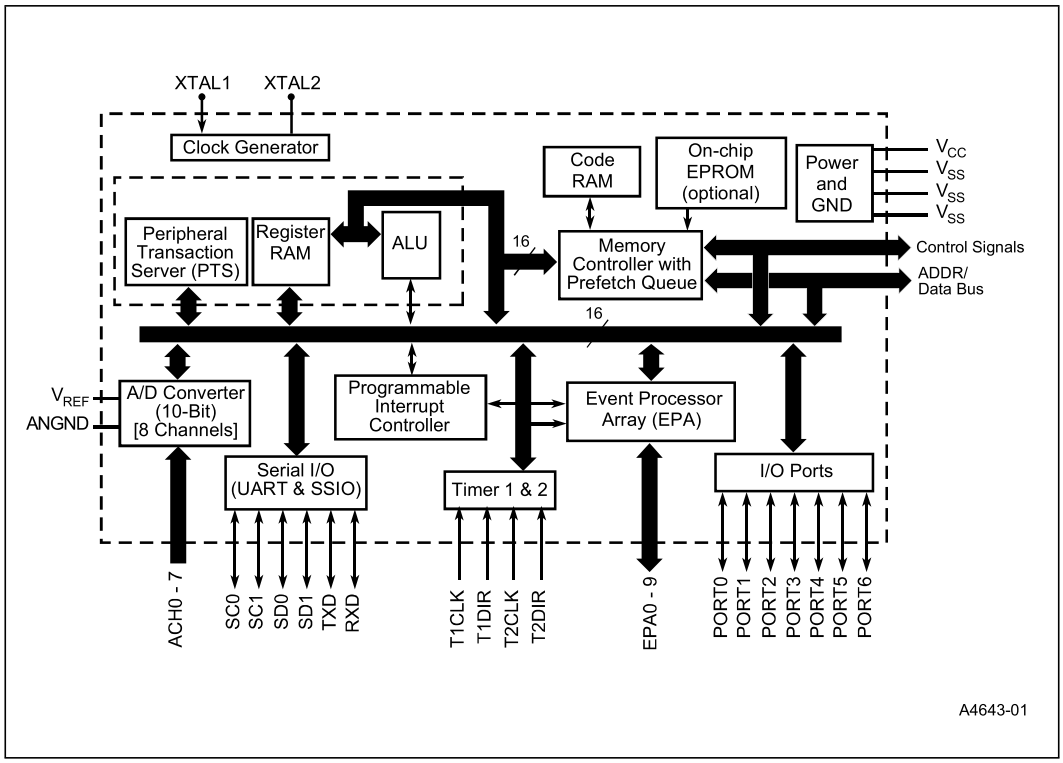
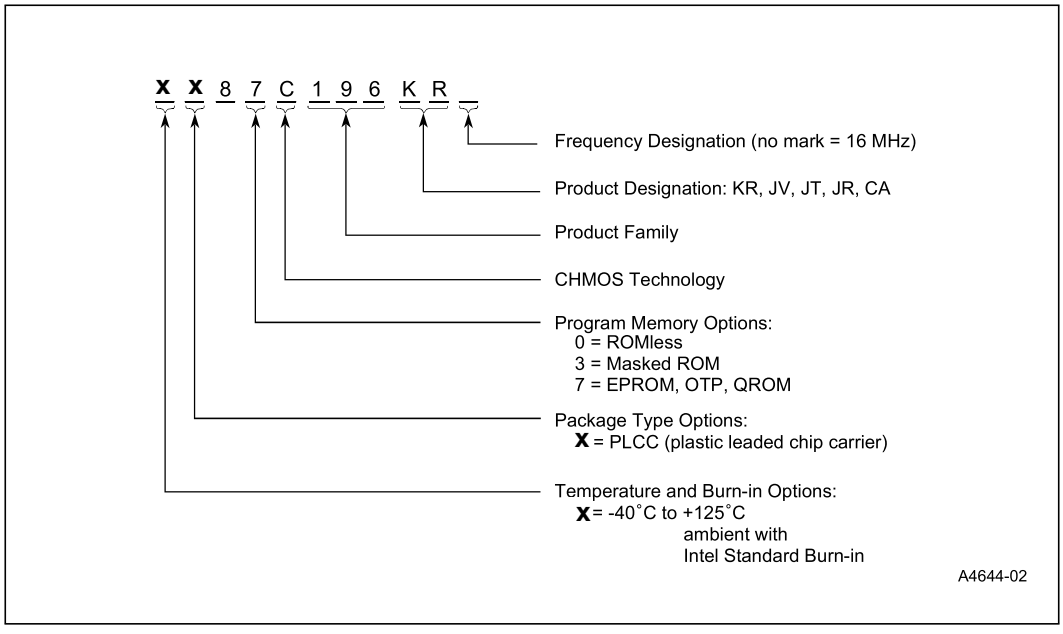


Figure 2. 8XC196Kx, Jx, and CA Family Nomenclature



3.0 Packaging Information

Figure 3. 87C196KR 68-Pin PLCC Package Diagram

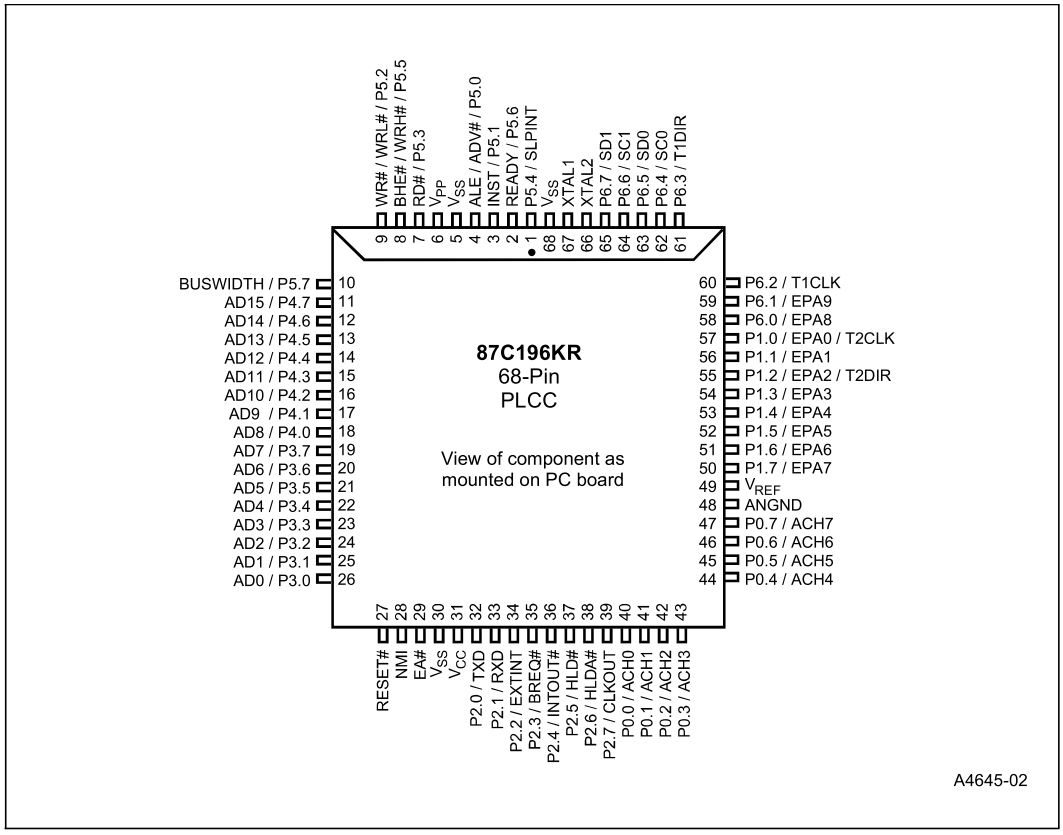


Figure 4. 87C196JV, JT, JR 52-Pin PLCC Package Diagram

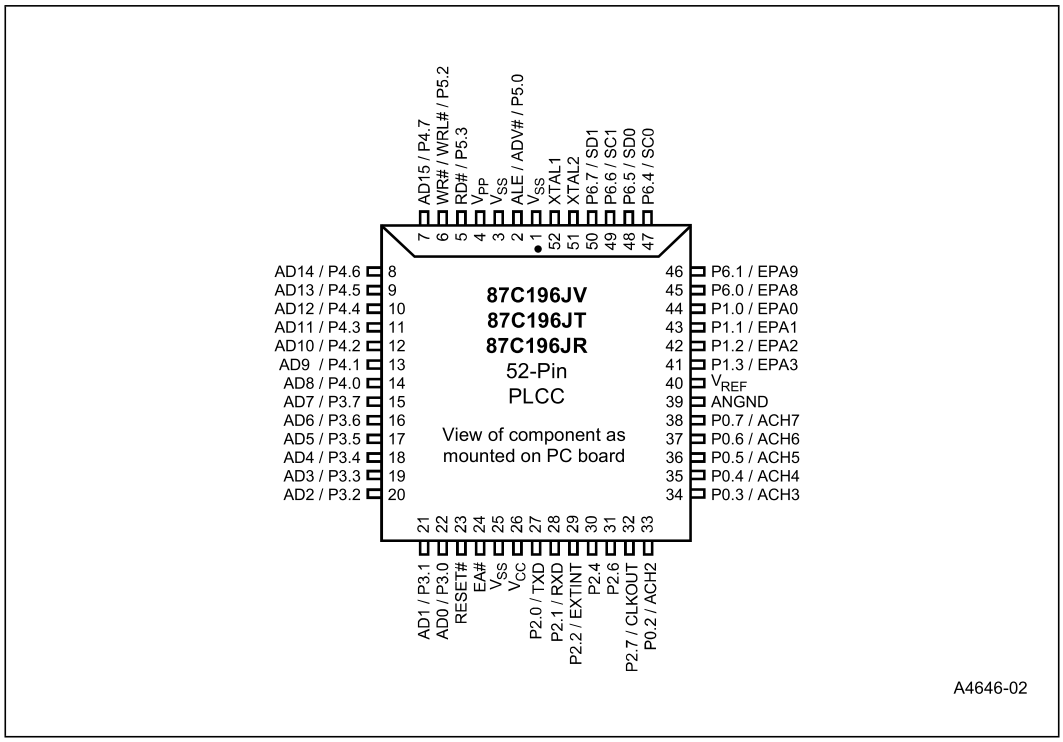


Figure 5. 87C196CA 68-Pin PLCC Package Diagram

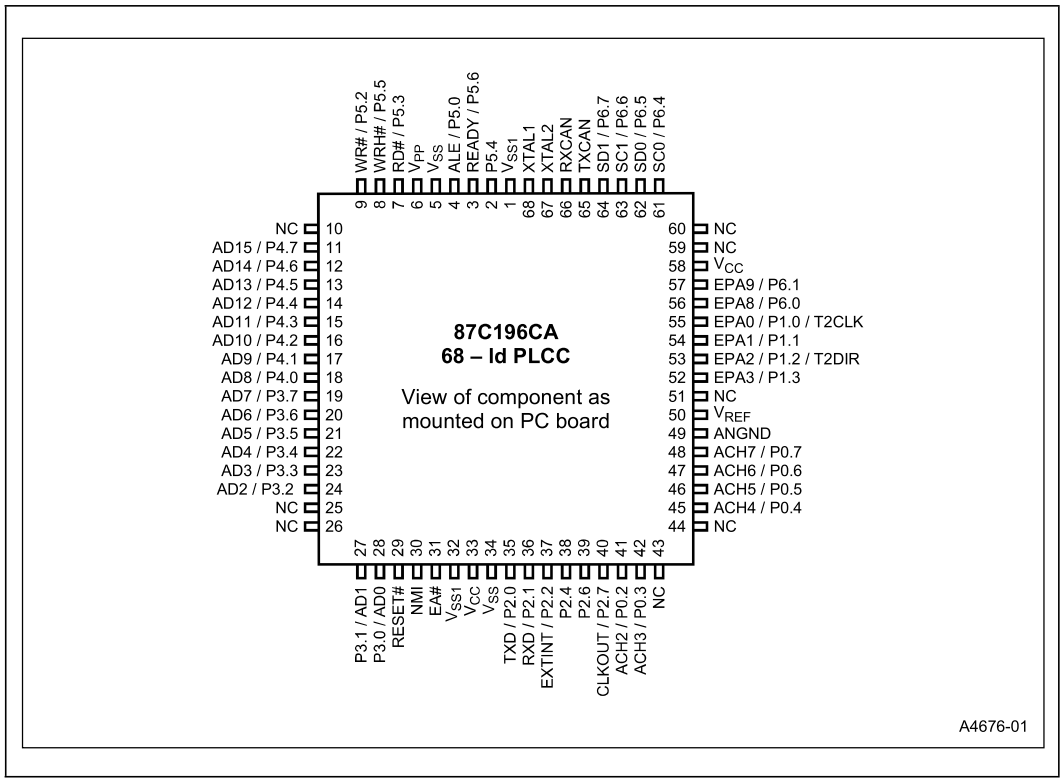


Table 2. Pin Descriptions (Sheet 1 of 2)

Symbol	Name and Function
V_{CC}	Main supply voltage (+5 V).
V_{SS}	Digital circuit ground (0 V). There are three V_{SS} pins, all of which MUST be connected to a single ground plane.
V_{REF}	Reference for the A/D converter (+5 V). V_{REF} is also the supply voltage to the analog portion of the A/D converter and the logic used to read Port 0. Must be connected for A/D and Port 0 to function.
V_{PP}	Programming voltage for the EPROM parts. It should be +12.5 V for programming. It is also the timing pin for the return from powerdown circuit. Connect this pin with a 1 µF capacitor to V_{SS} and a 1 MΩ resistor to V_{CC}. If this function is not used, V_{PP} may be tied to V_{CC}.
ANGND	Reference ground for the A/D converter. Must be held at nominally the same potential as V_{SS}.
XTAL1	Input of the oscillator inverter and the internal clock generator.
XTAL2	Output of the oscillator inverter.
P2.7/CLKOUT	Output of the internal clock generator. The frequency is ½ the oscillator frequency. It has a 50% duty cycle. Also LSIO pin when not used as CLKOUT.
RESET#	Reset input to the chip. Input low for at least 16 state times will reset the chip. The subsequent low to high transition resynchronizes CLKOUT and commences a 10-state time sequence in which the PSW is cleared, bytes are read from 2018H and 201AH loading the CCBs, and a jump to location 2080H is executed. Input high for normal operation. RESET# has an internal pullup.
P5.7/BUSWIDTH	Input for bus width selection. If CCR bit 1 is a one and CCR1 bit 2 is a one, this pin dynamically controls the Bus width of the bus cycle in progress. If BUSWIDTH is low, an 8-bit cycle occurs. If BUSWIDTH is high, a 16-bit cycle occurs. If CCR bit 1 is “0” and CCR1 bit 2 is “1”, all bus cycles are 8-bit; if CCR bit 1 is “1” and CCR1 bit 2 is “0”, all bus cycles are 16-bit. CCR bit 1 =”0" and CCR1 bit 2 = “0” is illegal. Also an LSIO pin when not used as BUSWIDTH.
NMI	A positive transition causes a non-maskable interrupt vector through memory location 203EH.
P5.1/INST	Output high during an external memory read indicates the read is an instruction fetch. INST is valid throughout the bus cycle. INST is active only during external memory fetches. During internal [EP]ROM fetches INST is held low. Also LSIO when not INST.
EA#	Input for memory select (External Access). EA# equal to a high causes memory accesses within the [EP]ROM address space to be directed to on-chip EPROM/ ROM. EA# equal to a low causes accesses to these locations to be directed to off-chip memory. EA# = +12.5 V causes execution to begin in the Programming Mode. EA# latched at reset.
P5.0/ALE/ADV#	Address Latch Enable or Address Valid output, as selected by CCR. Both pin options provide a latch to demultiplex the address from the address/data bus. When the pin is ADV#, it goes inactive (high) at the end of the bus cycle. ADV# can be used as a chip select for external memory. ALE/ADV# is active only during external memory accesses. Also LSIO when not used as ALE.
P5.3/RD#	Read signal output to external memory. RD# is active only during external memory reads. LSIO when not used as RD#.
P5.2/WR#/WRL#	Write and Write Low output to external memory, as selected by the CCR, WR# will go low for every external write, while WRL# will go low only for external writes where an even byte is being written. WR#/WRL# is active during external memory writes. Also an LSIO pin when not used as WR#/WRL#.

Table 2. Pin Descriptions (Sheet 2 of 2)

Symbol	Name and Function
P5.5/BHE#/WRH#	Byte High Enable or Write High output, as selected by the CCR. BHE# = 0 selects the bank of memory that is connected to the high byte of the data bus. A0 = 0 selects that bank of memory that is connected to the low byte. Thus accesses to a 16-bit wide memory can be to the low byte only (A0 = 0, BHE# =1), to the high byte only (A0 = 1, BHE# = 0) or both bytes (A0 = 0, BHE# = 0). If the WRH# function is selected, the pin will go low if the bus cycle is writing to an odd memory location. BHE#/WRH# is only valid during 16-bit external memory write cycles. Also an LSIO pin when not BHE#/WRH#.
P5.6/READY	Ready input to lengthen external memory cycles, for interfacing with slow or dynamic memory, or for bus sharing. If the pin is high, CPU operation continues in a normal manner. If the pin is low prior to the falling edge of CLKOUT, the memory controller goes into a wait state mode until the next positive transition in CLKOUT occurs with READY high. When external memory is not used, READY has no effect. The max number of wait states inserted into the bus cycle is controlled by the CCR/CCR1. Also an LSIO pin when READY is not selected.
P5.4/SLPINT	Dual functional I/O pin. As a bidirectional port pin (LSIO) or as a system function. The system function is a Slave Port Interrupt Output Pin.
P6.2/T1CLK	Dual function I/O pin. Primary function is that of a bidirectional I/O pin (LSIO); however it may also be used as a TIMER1 Clock input. The TIMER1 will increment or decrement on both positive and negative edges of this pin.
P6.3/T1DIR	Dual function I/O pin. Primary function is that of a bidirectional I/O pin (LSIO); however it may also be used as a TIMER1 Direction input. The TIMER1 will increment when this pin is high and decrements when this pin is low.
PORT1/EPA0–7 P6.0–6.1/EPA8–9	Dual function I/O port pins. Primary function is that of bidirectional I/O (LSIO). System function is that of High Speed capture and compare. EPA0 and EPA2 have yet another function of T2CLK and T2DIR of the TIMER2 timer/counter.
PORT 0/ACH0–7	8-bit high impedance input-only port. These pins can be used as digital inputs and/or as analog inputs to the on-chip A/D converter. These pins are also used as inputs to EPROM parts to select the Programming Mode.
P6.4–6.7/SSIO	Dual function I/O ports that have a system function as Synchronous Serial I/O. Two pins are clocks and two pins are data, providing full duplex capability.
PORT 2	8-bit multi-functional port. All of its pins are shared with other functions.
PORT 3 and 4	8-bit bidirectional I/O ports with open drain outputs. These pins are shared with the multiplexed address/data bus which has strong internal pullups.
TXCAN	Push-pull output to the CAN bus line.
RXCAN	High-impedance input-only from the CAN bus line.

4.0 Electrical Characteristics

Note: This document contains information on products in production. The specifications are subject to change without notice.

4.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–60°C to +150°C
Voltage from V_{PP} or EA# to V_{SS} or ANGND	–0.5 V to +13.0 V
Voltage from any other pin to V_{SS} or ANGND	–0.5 V to +7.0 V
Power Dissipation	0.5 W

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.

4.2 Operating Conditions

Table 4. Operating Conditions

Parameter	Values
T_A (Ambient Temperature Under Bias)	–40°C to +125°C
V_{CC} (Digital Supply Voltage)	4.50 V to 5.50 V
V_{REF} (Analog Supply Voltage) (Notes 1, 2)	4.50 V to 5.50 V
F_{OSC} (Oscillator Frequency):	4 MHz to 16 MHz(2)

NOTE:
1. ANGND and V_{SS} should be nominally at the same potential.
2. Device is static and should operate below 1 Hz, but only tested down to 4 MHz.

Warning: Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

4.3 DC Characteristics

Table 5. DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
I_{CC}	V_{CC} supply current (–40°C to +125°C ambient)		50	75 (JV=80) (CA=90)	mA	X_{TAL1} = 16 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V (While device is in reset)
I_{CC1}	Active mode supply current (typical)		50 (JV=55)		mA	
I_{REF}	A/D reference supply current		2	5	mA	
I_{IDLE}	Idle mode current		15	30 (JV=32) (CA=40)	mA	X_{TAL1} = 16 MHz, $V_{CC} = V_{PP} = V_{REF}$ = 5.5 V
I_{PD}	Powerdown mode current		50		µA	$V_{CC} = V_{PP} = V_{REF}$ = 5.5 V (Note 4)
V_{IL}	Input low voltage (all pins)	–0.5 V		0.3 V_{CC}	V	
V_{IH}	Input high voltage (all pins)	0.7 V_{CC}		V_{CC} + 0.5	V	(Note 5)
V_{OL}	Output low voltage (outputs configured as push/pull)			0.3 0.45 1.5	V	I_{OL} = 200 µA (Note 3) I_{OL} = 3.2 mA I_{OL} = 7.0 mA
V_{OH}	Output high voltage (outputs configured as complementary)	V_{CC} – 0.3 V_{CC} – 0.7 V_{CC} – 1.5			V	I_{OH} = – 200 µA (Note 3) I_{OH} = – 3.2 mA I_{OH} = – 7.0 mA
I_{LI}	Input leakage current (standard inputs)			± 8 JT,JV,CA: ±10	µA	$V_{SS} \le V_{IN} \le V_{CC}$ (Note 2)
I_{LI1}	Input leakage current (Port 0—A/D inputs)			± 1 JT,JV: ±2 CA: ±1.5	µA	$V_{SS} \le V_{IN} \le V_{CC}$
I_{IH}	Input high current (NMI pin)			+175	µA	$V_{SS} \le V_{IN} \le V_{CC}$
V_{OH1}	SLPINT (P5.4) and HLDA (P2.6) Output high voltage in RESET	2.0			V	I_{OH} = 0.8 mA (Note 8)
V_{OH2}	Output high voltage in RESET	V_{CC} – 1 V			V	I_{OH} = – 15 µA (Notes 1, 6)

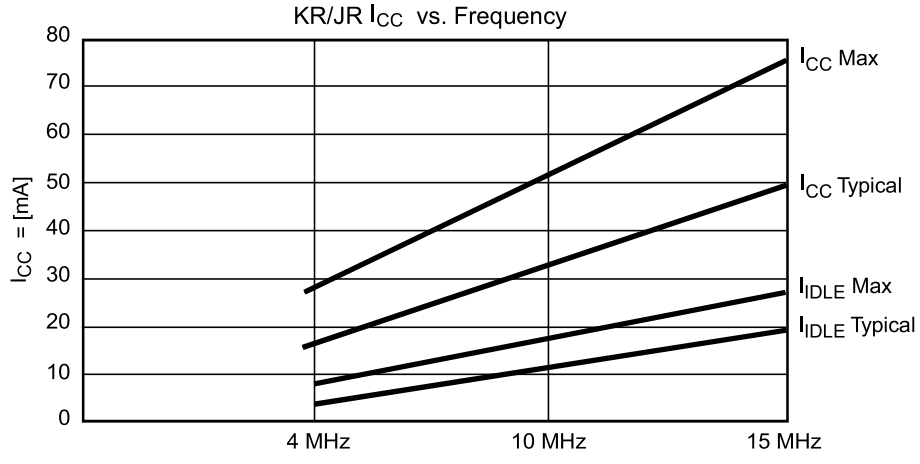
NOTES:
1. All BD (bidirectional) pins except P5.5/INST and P2.7/CLKOUT which are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port 2, Port3, Port4, Port5, and Port6.
2. Standard Input pins include XTAL1, EA#, RESET#, and Ports 1,2,3,4,5,6 when configured as inputs.
3. All bidirectional I/O pins when configured as outputs (push/pull).
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC}$ = 5.0 V.
5. V_{IH} max for Port0 is V_{REF} + 0.5 V.
6. Refer to “VOH2/IOH2 Specification” errata #1 in errata section of this datasheet.
7. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.
8. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).

Table 5. DC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Test Conditions
I_{OH2} (KR)	Output high current in RESET	–6 –15 –20		–35 –60 –70	µA	$V_{OH2} = V_{CC} – 1.0$ V $V_{OH2} = V_{CC} – 2.5$ V $V_{OH2} = V_{CC} – 4.0$ V
I_{OH2} (JV, JT, JR,CA)	Output High Current in RESET	–30 –75 –90		–120 –240 –280	µA	$V_{OH2} = V_{CC} – 1.0$ V $V_{OH2} = V_{CC} – 2.5$ V $V_{OH2} = V_{CC} – 4.0$ V
R_{RST}	Reset pullup resistor	6 K		65 K	Ω	
V_{OL3}	Output low voltage in reset (RESET pin only)			0.3 0.5 0.8	V	I_{OL3} = 4 mA (Note 7) I_{OL3} = 6 mA I_{OL3} = 10 mA
C_S	Pin Capacitance (any pin to V_{SS})			10	pF	F_{TEST} = 1.0 MHz
R_{WPU}	Weak pullup resistance (approx.)		150 K		Ω	(Note 4)

NOTES:
1. All BD (bidirectional) pins except P5.5/INST and P2.7/CLKOUT which are excluded due to their not being weakly pulled high in reset. BD pins include Port1, Port 2, Port3, Port4, Port5, and Port6.
2. Standard Input pins include XTAL1, EA#, RESET#, and Ports 1,2,3,4,5,6 when configured as inputs.
3. All bidirectional I/O pins when configured as outputs (push/pull).
4. Typicals are based on limited number of samples and are not guaranteed. The values listed are at room temperature and $V_{REF} = V_{CC} = 5.0$ V.
5. V_{IH} max for Port0 is $V_{REF} + 0.5$ V.
6. Refer to “VOH2/IOH2 Specification” errata #1 in errata section of this datasheet.
7. This specification is not tested in production and is based upon theoretical estimates and/or product characterization.
8. Violating these specifications in reset may cause the device to enter test modes (P5.4 and P2.6).

Figure 6. 87C196KR and JR I_{CC} vs. Frequency



Notes:
I_{CC} Max = 3.88 x Freq + 13.43
I_{IDLE} Max = 1.65 x Freq + 2.2

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Figure 7. JT I_{CC} vs. Frequency

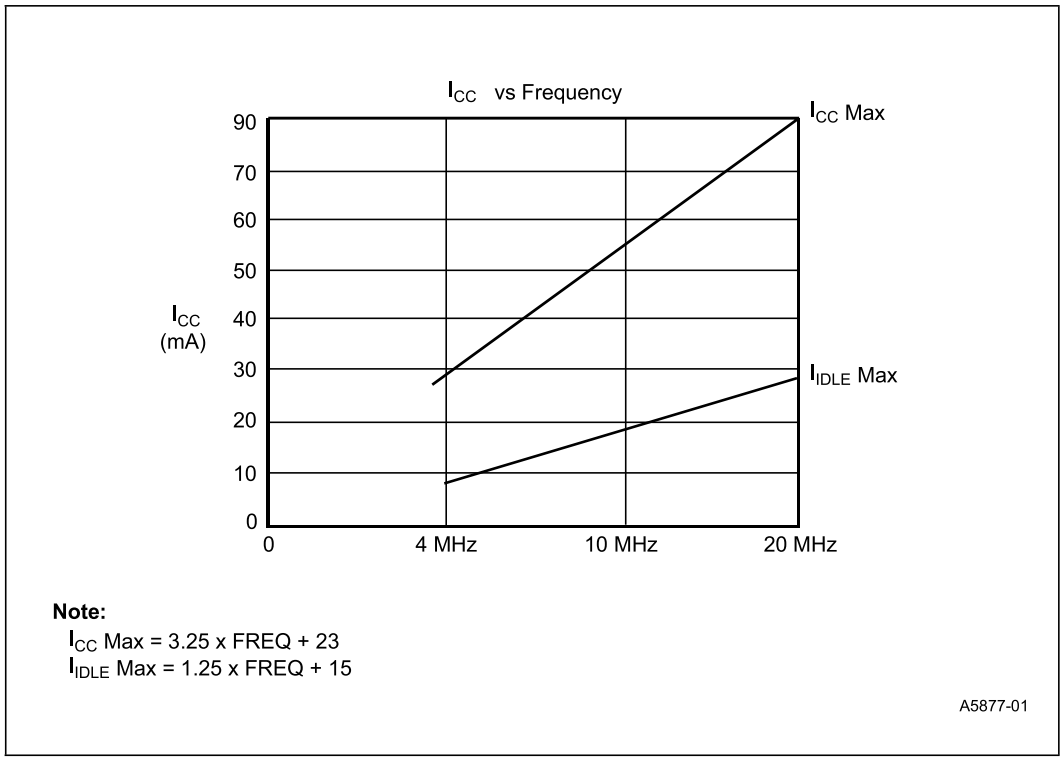
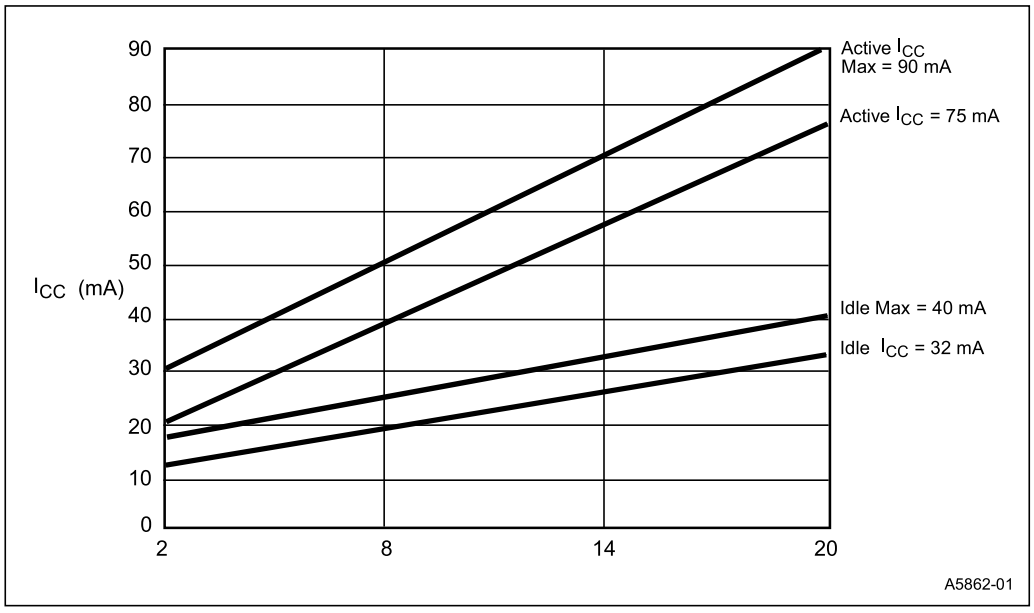


Figure 8. 87C196CA I_{CC} vs. Frequency



4.4 AC Characteristics

Table 6. AC Characteristics (Sheet 1 of 2)
(over specified operating conditions); Test conditions: capacitance load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

Symbol	Parameter	Min	Max	Units
The system must meet these specifications to work with the 87C196KR, JV, JT, JR, CA Microcontroller.				
T_{AVYV}	Address Valid to READY Setup		2 T_{OSC} – 75	ns
T_{LLYV}	ALE Low to READY Setup		T_{OSC} – 70	ns
T_{YLYH}	Non Ready Time	No Upper Limit		ns
T_{CLYX}	READY Hold after CLKOUT Low	0	T_{OSC} – 30	ns(1)
T_{LLYX}	READY Hold after ALE Low	T_{OSC} – 15	2 T_{OSC} – 40	ns(1)
T_{AVGV}	Address Valid to Buswidth Setup		2 T_{OSC} – 75	ns
T_{LLGV}	ALE Low to Buswidth Setup		T_{OSC} – 60	ns
T_{CLGX}	Buswidth Hold after CLKOUT Low	0		ns
T_{AVDV}	Address Valid to Input Data Valid		3 T_{OSC} – 55	ns
T_{RLDV}	RD# Active to Input Data Valid		T_{OSC} – 22	ns
T_{CLDV}	CLKOUT Low to Input Data Valid		T_{OSC} – 50	ns
T_{RHDZ}	End of RD# to Input Data Float		T_{OSC}	ns
T_{RXDX}	Data Hold after RD# Inactive	0		ns
The 87C196KR, JV, JT, JR, CA Microcontroller meets these specifications.				
F_{XTAL}	Oscillator Frequency	4	16	MHz(2)
T_{OSC}	Oscillator Period ($1/F_{XTAL}$)	62.5	250	ns
T_{XHCH}	XTAL1 High to CLKOUT High or Low	20	110	ns(3)
T_{OFD}	Clock Failure to Reset Pulled Low	4	40	µS(7)
T_{CLCL}	CLKOUT Period	2 T_{OSC}		ns
T_{CHCL}	CLKOUT High Period	T_{OSC} – 10	T_{OSC} + 15	ns
T_{CLLH}	CLKOUT Falling Edge to ALE Rising	–10 CA: –15	15 CA: 10	ns
T_{LLCH}	ALE/ADV# Falling Edge to CLKOUT Rising	–20	15	ns
T_{LHLH}	ALE/ADV# Cycle Time	4 T_{OSC}		ns
T_{LHLL}	ALE/ADV# High Period	T_{OSC} – 10	T_{OSC} + 10	ns
T_{AVLL}	Address Setup to ALE/ADV# Falling Edge	T_{OSC} – 15		ns
T_{LLAX}	Address Hold after ALE/ADV# Falling Edge	T_{OSC} – 40		ns

NOTES:
1. If max is exceeded, additional wait states will occur.
2. Testing performed at 4 MHz; however, the device is static by design and will typically operate below 1 Hz.
3. Typical specifications, not guaranteed.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.
6. T_{RLAZ} (max) = 5 ns by design.
7. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure.

Table 6. AC Characteristics (Sheet 2 of 2)
(over specified operating conditions); Test conditions: capacitance load on all pins = 100 pF, Rise and fall times = 10 ns, F_{OSC} = 16 MHz

Symbol	Parameter	Min	Max	Units
T_{LLRL}	ALE/ADV# Falling Edge to RD# Falling Edge	T_{OSC} – 30		ns
T_{RLCL}	RD# Low to CLKOUT Falling Edge	4	30	ns
T_{RLRH}	RD# Low Period	T_{OSC} – 5 CA: T_{OSC} – 10		ns
T_{RHLH}	RD# Rising Edge to ALE/ADV# Rising Edge	T_{OSC}	T_{OSC} + 25	ns(4)
T_{RLAZ}	RD# Low to Address Float		5	ns(6)
T_{LLWL}	ALE/ADV# Falling Edge to WR# Falling Edge	T_{OSC} – 10		ns
T_{CLWL}	CLKOUT Low to WR# Falling Edge	–5	25	ns
T_{QVWH}	Data Stable to WR# Rising Edge	T_{OSC} – 23		ns
T_{CHWH}	CLKOUT High to WR# Rising Edge	–10	15	ns
T_{WLWH}	WR# Low Period	T_{OSC} – 20		ns
T_{WHQX}	Data Hold after WR# Rising Edge	T_{OSC} – 25		ns
T_{WHLH}	WR# Rising Edge to ALE/ADV# Rising Edge	T_{OSC} – 10	T_{OSC} + 15	ns(4)
T_{WHBX}	BHE#, INST Hold after WR# Rising Edge	T_{OSC} – 10		ns
T_{WHAX}	AD[15:8] Hold after WR# Rising Edge	T_{OSC} – 30		ns(5)
T_{RHBX}	BHE#, INST Hold after RD# Rising Edge	T_{OSC} – 10		ns
T_{RHAX}	AD[15:8] Hold after RD# Rising Edge	T_{OSC} – 30		ns(5)

NOTES:
1. If max is exceeded, additional wait states will occur.
2. Testing performed at 4 MHz; however, the device is static by design and will typically operate below 1 Hz.
3. Typical specifications, not guaranteed.
4. Assuming back-to-back bus cycles.
5. 8-bit bus only.
6. T_{RLAZ} (max) = 5 ns by design.
7. T_{OFD} is the time for the oscillator fail detect circuit (OFD) to react to a clock failure.

Figure 9. System Bus Timing

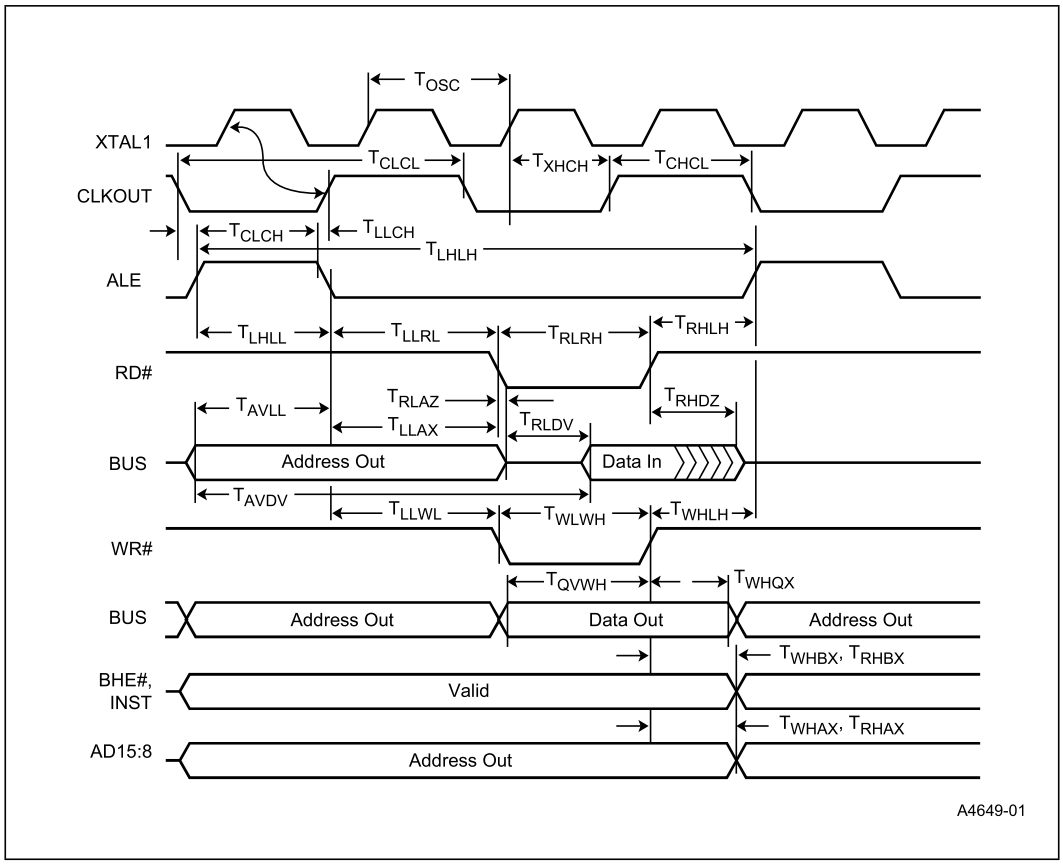


Figure 10. READY/Buswidth Timing

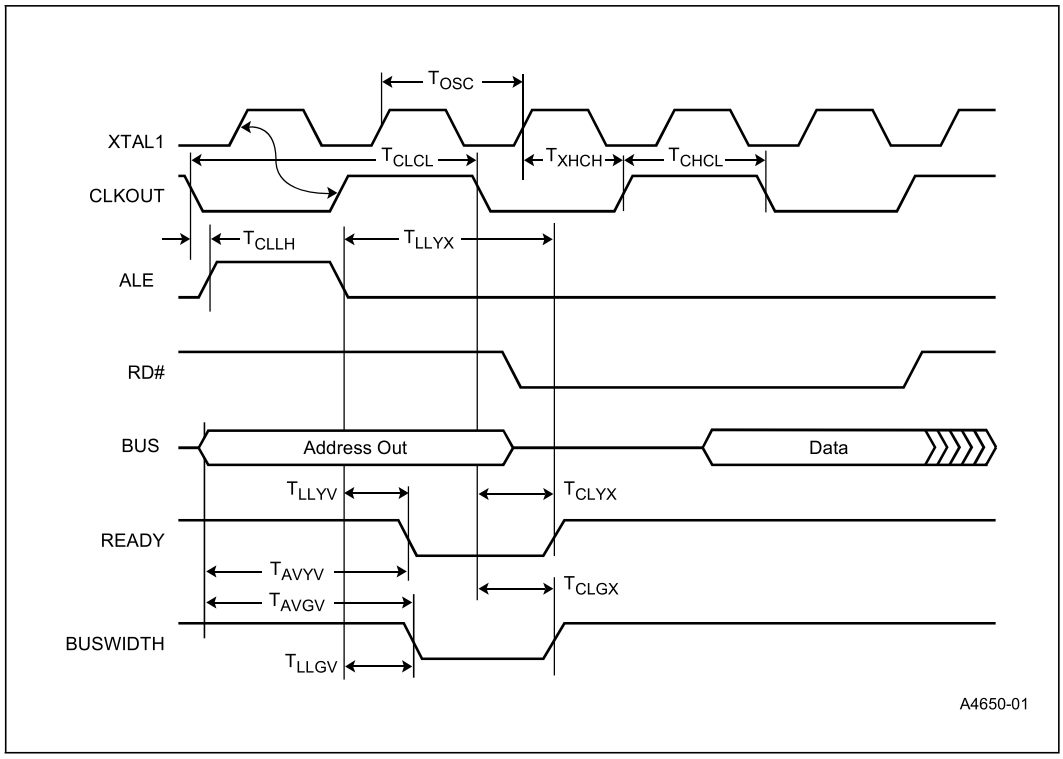


Table 7. External Clock Drive

Symbol	Parameter	Min	Max	Units
$1/T_{XLXL}$	Oscillator Frequency	4	16	MHz
T_{XLXL}	Oscillator Period (T_{OSC})	62.5	250	ns
T_{XHXX}	High Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXX}	Low Time	0.35 T_{OSC}	0.65 T_{OSC}	ns
T_{XLXH}	Rise Time		10	ns
T_{XHXL}	Fall Time		10	ns

Figure 11. External Clock Drive Waveforms

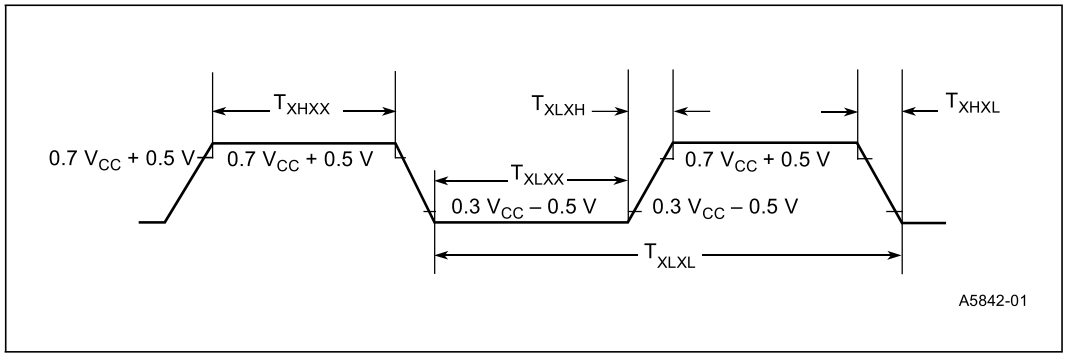
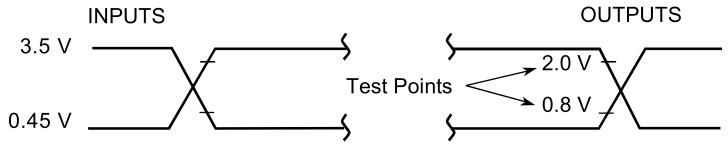


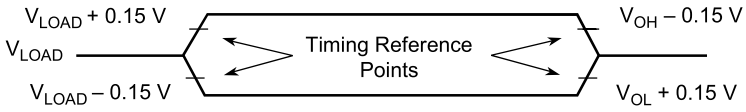
Figure 12. AC Testing Input, Output Waveforms



Note:
AC testing inputs are driven at 3.5 V for a logic " 1" and 0.45 V for a logic " 0" . Timing measurements are made at 2.0 V for a logic " 1" and 0.8 V for a logic " 0".

A4651-01

Figure 13. Float Waveforms



Note:
For timing purposes, a port pin is no longer floating when a 150 mV change from load voltage occurs and begins to float when a 150 mV change from the loading V_{OH}/V_{OL} level occurs with $I_{OL}/I_{OH} \leq 15$ mA.

A5844-01

Table 8. Thermal Characteristics

Device and Package	θ_{JA}	θ_{JC}
xx87C196KR (68-Lead PLCC)	41°C/W	14°C/W
xx87C196JV, JT, JR (52-Lead PLCC)	42°C/W	15°C/W
xx87C196CA (68-Lead PLCC)	36.5°C/W	10°C/W

NOTES:
1. θ_{JA} = Thermal resistance between junction and the surrounding environment (ambient). Measurements are taken 1 ft. away from case in air flow environment.
   θ_{JC} = Thermal resistance between junction and package surface (case).
2. All values of θ_{JA} and θ_{JC} may fluctuate depending on the environment (with or without airflow, and how much airflow) and device power dissipation at temperature of operation. Typical variations are ±2°C/W.
3. Values listed are at a maximum power dissipation of 0.50 W.
4. To address the fact that many of the package prefix variables have changed, all package prefix variables in the document are now indicated with an "x".

4.4.1 Explanation of AC Symbols

Each symbol is two pairs of letters prefixed by "t" for time. The characters in a pair indicate a signal and its condition, respectively. Symbols represent the time between the two signal/condition points.

Conditions	Signals	
H–High	A–Address	HA–HLDA#
L–Low	B–BHE#	L–ALE/ADV#
V–Valid	C–CLKOUT	R–RD#
X–No Longer Valid	D–DATA	W–WR#/WRH#/WRI#
Z–Floating	G–Buswidth	X–XTAL1
	H–HOLD#	Y–READY

4.4.2 EPROM Specifications

Table 9. AC EPROM Programming Characteristics

Operating Conditions: Load Capacitance = 150 pF; T_C = 25 °C ± 5 °C; V_{REF} = 5.0 V ± 0.5 V; V_{SS}, ANGND = 0 V; V_{PP} = 12.5 V ± 0.25 V; EA# = 12.5 V ± 0.25 V; F_{OSC} = 5.0 MHz

Symbol	Parameter	Min	Max	Units
T_{AVLL}	Address Setup Time	0		T_{OSC}
T_{LLAX}	Address Hold Time	100		T_{OSC}
T_{DVPL}	Data Setup Time	0		T_{OSC}
T_{PLDX}	Data Hold Time	400		T_{OSC}
T_{LLLH}	PALE# Pulse Width	50		T_{OSC}
T_{PLPH}	PROG# Pulse Width(3)	50		T_{OSC}
T_{LHPL}	PALE# High to PROG# Low	220		T_{OSC}
T_{PHLL}	PROG# High to Next PALE# Low	220		T_{OSC}
T_{PHDX}	Word Dump Hold Time		50	T_{OSC}
T_{PHPL}	PROG# High to Next PROG# Low	220		T_{OSC}
T_{PLDV}	PROG# Low to Word Dump Valid		50	T_{OSC}
T_{SHLL}	RESET# High to First PALE# Low	1100		T_{OSC}
T_{PHIL}	PROG# High to AINC# Low	0		T_{OSC}
T_{ILIH}	AINC# Pulse Width	240		T_{OSC}
T_{ILVH}	PVER Hold after AINC# Low	50		T_{OSC}
T_{ILPL}	AINC# Low to PROG# Low	170		T_{OSC}
T_{PHVL}	PROG# High to PVER# Valid		220	T_{OSC}

NOTES:
1. Run-time programming is done with F_{OSC} = 6.0 MHz to 10.0 MHz, V_{CC}, V_{PD}, V_{REF} = 5 V ± 0.5 V, TC = 25 °C ± 5 °C and V_{PP} = 12.5 V ± 0.25 V. For run-time programming over a full operating range, contact factory.
2. Programming specifications are not tested, but guaranteed by design.
3. This specification is for the word dump mode. For programming pulses, use 300 T_{OSC} + 100 µS.

Table 10. DC EPROM Programming Characteristics

Symbol	Parameter	Min	Max	Units
I_{PP}	V_{PP} Programming Supply Current		100 CA: 200	mA

NOTE: V_{PP} must be within 1 V of V_{CC} while V_{CC} < 4.5 V. V_{PP} must not have a low impedance path to ground or V_{SS} while V_{CC} > 4.5 V.

Figure 14. Slave Programming Mode Data Program Mode with Single Program Pulse

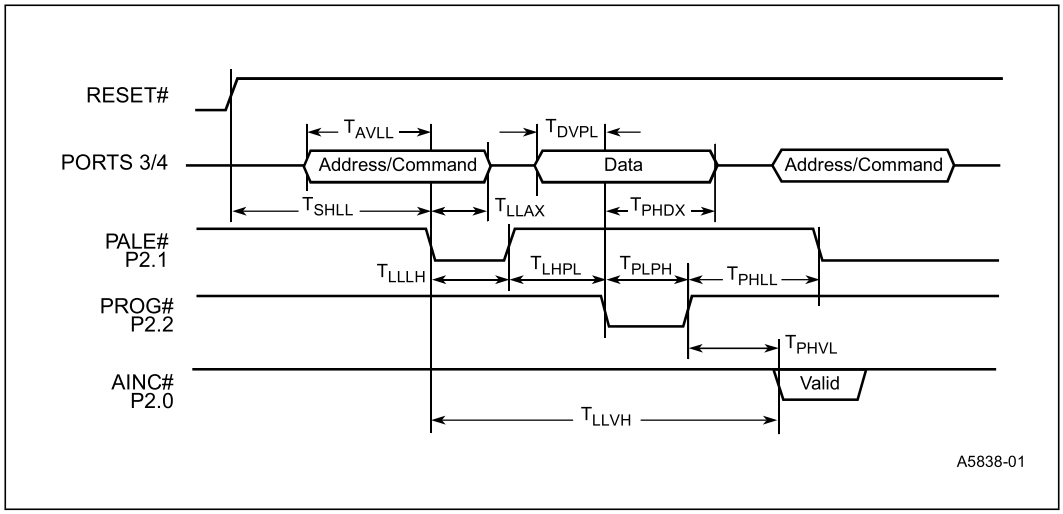


Figure 15. Slave Programming Mode in Word Dump or Data Verify Mode with Auto Increment

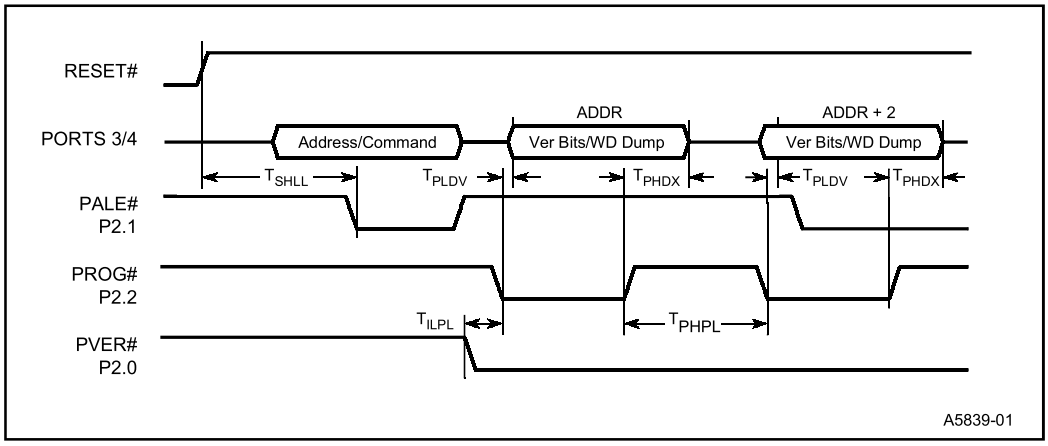
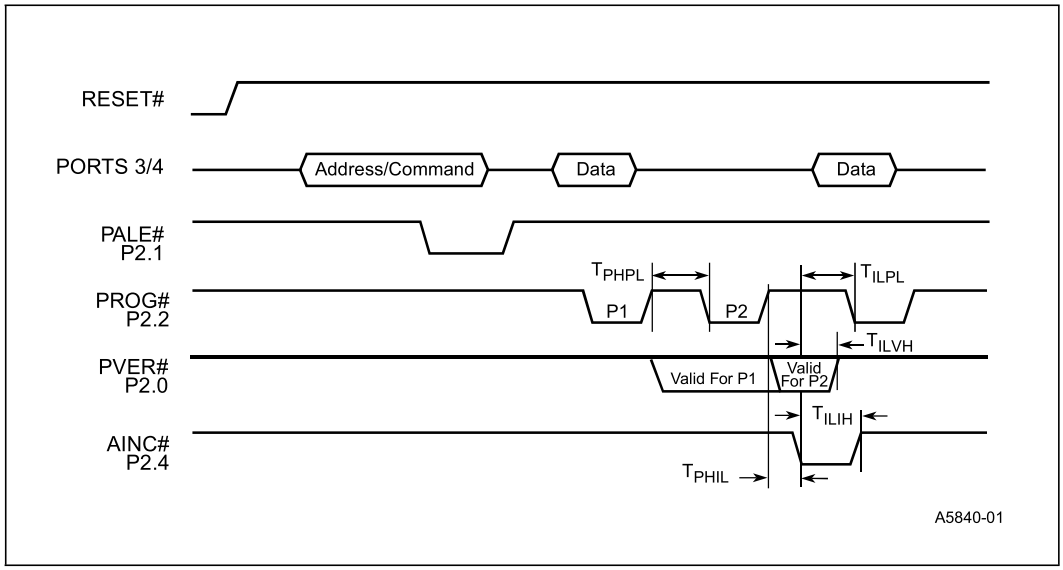


Figure 16. Slave Programming Mode Timing in Data Program Mode with Repeated PROG Pulse and Auto Increment



4.4.3 A to D Converter Specifications

The speed of the A/D converter in the 10-bit or 8-bit modes can be adjusted by setting the AD_TIME special function register to the appropriate value. The AD_TIME register only programs the speed at which the conversions are performed, not the speed at which it can convert correctly.

The converter is ratiometric, so absolute accuracy is dependent on the accuracy and stability of V_{REF}.

V_{REF} must not exceed V_{CC} by more than 0.5 V since it supplies both the resistor ladder and the digital portion of the converter and input port pins.

For testing purposes, after a conversion is started, the device is placed in the IDLE mode until the conversion is complete. Testing is performed at V_{REF} = 5.12 V and 16 MHz operating frequency.

There is an AD_TEST register that allows for conversion on ANGND and V_{REF} as well as zero offset adjustment. The absolute error listed is without doing any adjustments.

Table 11. A/D Operating Conditions

Symbol	Description	Min	Max	Units
T_A	Automotive Ambient Temperature	–40	+125	°C
V_{CC}	Digital Supply Voltage	4.50	5.50	V
V_{REF}	Analog Supply Voltage	4.50	5.50	V
T_{SAM}	Sample Time	2.0		µS
T_{CONV}	Conversion Time	16.5 CA: 15	19.5 CA: 18	µS
F_{OSC}	Oscillator Frequency	4	16	MHz

NOTES:
1. ANGND and V_{SS} should nominally be at the same potential.
2. V_{REF} must not exceed V_{CC} by more than +0.5 V.
3. Testing is performed at V_{REF} = 5.12 V.
4. The value of AD_TIME must be selected to meet these specifications.

Table 12. A/D Operating Parameter Values

Parameter	Typical(†,1)	Min	Max	Units††
Resolution		1024 10	1024 10	Level Bits
Absolute Error		0	–3 +3	LSBs
Full Scale Error	±2			LSBs
Zero Offset Error	±2			LSBs
Non-linearity			±3	LSBs
Differential Non-linearity		> –0.5	+0.5	LSBs
Channel-to-Channel Matching		0	±1	LSBs
Repeatability	±0.25	0		LSBs(1)
Temperature Coefficients: Offset Fullscale Differential Non-linearity	 0.009 0.009 0.009			LSB/C(1)
Off Isolation		–60		dB(1)(2)(3)
Feedthrough	–60			dB(1)(2)
V_{CC} Power Supply Rejection	–60			dB(1)(2)
Input Resistance		750	1.2 K	Ω(1)
DC Input Leakage		0	±1 JT, JV = ±2 CA = ±3	µA

NOTES:

† These values are expected for most parts at 25°C but are not tested or guaranteed.

†† An “LSB,” as used here, has a value of approximately 5 mV. (See Automotive Handbook for A/D glossary of terms.)

1. These values are not tested in production and are based on theoretical estimates and/or laboratory test.
2. DC to 100 KHz.
3. Multiplexer break-before-make guaranteed.

Table 13. HOLD#/HLDA# Timings

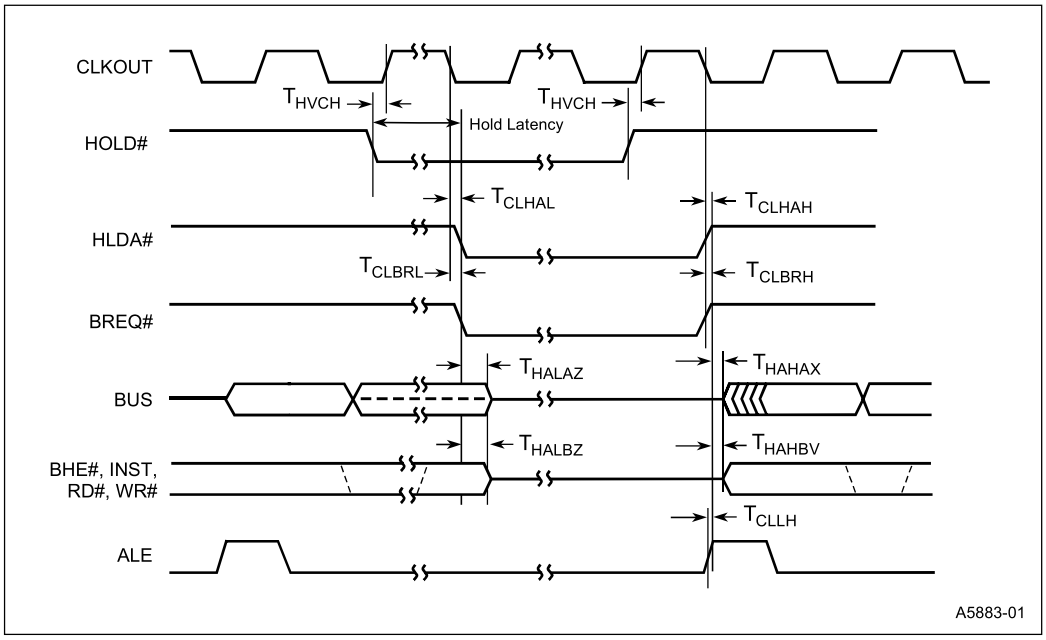
Symbol	Description	Min	Max	Units	Notes
T_{HVCH}	HOLD Setup	65		ns	Note 1
T_{CLHAL}	CLKOUT Low to HLDA Low	–15	15	ns	
T_{CLBRL}	CLKOUT Low to BREQ Low	–15	15	ns	
T_{AZHAL}	HLDA# Low to Address Float		25	ns	
T_{BZHAL}	HLDA# Low to BHE#, INST, RD#, WR# Weakly Driven		25	ns	
T_{CLHAH}	CLKOUT Low to HLDA High	–15	15	ns	
T_{CLBRH}	CLKOUT Low to BREQ High	–15	15	ns	
T_{HAHAX}	HLDA High to Address Valid	–15		ns	
T_{HAHBV}	HLDA High to BHE, INST, RD, WR Valid	–10		ns	
T_{CLLH}	CLKOUT Low to ALE High	–10	15	ns	

NOTE:
1. To guarantee recognition at next clock.

Table 14. DC Specifications in HOLD

Parameter	Min	Max	Units
Weak Pullups on ADV#, RD#, WR#, WRL#, BHE#	50 K	250 K	V_{CC} = 5.5 V, V_{IN} = 0.45 V
Weak Pulldowns on ALE, INST	10 K	50 K	V_{CC} = 5.5 V, V_{IN} = 2.4 V

Figure 17. HOLD Timings



4.4.4 AC Characteristics—Slave Port

Figure 18. Slave Port Waveform (SLPL = 0)

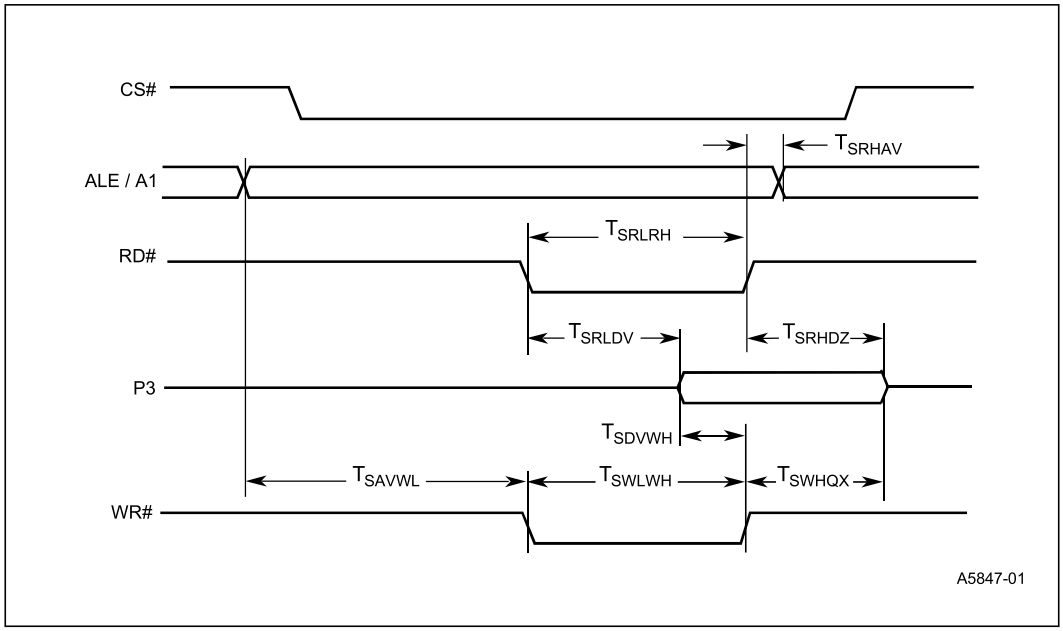


Table 15. Slave Port Timing–(SLPL = 0) (See notes 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SAVWL}	Address Valid to WR# Low	50		ns
T_{SRHAV}	RD# High to Address Valid	60		ns
T_{SRLRH}	RD# Low Period	T_{OSC}		ns
T_{SWLWH}	WR# Low Period	T_{OSC}		ns
T_{SRLDV}	RD# Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to WR# High	20		ns
T_{SWHQX}	WR# High to Data Invalid	30		ns
T_{SRHDZ}	RD# High to Data Float	15		ns

NOTES:
1. Test conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns, Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

Figure 19. Slave Port Waveform (SLPL = 1)

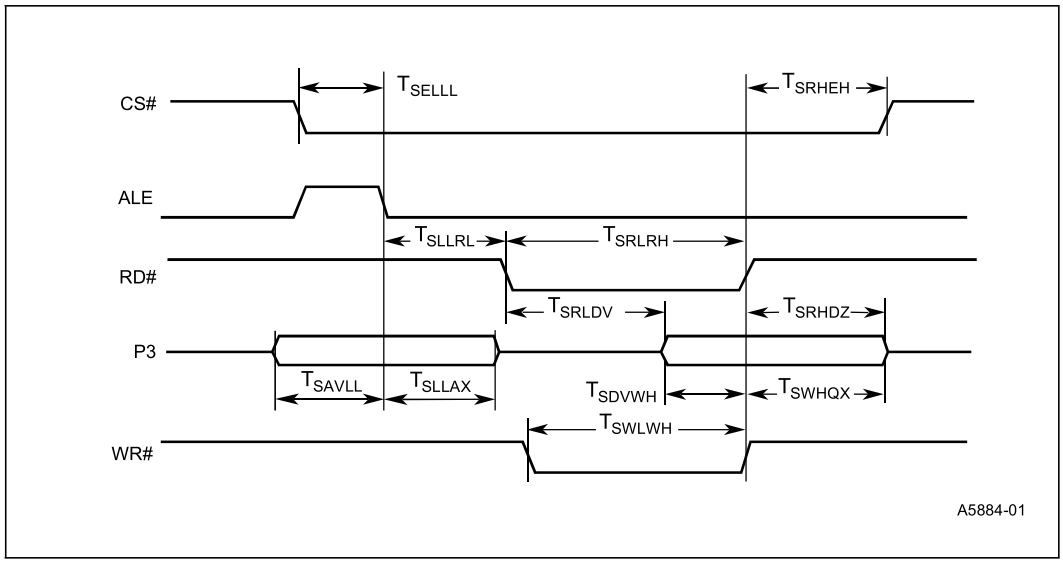


Table 16. Slave Port Timing–(SLPL = 1) (See notes 1, 2, 3)

Symbol	Parameter	Min	Max	Units
T_{SELLL}	CS# Low to ALE Low	20		ns
T_{SRHEH}	RD# or WR# High to CS# High	60		ns
T_{SLLRL}	ALE Low to RD# Low	T_{OSC}		ns
T_{SRLRH}	RD# Low Period	T_{OSC}		ns
T_{SWLWH}	WR# Low Period	T_{OSC}		ns
T_{SAVLL}	Address Valid to ALE Low	20		ns
T_{SLLAX}	ALE Low to Address Invalid	20		ns
T_{SRLDV}	RD# Low to Output Data Valid		60	ns
T_{SDVWH}	Input Data Setup to WR# High	20		ns
T_{SWHQX}	WR# High to Data Invalid	30		ns
T_{SRHDZ}	RD# High to Data Float	15		ns

NOTES:
1. Test conditions: F_{OSC} = 16 MHz, T_{OSC} = 60 ns, Rise/Fall Time = 10 ns. Capacitive Pin Load = 100 pF.
2. These values are not tested in production, and are based upon theoretical estimates and/or laboratory tests.
3. Specifications above are advanced information and are subject to change.

4.4.5 AC Characteristics—Serial Port— Shift Register Mode

Table 17. Serial Port Timing—Shift Register Mode

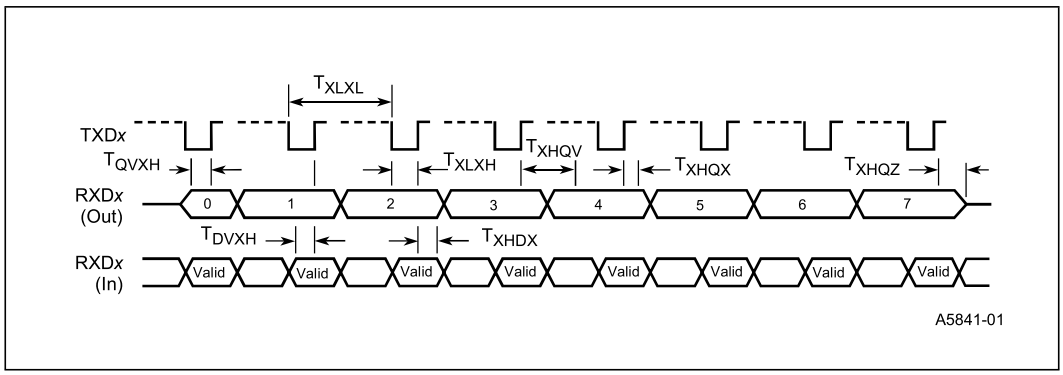
Test Conditions: T_A = –40°C to +125°C; V_{CC} = 5.0 V ± 10%; V_{SS} = 0.0 V; Load Capacitance = 100 pF

Symbol	Parameter	Min	Max	Units
T_{XLXL}	Serial Port Clock Period	8 T_{OSC}		ns
T_{XLXH}	Serial Port Clock Falling Edge to Rising Edge	4 T_{OSC} – 50	4 T_{OSC} + 50	ns
T_{QVXH}	Output Data Setup to Clock Rising Edge	3 T_{OSC}		ns
T_{XHQX}	Output Data Hold after Clock Rising Edge	2 T_{OSC} – 50		ns
T_{XHQV}	Next Output Data Valid after Clock Rising Edge		2 T_{OSC} + 50	ns
T_{DVXH}	Input Data Setup to Clock Rising Edge	2 T_{OSC} + 200		ns
T_{XHDX}(1)	Input Data Hold after Clock Rising Edge	0		ns
T_{XHQZ}(1)	Last Clock Rising to Output Float		5 T_{OSC}	ns

NOTES:
1. Parameter not tested.

4.4.6 Waveform—Serial Port—Shift Register Mode 0

Figure 20. Serial Port Waveform—Shift Register Mode



5.0 52-Lead Devices

Intel offers 52-lead versions of the 87C196KR device: the 87C196JV, JT, and JR devices. The first samples and production units use the 87C196KR die and bond it out in a 52-lead package.

It is important to point out some functionality differences because of future devices or to remain software consistent with the 68-lead device. Because of the absence of pins on the 52-lead device some functions are not supported.

52-Lead Unsupported Functions:

- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT Pin Support
- HLD#/HLDA# Functionality
- External Clocking/Direction of Timer1
- WRH# or BHE Functions
- Dynamic Buswidth
- Dynamic Wait State Control

The following is a list of recommended practices when using the 52-lead device:

1. **External Memory**. Use an 8-bit bus mode only. There is neither a WRH# or BUSWIDTH pin. The bus cannot dynamically switch from 8- to 16-bit or vice versa. Set the CCB bytes to an 8-bit only mode, using WR# function only.
2. **Wait State Control**. Use the CCB bytes to configure the maximum number of wait states. If the READY pin is selected to be a system function, the device will lockup waiting for READY. If the READY pin is configured as LSIO (default after RESET#), the internal logic will receive a logic “0” level and insert the CCB defined number of wait states in the bus cycle. DON'T USE IRC = “111”.
3. **NMI Support**. The NMI is not bonded out. Make the NMI vector at location 203Eh vector to a Return instruction. This is for glitch safety protection only.
4. **Auto-Programming Mode**. The 52-lead device will ONLY support the 16-bit zero wait state bus during auto-programming.
5. **EPA4 through EPA7**. Since the JR, JT, and JV devices use the KR silicon, these functions are in the device, just not bonded out. A programmer can use these as compare only channels or for other functions like software timer, start an A/D conversion, or reset timers.
6. **Slave Port Support**. The Slave port cannot be easily used on 52-lead devices due to 5.4/SLPINT and P5.1/SLPCS not being bonded-out.

7. **Port Functions**. Some port pins have been removed. P5.7, P5.6, P5.5, P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The PxREG, PxSSEL, and PxIO registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

   Additionally, these port pins should be setup internally by software as follows:

   a. Written to PxREG as “1” or “0”.

   b. Configured as Push/Pull, PxIO as “0”.

   c. Configured as LSIO.

Warning: This configuration will effectively strap the pin either high or low. DO NOT Configure as Open Drain output “1”, or as an Input pin. This device is CMOS.

6.0 Design Considerations

6.1 87C196KR, JV, JT, JR, and CA Design Considerations

1. EPA Timer RESET/Write Conflict

   If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

2. Valid Time Matches

   The timer must increment/decrement to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

3. P6 PIN.4-.7 Not Updated Immediately

   Values written to P6 REG are temporarily held in a buffer. If P6 MODE is cleared, the buffer is loaded into P6 REG.x. If P6 MODE is set, the value stays in the buffer and is loaded into P6 REG.x when P6 MODE.x is cleared. Since reading P6 REG returns the current value in P6. REG and not the buffer, changes to P6 REG cannot be read until/ unless P6 MODE.x is cleared.

4. Write Cycle during Reset

   If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

5. Indirect Shift Instruction

   The upper 3 bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 x *n*, where *n* = 1, 3, 5, or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

6. P2.7 (CLKOUT)

   P2.7 (CLKOUT) does not operate in open drain mode.

7. CLKOUT

   The CLKOUT signal is active on P2.7 during RESET for the KR, JV, JT, JR and CA devices.

8. EPA Overruns

   EPA “lock-up” can occur if overruns are not handled correctly, refer to Intel Techbit #DB0459 “Understanding EPA Capture Overruns”, dated 12-9-93. Applies to EPA channels with interrupts and overruns enabled (ON/RT bit in EPA_CONTROL register set to “1”).

9. Indirect Addressing with Auto-Increment

   For the special case of a pointer pointing to itself using auto-increment, an incorrect access of the incremented pointer address will occur instead of an access to the original pointer address. All other indirect auto-increment accesses will note be affected. Please refer to Techbit #MC0593.

   Incorrect sequence:

```
ld ax,#ax       ;   Results in ax being incremented by 1 and the contents of the address
ldb bx,[ax]+    ;   pointed to by ax+1 to be loaded into bx.
```

   Correct sequence:

```
ld ax,#bx       ;   where ax ≠ bx. Results in the contents of the address pointed to by ax
ldb cx,[ax]+    ;   to be loaded into bx and ax incremented by 1.
```

10. JV Additional Register RAM

    The 8XC196JV has a total of 1.5 Kbytes of register RAM. The RAM is located in two memory ranges: 0000h – 03FFh and 1C00h – 1DFFh.

6.2 87C196JR C-step to JR D-step – or – JV/JT A-step Design Considerations

This section documents differences between the 87C197JV A-step (JV-A)/87C196JT A-step (JT-A)/87C196JR D-step (JR-D) and the 87C196JR C-step/(JR-C). For a list of design considerations between 68-lead and 52-lead devices, please refer to the 52-lead Device Design Considerations section of this datasheet. Since the 87C196JV and JT are simply memory scalars of the 87C196JR, the term ``JR'' in this section will refer to JV, JT, and JR versions of the device unless otherwise noted.

The JR-C is simply a 87C196KR C-step (KR-C) device packaged within a 52-lead package. This reduction in pin count necessitated not bonding-out certain pins of the KR-C device. The fact that these “removed pins” were still present on the device but not available to the outside world allowed the programmer to take advantage of some of the 68-lead KR features.

The JR-D is a fully-optimized 52-lead device based on the 87C196KR C-step device. The KR-C design data base was used to assure that the JR-D would be fully compatible with the KR-C, JR-C and other Kx family members. The main differences between the JR-D and the JR-C is that several of the unused (not bonded-out) functions on the JR-C were removed altogether on the JR-D.

Following is a list of differences between the JR-C and the JR-D:

1. Port3 Push-Pull Operation

   It was discovered on JR-C that if Port3 is selected for push-pull operation (P34_DRV register) during low speed I/O (LSIO), the port was driving data when the system bus

was attempting to input data. It is rather unlikely that this errata would affect an application because the application would have to use Port3 for both LSIO and as an external addr/data bus. Nonetheless, this errata was corrected on the JR-D.

2. V_{OH2} Strengthened

   The DC Characteristics section of the Automotive KR datasheet contains a parameter, V_{OH2} (Output High Voltage in RESET (BD ports)), which is specified at V_{CC} – 1 V min at
   I_{OH2} = –15 µA. This specification indicates the strength of the internal weak pull-ups that are active during and after reset. These weak pull-ups stay active until the user writes to PxMODE (previously known as PxSSEL) and configures the port pin as desired.

   These pull-ups do not meet this V_{OH2} spec on the JR-C. The weak pull-ups on specified JR-D ports have been enhanced to meet the published specification of I_{OH2} = –15 µA.

3. ONCE Mode

   ONCE mode is entered by holding a single pin low on the rising edge of RESET#. On the KR, this pin is P5.4/SLPINT. The JR-C does not support ONCE mode since P5.4/SLPINT (ONCE mode entry pin) is not bonded-out on these devices. To provide ONCE mode on the JR-D, the ONCE mode entry function was moved from P5.4/SLPINT to P2.6/HLDA. This will allow the JR-D to enter ONCE mode using P2.6 instead of removed pin P5.4.

4. Port0

   On the JR-C, P0.0 and P0.1 are not bonded out. However, these inputs are present in the device and reading them will provide an indeterminate result.

   On the JR-D, the analog inputs for these two channels at the multiplexer are tied to V_{REF}. Therefore, initiating an analog conversion on ACH0 or ACH1 will result in a value equal to full scale (3FFh). On the JR-D, the digital inputs for these two channels are tied to ground, therefore reading P0.0 or P0.1 will result in a digital ``0''.

5. Port1

   On the JR-C, P1.4, P1.5, P1.6 and P1.7 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with D-step and future devices, it is recommended that the corresponding bits associated with the removed pins NOT be used to conditionally branch in software. These bits should be treated as reserved.

   On the JR-D, unused port logic for these four port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been ``hard-wired'' to provide the following results when read:

Register Bits		When Read
P1_PIN.x	(x = 4,5,6,7)	1
P1_REG.x	(x = 4,5,6,7)	1
P1_DIR.x	(x = 4,5,6,7)	1
P1_MODE.x	(x = 4,5,6,7)	0

NOTE: Writing to these bits will have no effect.

6. Port2

On the JR-C, P2.3 and P2.5 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with D-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

On the JR-D, unused port logic for these two port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been “hardwired” to provide the following results when read:

Register Bits		When Read
P2_PIN.x	(x = 3,5)	1
P2_REG.x	(x = 3,5)	1
P2_DIR.x	(x = 3,5)	1
P2_MODE.x	(x = 3,5)	0

NOTE: Writing to these bits will have no effect.

7. Port5

   On the JR-C, P5.1, P5.4, P5.5, P5.6 and P5.7 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with D-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

   On the JR-D, unused port logic for these five port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been “hardwired” to provide the following results when read:

Register Bits		When Read
P5_PIN.x	(x = 1,4,5,6,7)	1
P5_REG.x	(x = 1,4,5,6,7)	1
P5_DIR.x	(x = 1,4,5,6,7)	1
P5_MODE.x	(x = 1,4,6)	0
P5_MODE.x	(x = 5)(EA# = 0)	1
P5_MODE.x	(x = 5)(EA# = 1)	0
P5_MODE.x	(x = 7)	1

NOTE: Writing to these bits will have no effect.

8. Port6

   On the JR-C, P6.2 and P6.3 are not bonded out but are present internally on the device. This allows the programmer to write to the port registers and clear, set or read the pin even though it is not available to the outside world. However, to maintain compatibility with D-step and future devices, it is recommended that the corresponding bits associated with the removed pins not be used to conditionally branch in software. These bits should be treated as reserved.

On the JR-D, unused port logic for these two port pins has been removed from the device and is not available to the programmer. Corresponding bits in the port registers have been “hardwired” to provide the following results when read:

Register Bits		When Read
P6_PIN.x	(x = 2,3)	1
P6_REG.x	(x = 2,3)	1
P6_DIR.x	(x = 2,3)	1
P6_MODE.x	(x = 2,3)	0

NOTE: Writing to these bits will have no effect.

9. EPA Channels 4 through 7

   The JR C-step device is simply a 68-lead KR-C device packaged in a 52-lead package. The reduced pin-out is achieved by not bonding-out the unsupported pins. EPA4–EPA7 are among these pins that are not bonded-out. The fact that EPA4–EPA7 are still present allows the programmer to use these channels as software timers, to start A/D conversions, reset timers, etc. All of the port pin logic is still present and it is possible to use the EPA to toggle these pins internally. Please refer to the 52-Lead Device section in this datasheet for further information.

   On the JR D-step, the EPA4–EPA7 logic has NOT been removed from the device. This allows the programmer to still use these channels (as on the C-step) for software timers, etc. The only difference is that the associated port pin logic has been removed and does not exist internally. To maintain C-step to D-step compatibility, programmers should make sure that their software does not rely upon the removed pins.

6.2.1 87C196CA Design Considerations

The 87C196CA device is a memory scalar of the 87C196KR device with integrated CAN 2.0. The CA is designed for strict functional and electrical compatibility to the Kx family as well as integration of on-chip networking capability. The 87C196CA has fewer peripheral functions than the 196KR, due in part to the integration of the CAN peripheral. Following are the functionality differences between the 196KR and 196CA devices.

196KR Features Unsupported on the 196CA:

- Analog Channels 0 and 1
- INST Pin Functionality
- SLPINT and SLPCS Pin Support
- HLD/HLDA Functionality
- External Clocking/Direction of Timer1
- Quadrature Clocking Timer 1
- Dynamic Buswidth
- EPA Capture Channels 4–7

1. External Memory

   Removal of the Buswidth pin means the bus cannot dynamically switch from 8- to 16-bit bus mode or vice versa. The programmer must define the bus mode by setting the associated bits in the CCB.

2. Auto-Programming Mode

   The 87C196CA device will ONLY support the 16-bit zero wait state bus during auto-programming.

3. EPA4 through EPA7

Since the CA device is based on the KR design, these functions are in the device, however there are no associated pins. A programmer can use these as compare only channels or for other functions like software timer, start an A/D conversion, or reset timers.

4. Slave Port Support

   The Slave port can not be used on the 196CA due to a function change for P5.4/ SLPINT and P5.1/SLPCS not being bonded-out.

5. Port Functions

   Some port pins have been removed. P5.1, P6.2, P6.3, P1.4 through P1.7, P2.3, P2.5, P0.0 and P0.1. The PxREG, PxSSEL, and PxIO registers can still be updated and read. The programmer should not use the corresponding bits associated with the removed port pins to conditionally branch in software. Treat these bits as RESERVED.

   Additionally, these port pins should be setup internally by software as follows:

   a. Written to PxREG as ``1'' or ``0''.

   b. Configured as Push/Pull, PxIO as ``0''.

   c. Configured as LSIO.

      This configuration will effectively strap the pin either high or low. DO NOT Configure as Open Drain output ``1'', or as an Input pin. This device is CMOS.

6. EPA Timer RESET/Write Conflict

   If the user writes to the EPA timer at the same time that the timer is reset, it is indeterminate which will take precedence. Users should not write to a timer if using EPA signals to reset it.

7. Valid Time Matches

   The timer must increase/decrease to the compare value for a match to occur. A match does not occur if the timer is loaded with a value equal to an EPA compare value. Matches also do not occur if a timer is reset and 0 is the EPA compare value.

8. Write Cycle during Reset

   If RESET occurs during a write cycle, the contents of the external memory device may be corrupted.

9. Indirect Shift Instruction

   The upper 3 bits of the byte register holding the shift count are not masked completely. If the shift count register has the value 32 c n, where n e 1, 3, 5, or 7, the operand will be shifted 32 times. This should have resulted in no shift taking place.

10. P2.7 (CLKOUT)

    P2.7 (CLKOUT) does not operate in open drain mode.

7.0 Revision History

Revision	Date	Description
008	08/04	To address the fact that many of the package prefix variables have changed, all package prefix variables in this document are now indicated with an "x".
007	05/98	Removed the 87C196KQ and 87C196JQ products and related information from datasheet. Added 87C196CA product and related information to datasheet.
006	11/95	The 87C196JV datasheet status has been moved from “Product Preview” to that of “no marking. A ”by design” note was added to the T_{RLAZ} specification. In the Design Considerations section, the #7.CLKOUT design consideration was corrected. Only the two most current revision histories of this datasheet were retained in the datasheet revision history section.