



K30 Sub-Family Data Sheet

Supports the following:

MK30DN512ZVLK10,
MK30DN512ZVMB10

Features

- Operating Characteristics
 - Voltage range: 1.71 to 3.6 V
 - Flash write voltage range: 1.71 to 3.6 V
 - Temperature range (ambient): -40 to 105°C
- Performance
 - Up to 100 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz
- Memories and memory interfaces
 - Up to 512 KB program flash memory on non-FlexMemory devices
 - Up to 128 KB RAM
 - Serial programming interface (EzPort)
- Clocks
 - 3 to 32 MHz crystal oscillator
 - 32 kHz crystal oscillator
 - Multi-purpose clock generator
- System peripherals
 - Multiple low-power modes to provide power optimization based on application requirements
 - Memory protection unit with multi-master protection
 - 16-channel DMA controller, supporting up to 63 request sources
 - External watchdog monitor
 - Software watchdog
 - Low-leakage wakeup unit
- Security and integrity modules
 - Hardware CRC module to support fast cyclic redundancy checks
 - 128-bit unique identification (ID) number per chip

K30P81M100SF2



- Human-machine interface
 - Segment LCD controller supporting up to 40 frontplanes and 8 backplanes, or 44 frontplanes and 4 backplanes, depending on the package size
 - Low-power hardware touch sensor interface (TSI)
 - General-purpose input/output
- Analog modules
 - Two 16-bit SAR ADCs
 - Programmable gain amplifier (PGA) (up to x64) integrated into each ADC
 - 12-bit DAC
 - Three analog comparators (CMP) containing a 6-bit DAC and programmable reference input
 - Voltage reference
- Timers
 - Programmable delay block
 - Eight-channel motor control/general purpose/PWM timer
 - Two 2-channel quadrature decoder/general purpose timers
 - Periodic interrupt timers
 - 16-bit low-power timer
 - Carrier modulator transmitter
 - Real-time clock
- Communication interfaces
 - Controller Area Network (CAN) module
 - Two SPI modules
 - Two I2C modules
 - Four UART modules
 - Secure Digital host controller (SDHC)
 - I2S module

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

Table of Contents

1 Ordering parts.....	3	5.4.2 Thermal attributes.....	21
1.1 Determining valid orderable parts.....	3	6 Peripheral operating requirements and behaviors.....	22
2 Part identification.....	3	6.1 Core modules.....	22
2.1 Description.....	3	6.1.1 Debug trace timing specifications.....	22
2.2 Format.....	3	6.1.2 JTAG electricals.....	23
2.3 Fields.....	3	6.2 System modules.....	26
2.4 Example.....	4	6.3 Clock modules.....	26
3 Terminology and guidelines.....	4	6.3.1 MCG specifications.....	26
3.1 Definition: Operating requirement.....	4	6.3.2 Oscillator electrical specifications.....	28
3.2 Definition: Operating behavior.....	5	6.3.3 32 kHz Oscillator Electrical Characteristics.....	30
3.3 Definition: Attribute.....	5	6.4 Memories and memory interfaces.....	31
3.4 Definition: Rating.....	6	6.4.1 Flash electrical specifications.....	31
3.5 Result of exceeding a rating.....	6	6.4.2 EzPort Switching Specifications.....	33
3.6 Relationship between ratings and operating requirements.....	6	6.5 Security and integrity modules.....	34
3.7 Guidelines for ratings and operating requirements.....	7	6.6 Analog.....	34
3.8 Definition: Typical value.....	7	6.6.1 ADC electrical specifications.....	34
3.9 Typical value conditions.....	8	6.6.2 CMP and 6-bit DAC electrical specifications.....	41
4 Ratings.....	9	6.6.3 12-bit DAC electrical characteristics.....	44
4.1 Thermal handling ratings.....	9	6.6.4 Voltage reference electrical specifications.....	47
4.2 Moisture handling ratings.....	9	6.7 Timers.....	48
4.3 ESD handling ratings.....	9	6.8 Communication interfaces.....	48
4.4 Voltage and current operating ratings.....	9	6.8.1 CAN switching specifications.....	48
5 General.....	10	6.8.2 DSPI switching specifications (limited voltage range).....	49
5.1 AC electrical characteristics.....	10	6.8.3 DSPI switching specifications (full voltage range).....	50
5.2 Nonswitching electrical specifications.....	10	6.8.4 Inter-Integrated Circuit Interface (I2C) timing.....	52
5.2.1 Voltage and current operating requirements.....	10	6.8.5 UART switching specifications.....	53
5.2.2 LVD and POR operating requirements.....	11	6.8.6 SDHC specifications.....	53
5.2.3 Voltage and current operating behaviors.....	12	6.8.7 I2S switching specifications.....	54
5.2.4 Power mode transition operating behaviors.....	14	6.9 Human-machine interfaces (HMI).....	57
5.2.5 Power consumption operating behaviors.....	15	6.9.1 TSI electrical specifications.....	57
5.2.6 EMC radiated emissions operating behaviors.....	18	6.9.2 LCD electrical characteristics.....	58
5.2.7 Designing with radiated emissions in mind.....	19	7 Dimensions.....	59
5.2.8 Capacitance attributes.....	19	7.1 Obtaining package dimensions.....	59
5.3 Switching specifications.....	19	8 Pinout.....	59
5.3.1 Device clock specifications.....	19	8.1 K30 Signal Multiplexing and Pin Assignments.....	59
5.3.2 General switching specifications.....	19	8.2 K30 Pinouts.....	64
5.4 Thermal specifications.....	20	9 Revision History.....	66
5.4.1 Thermal operating requirements.....	20		

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK30 and MK30 .

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	- M = Fully qualified, general market flow - P = Prequalification
K##	Kinetis family	K30
A	Key attribute	- D = Cortex-M4 w/ DSP - F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	- N = Program flash only - X = Program flash and FlexMemory

Table continues on the next page...

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB • 512 = 512 KB • 1M0 = 1 MB • 2M0 = 2 MB
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = -40 to 105 • C = -40 to 85
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm) • LK = 80 LQFP (12 mm x 12 mm) • LL = 100 LQFP (14 mm x 14 mm) • MC = 121 MAPBGA (8 mm x 8 mm) • LQ = 144 LQFP (20 mm x 20 mm) • MD = 144 MAPBGA (13 mm x 13 mm) • MJ = 256 MAPBGA (17 mm x 17 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz • 7 = 72 MHz • 10 = 100 MHz • 12 = 120 MHz • 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK30DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

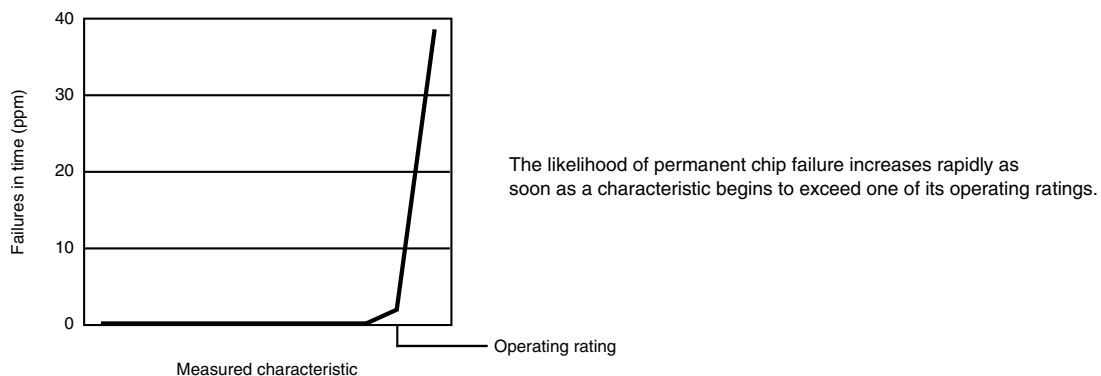
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

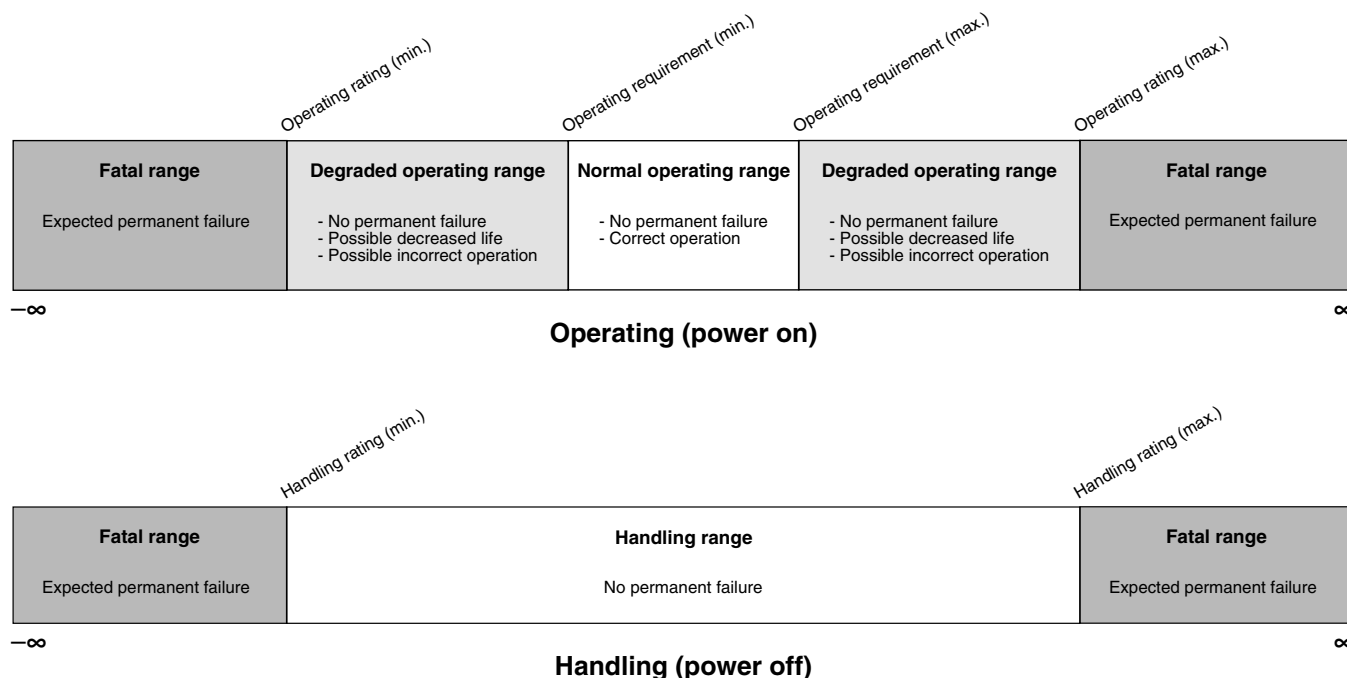
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	−0.3	1.2	V

3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

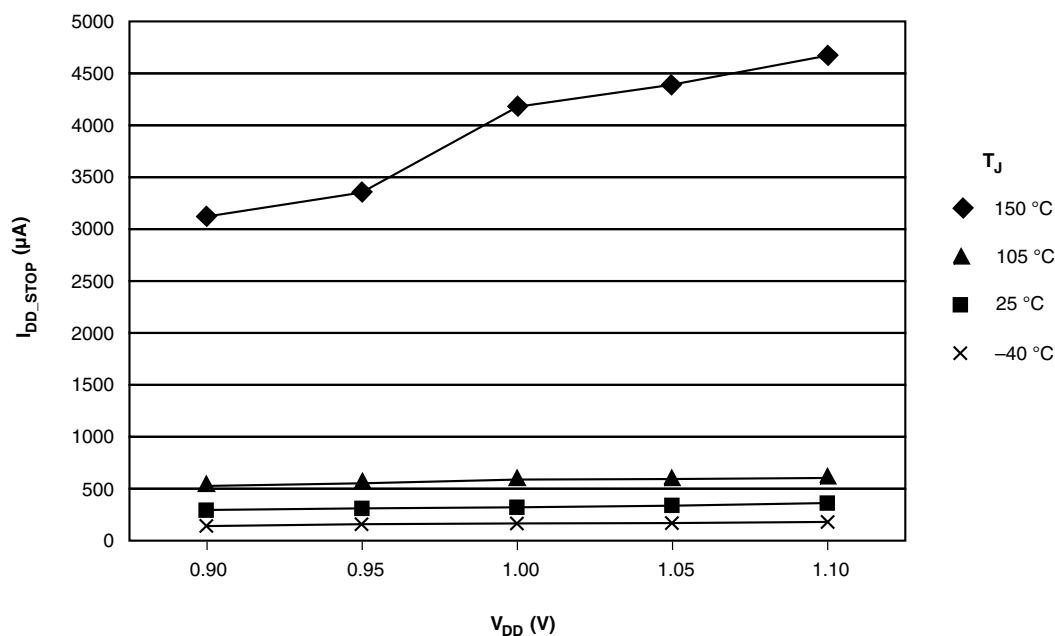
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	-0.3	3.8	V
I_{DD}	Digital supply current	—	185	mA
V_{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V_{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	$V_{DD} + 0.3$	V
I_D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V_{DDA}	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V
V_{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

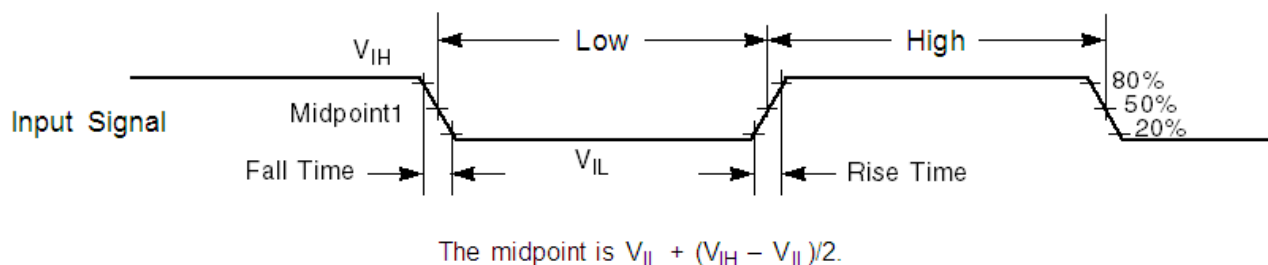


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
 - have $C_L=30\text{pF}$ loads,
 - are configured for fast slew rate ($\text{PORTx_PCRn[SRE]}=0$), and
 - are configured for high drive strength ($\text{PORTx_PCRn[DSE]}=1$)
2. input pins
 - have their passive filter disabled ($\text{PORTx_PCRn[PFE]}=0$)

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD} -to- V_{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS} -to- V_{SSA} differential voltage	-0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.7 \times V_{DD}$	—	V	
		$0.75 \times V_{DD}$	—	V	
V_{IL}	Input low voltage $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.35 \times V_{DD}$	V	
		—	$0.3 \times V_{DD}$	V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$	-5	—	mA	1
I_{ICAIO}	Analog ² , EXTAL, and XTAL pin DC injection current — single pin $V_{IN} < V_{SS}-0.3\text{V}$ (Negative current injection) $V_{IN} > V_{DD}+0.3\text{V}$ (Positive current injection)	-5	—	mA	3
		—	+5		
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins - Negative current injection - Positive current injection	-25	—	mA	
		—	+25		
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	4
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through an ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} is less than V_{DIO_MIN} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO_MIN}-V_{IN})/|I_{ICDIO}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function. Additionally, EXTAL and XTAL are analog pins.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX} , a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO_MIN}-V_{IN})/|I_{ICAIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO_MAX})/|I_{ICAIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
4. Open drain outputs must be pulled to V_{DD} .

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V _{LVW1H}	Low-voltage warning thresholds — high range					1
V _{LVW2H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW3H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW4H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V _{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V _{LVW1L}	Low-voltage warning thresholds — low range					1
V _{LVW2L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW3L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW4L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V _{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

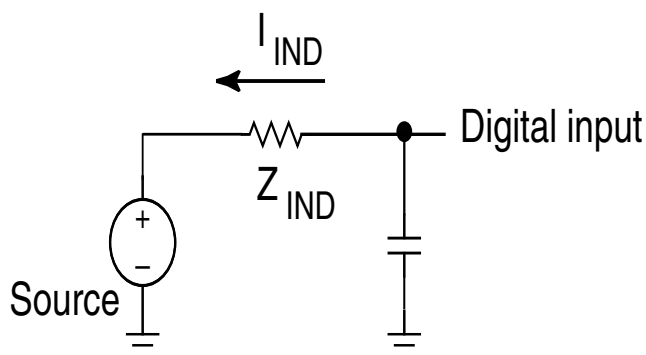
Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -9\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -3\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	Output high voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -0.6\text{ mA}$	$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength					2
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 9\text{ mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 3\text{ mA}$	—	—	0.5	V	
	Output low voltage — low drive strength					
	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 2\text{ mA}$	—	—	0.5	V	
	• $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 0.6\text{ mA}$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• $V_{SS} \leq V_{IN} \leq V_{DD}$					
	• All pins except EXTAL32, XTAL32, EXTAL, XTAL	—	0.002	0.5	μA	
	• EXTAL (PTA18) and XTAL (PTA19)	—	0.004	1.5	μA	
	• EXTAL32, XTAL32	—	0.075	10	μA	
I_{IND}	Input leakage current, digital pins					4, 5
	• $V_{SS} \leq V_{IN} \leq V_{IL}$					
	• All digital pins	—	0.002	0.5	μA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	μA	
	• PTD7	—	0.004	1	μA	
I_{IND}	Input leakage current, digital pins					4, 5, 6
	• $V_{IL} < V_{IN} < V_{DD}$					
	• $V_{DD} = 3.6\text{ V}$	—	18	26	μA	
	• $V_{DD} = 3.0\text{ V}$	—	12	49	μA	
	• $V_{DD} = 2.5\text{ V}$	—	8	13	μA	
	• $V_{DD} = 1.7\text{ V}$	—	3	6	μA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins • $V_{DD} < V_{IN} < 5.5\text{ V}$	—	1	50	μA	4, 5
Z_{IND}	Input impedance examples, digital pins • $V_{DD} = 3.6\text{ V}$ • $V_{DD} = 3.0\text{ V}$ • $V_{DD} = 2.5\text{ V}$ • $V_{DD} = 1.7\text{ V}$	— — — —	— — — —	48 55 57 85	$\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$ $\text{k}\Omega$	4, 7
R_{PU}	Internal pullup resistors	20	35	50	$\text{k}\Omega$	8
R_{PD}	Internal pulldown resistors	20	35	50	$\text{k}\Omega$	9

1. Typical values characterized at 25°C and $V_{DD} = 3.6\text{ V}$ unless otherwise noted.
2. Open drain outputs must be pulled to V_{DD} .
3. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
4. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
5. Internal pull-up/pull-down resistors disabled.
6. Characterized, not tested in production.
7. Examples calculated using V_{IL} relation, V_{DD} , and max I_{IND} : $Z_{IND} = V_{IL} / I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V.
8. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$
9. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$



5.2.4 Power mode transition operating behaviors

All specifications except t_{POR} , and $V_{LLSx} \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz
- MCG mode: FEI

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip. V_{DD} slew rate ≥ 5.7 kV/s V_{DD} slew rate < 5.7 kV/s	— —	300 1.7 V / (V_{DD} slew rate)	μ s	1
	• VLLS1 $\rightarrow$ RUN	—	134	μ s	
	• VLLS2 $\rightarrow$ RUN	—	96	μ s	
	• VLLS3 $\rightarrow$ RUN	—	96	μ s	
	• LLS $\rightarrow$ RUN	—	6.2	μ s	
	• VLPS $\rightarrow$ RUN	—	5.9	μ s	
	• STOP $\rightarrow$ RUN	—	5.9	μ s	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	45 47	70 72	mA mA	2
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V @ 25°C @ 125°C	— — —	61 63 72	85 71 87	mA mA mA	3, 4
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	35	—	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	15	—	mA	5
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	6

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	N/A	—	mA	7
I _{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	N/A	—	mA	8
I _{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.59	1.4	mA	
	• @ 70°C	—	2.26	7.9	mA	
	• @ 105°C	—	5.94	19.2	mA	
I _{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	93	435	μA	
	• @ 70°C	—	520	2000	μA	
	• @ 105°C	—	1350	4000	μA	
I _{DD_LLS}	Low leakage stop mode current at 3.0 V					9
	• @ –40 to 25°C	—	4.8	20	μA	
	• @ 70°C	—	28	68	μA	
	• @ 105°C	—	126	270	μA	
I _{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					9
	• @ –40 to 25°C	—	3.1	8.9	μA	
	• @ 70°C	—	17	35	μA	
	• @ 105°C	—	82	148	μA	
I _{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					
	• @ –40 to 25°C	—	2.2	5.4	μA	
	• @ 70°C	—	7.1	12.5	μA	
	• @ 105°C	—	41	125	μA	
I _{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	2.1	7.6	μA	
	• @ 70°C	—	6.2	13.5	μA	
	• @ 105°C	—	30	46	μA	
I _{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.33	0.39	μA	
	• @ 70°C	—	0.60	0.78	μA	
	• @ 105°C	—	1.97	2.9	μA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers • @ 1.8V • @ -40 to 25°C • @ 70°C • @ 105°C • @ 3.0V • @ -40 to 25°C • @ 70°C • @ 105°C	—	0.71	0.81	μA	10
		—	1.01	1.3	μA	
		—	2.82	4.3	μA	
		—	0.84	0.94	μA	
		—	1.17	1.5	μA	
		—	3.16	4.6	μA	
		—				

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 100MHz core and system clock, 50MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
3. 100MHz core and system clock, 50MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
4. Max values are measured with CPU executing DSP instructions.
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
6. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Data reflects devices with 128 KB of RAM.
10. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

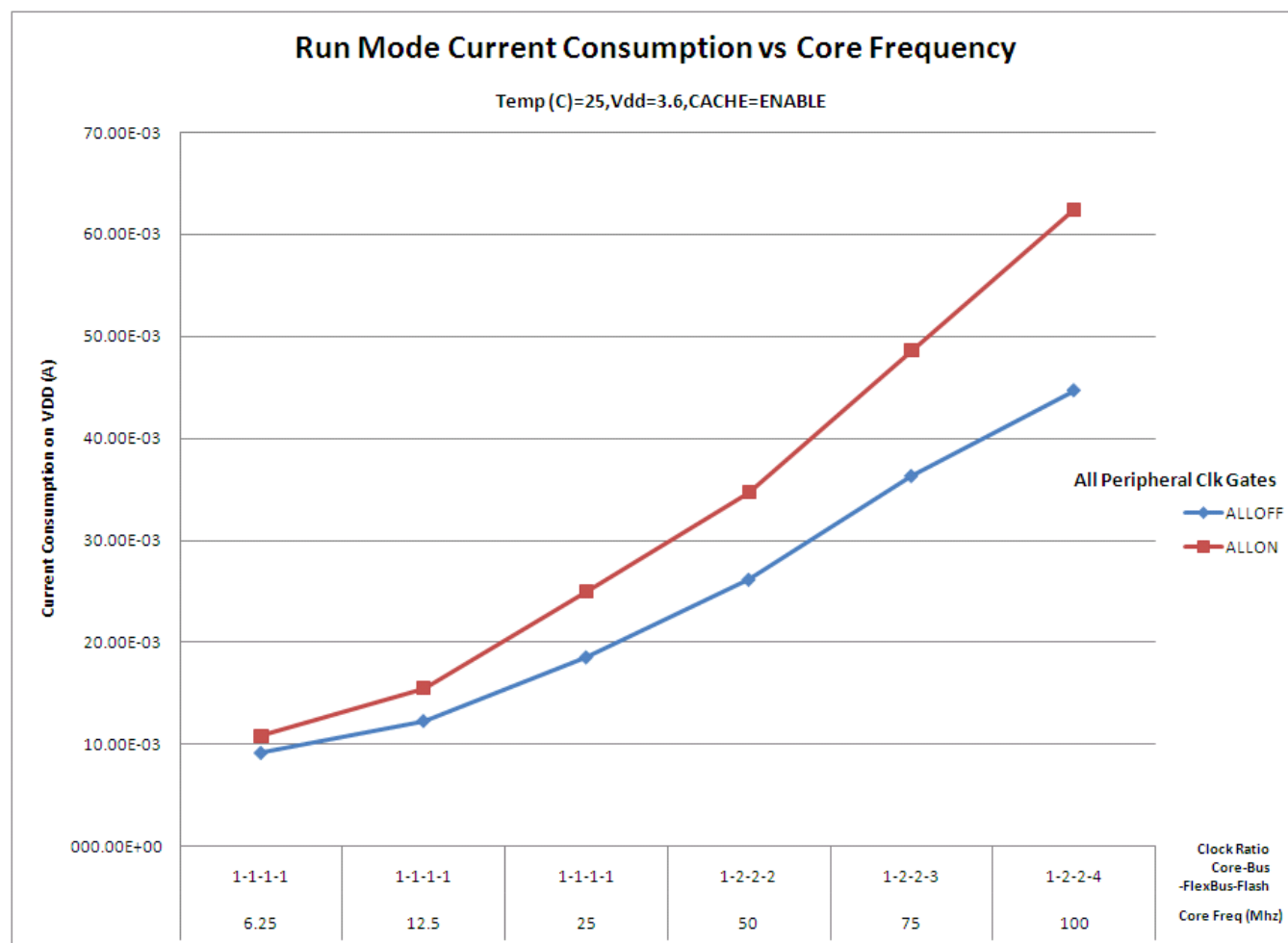


Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors as measured on 144LQFP and 144MAPBGA packages

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBμV	1, 2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBμV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBμV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBμV	
V _{RE_IEC}	IEC level	0.15–1000	K	K	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2. $V_{DD} = 3.3\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $f_{OSC} = 12\text{ MHz}$ (crystal), $f_{SYS} = 96\text{ MHz}$, $f_{BUS} = 48\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	16	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	4
	Port rise and fall time (low drive strength) - Slew disabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$ - Slew enabled $1.71 \leq V_{DD} \leq 2.7V$ $2.7 \leq V_{DD} \leq 3.6V$	— — — —	12 6 36 24	ns ns ns ns	5

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	−40	125	°C
T_A	Ambient temperature	−40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	81 MAPBGA	80 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	65	50	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	36	35	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	52	39	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	31	29	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	19	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	13	8	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	2	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.

Peripheral operating requirements and behaviors

2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Debug trace timing specifications

Table 12. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns
T_s	Data setup	3	—	ns
T_h	Data hold	2	—	ns

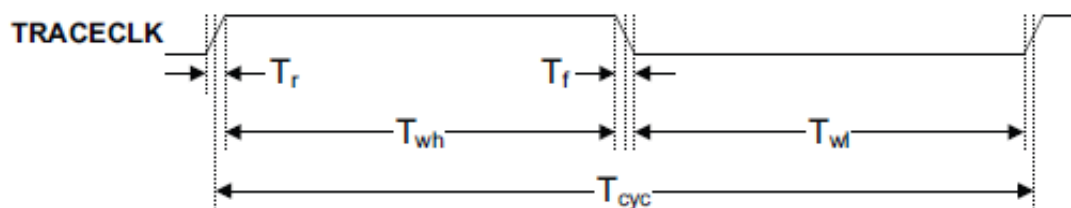


Figure 3. TRACE_CLKOUT specifications

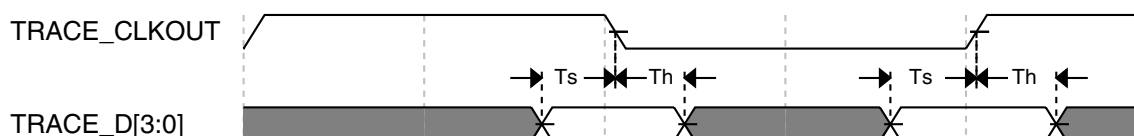


Figure 4. Trace data specifications

6.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 25 50	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	50 20 10	— — —	ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

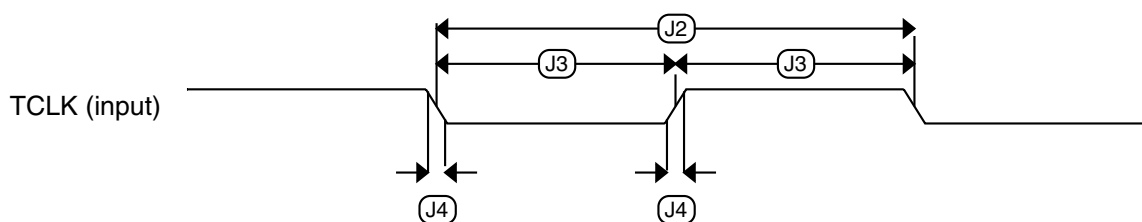
Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation - Boundary Scan - JTAG and CJTAG - Serial Wire Debug	0 0 0	10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns

Table continues on the next page...

Table 14. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
	• Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

**Figure 5. Test clock input timing**

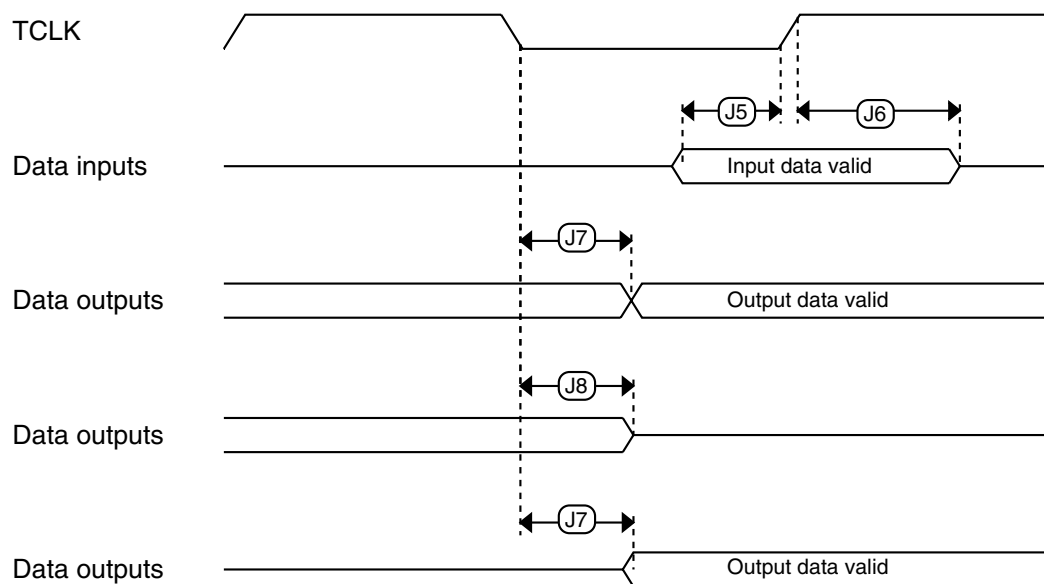


Figure 6. Boundary scan (JTAG) timing

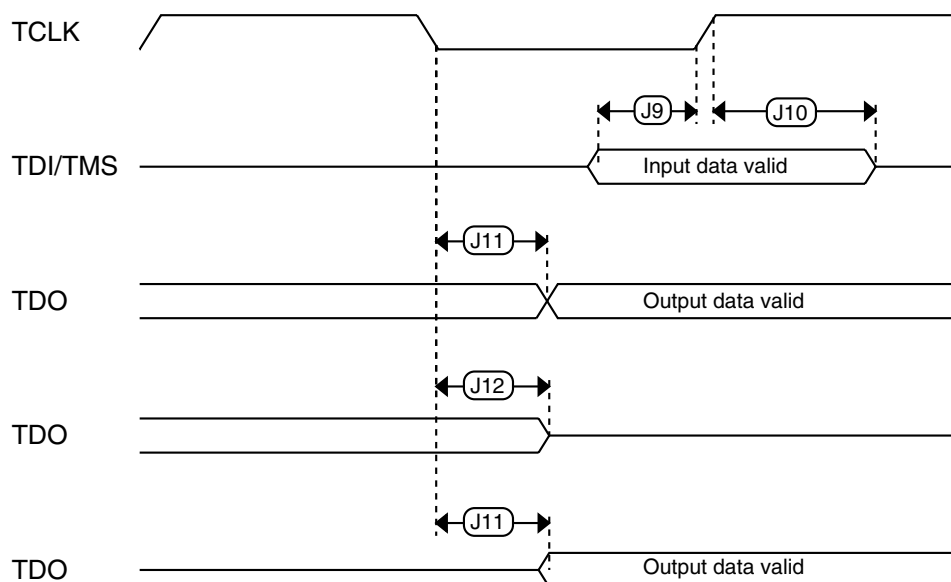


Figure 7. Test Access Port timing

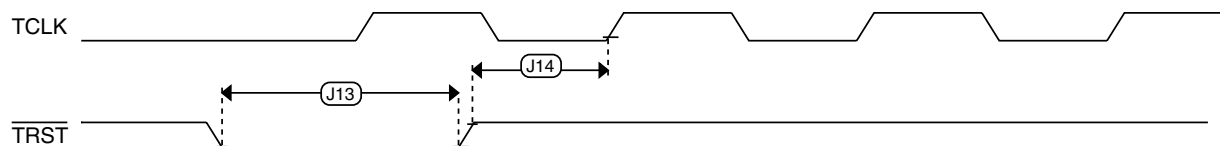


Figure 8. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{\text{ints_ft}}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$f_{\text{ints_t}}$	Internal reference frequency (slow clock) — user trimmed — over fixed voltage and temperature range of 0–70°C	31.25	—	38.2	kHz	
$\Delta f_{\text{dco_res_t}}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% f_{dco}	1
$\Delta f_{\text{dco_t}}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 1.5	± 4.5	% f_{dco}	1
$f_{\text{intf_ft}}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$f_{\text{intf_t}}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
$f_{\text{loc_low}}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{\text{ints_t}}$	—	—	kHz	
$f_{\text{loc_high}}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{\text{ints_t}}$	—	—	kHz	
FLL						
$f_{\text{fll_ref}}$	FLL reference frequency range	31.25	—	39.0625	kHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fil_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fil_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fil_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fil_ref}	80	83.89	100	MHz	
f _{dco_t_DMX32}	DCO output frequency	Low range (DRS=00) 732 × f _{fil_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fil_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fil_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fil_ref}	—	95.98	—	MHz	
J _{cyc_fll}	FLL period jitter - f_{VCO} = 48 MHz - f_{VCO} = 98 MHz	—	180	—	ps		
		—	150	—			
t _{fil_acquire}	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f _{vco}	VCO operating frequency		48.0	—	100	MHz	
I _{pll}	PLL operating current PLL @ 96 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)		—	1060	—	μA	7
I _{pll}	PLL operating current PLL @ 48 MHz (f_{osc_hi_1} = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)		—	600	—	μA	7
f _{pll_ref}	PLL reference frequency range		2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (RMS) - f_{vco} = 48 MHz - f_{vco} = 100 MHz	—	120	—	ps	8	
		—	50	—	ps		
J _{acc_pll}	PLL accumulated jitter over 1μs (RMS) - f_{vco} = 48 MHz - f_{vco} = 100 MHz	—	1350	—	ps	8	
		—	600	—	ps		
D _{lock}	Lock entry frequency tolerance		± 1.49	—	± 2.98	%	
D _{unl}	Lock exit frequency tolerance		± 4.47	—	± 5.97	%	
t _{pll_lock}	Lock detector detection time		—	—	150 × 10 ⁻⁶ + 1075(1/f _{pll_ref})	s	9

Peripheral operating requirements and behaviors

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.3.2 Oscillator electrical specifications

This section provides the electrical characteristics of the module.

6.3.2.1 Oscillator DC electrical specifications

Table 16. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	—	3.6	V	
I _{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	—	500	—	nA	1
		—	200	—	μA	
		—	300	—	μA	
		—	950	—	μA	
		—	1.2	—	mA	
		—	1.5	—	mA	
I _{DDOSC}	Supply current — high gain mode (HGO=1) • 32 kHz • 4 MHz • 8 MHz (RANGE=01) • 16 MHz • 24 MHz • 32 MHz	—	25	—	μA	1
		—	400	—	μA	
		—	500	—	μA	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
C _x	EXTAL load capacitance	—	—	—		2, 3
C _y	XTAL load capacitance	—	—	—		2, 3

Table continues on the next page...

Table 16. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M Ω	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M Ω	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M Ω	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M Ω	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k Ω	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k Ω	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k Ω	
V_{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD} =3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	

Table continues on the next page...

Table 17. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications**Table 18. 32kHz oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} ¹	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications

Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$V_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 20. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvp4}	Longword Program high-voltage time	—	7.5	18	μ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	416	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.4.1.2 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk256k}$	Read 1s Block execution time • 256 KB program/data flash	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	μ s	1

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program/data flash	—	435	3700	ms	2
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
$t_{pgmsec512}$	Program Section execution time • 512 bytes flash	—	2.4	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	870	7400	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
$t_{swapx01}$	Swap Control execution time • control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.4.1.3 Flash high voltage current behaviors

Table 22. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.4.1.4 Reliability specifications

Table 23. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
Program Flash						

Table continues on the next page...

Table 23. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
$t_{\text{nvmretp10k}}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{\text{nvmretp1k}}$	Data retention after up to 1 K cycles	20	100	—	years	
n_{nvmcycp}	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$.

6.4.2 EzPort Switching Specifications

Table 24. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{\text{SYS}}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{\text{SYS}}/8$	MHz
EP2	EZP_CS negation to next EZP_CS assertion	$2 \times t_{\text{EZP_CK}}$	—	ns
EP3	EZP_CS input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to EZP_CS input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	16	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	EZP_CS negation to EZP_Q tri-state	—	12	ns

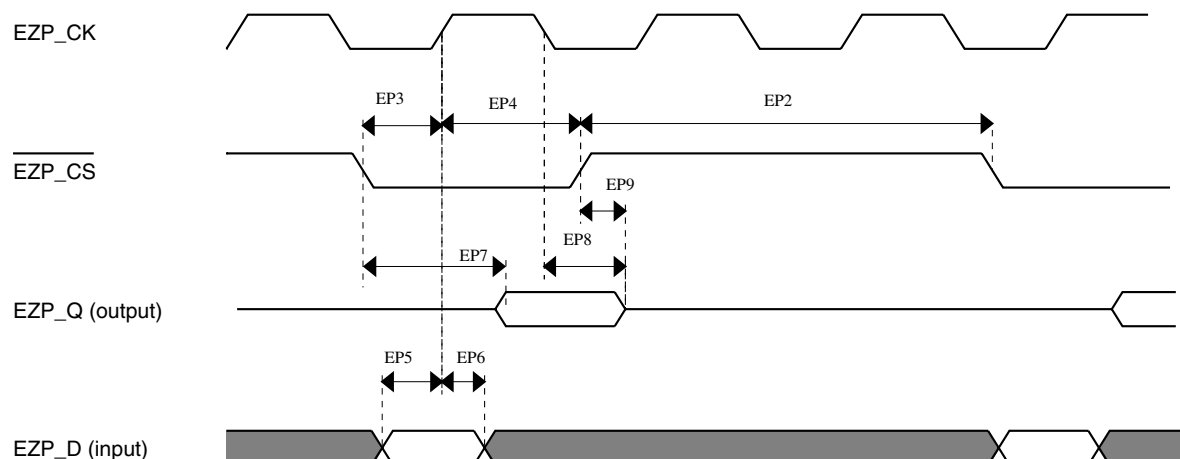


Figure 9. EzPort Timing Diagram

6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

6.6 Analog

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 25](#) and [Table 26](#) are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in [Table 27](#) and [Table 28](#).

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

6.6.1.1 16-bit ADC operating conditions

Table 25. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} ($V_{DD} - V_{DDA}$)	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} ($V_{SS} - V_{SSA}$)	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage	16-bit differential mode - All other modes	V_{REFL} V_{REFL}	— —	31/32 * V_{REFH} V_{REFH}	V	
C_{ADIN}	Input capacitance	16-bit mode 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	k Ω	
R_{AS}	Analog source resistance	13-bit / 12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k Ω	3
f_{ADCK}	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	$\leq$ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25 °C, $f_{ADCK} = 1.0$ MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

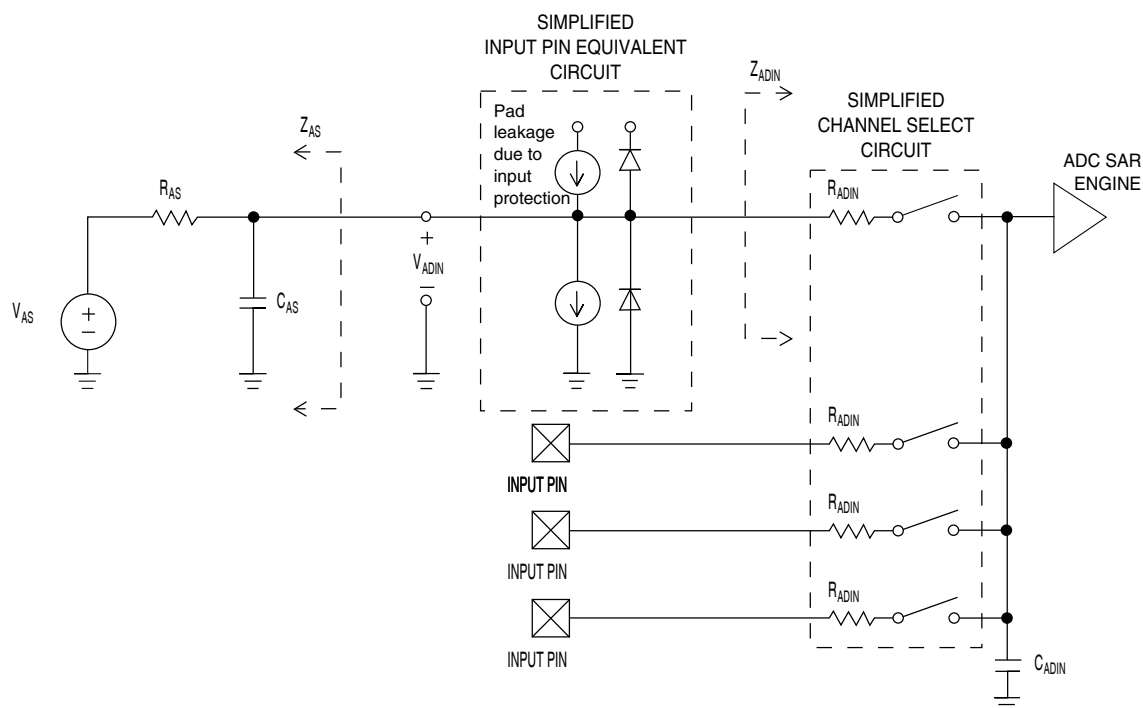


Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	- ADLPC = 1, ADHSC = 0 - ADLPC = 1, ADHSC = 1 - ADLPC = 0, ADHSC = 0 - ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	$t_{ADACK} = 1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	12-bit modes <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB ⁴	5
DNL	Differential non-linearity	12-bit modes <12-bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB ⁴	5
INL	Integral non-linearity	12-bit modes <12-bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB ⁴	5
E_{FS}	Full-scale error	12-bit modes <12-bit modes	— —	-4 -1.4	-5.4 -1.8	LSB ⁴	$V_{ADIN} = V_{DDA}$ 5

Table continues on the next page...

Table 26. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
E_Q	Quantization error	16-bit modes ≤13-bit modes	—	-1 to 0	—	LSB ⁴	
ENOB	Effective number of bits	16-bit differential mode - Avg = 32 - Avg = 4 16-bit single-ended mode - Avg = 32 - Avg = 4	12.8 11.9	14.5 13.8	— —	bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	
THD	Total harmonic distortion	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	— —	-94 -85	— —	dB dB	7
SFDR	Spurious free dynamic range	16-bit differential mode - Avg = 32 16-bit single-ended mode - Avg = 32	82 78	95 90	— —	dB dB	7
E_{IL}	Input leakage error		$I_{IN} \times R_{AS}$			mV	I_{IN} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume $V_{DDA} = 3.0$ V, Temp = 25°C, $f_{ADCK} = 2.0$ MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and the ADLPC bit (low power). For lowest power operation the ADLPC bit must be set, the HSC bit must be clear with 1 MHz ADC conversion clock speed.
4. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

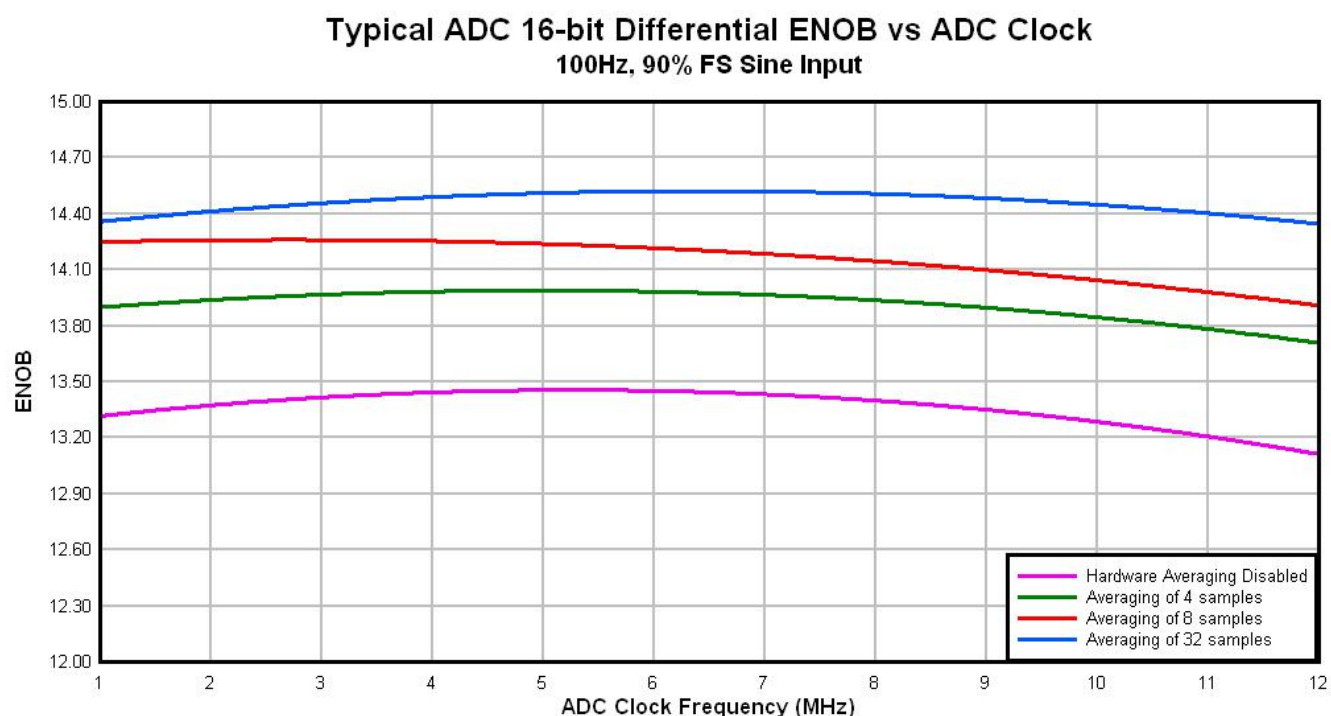


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

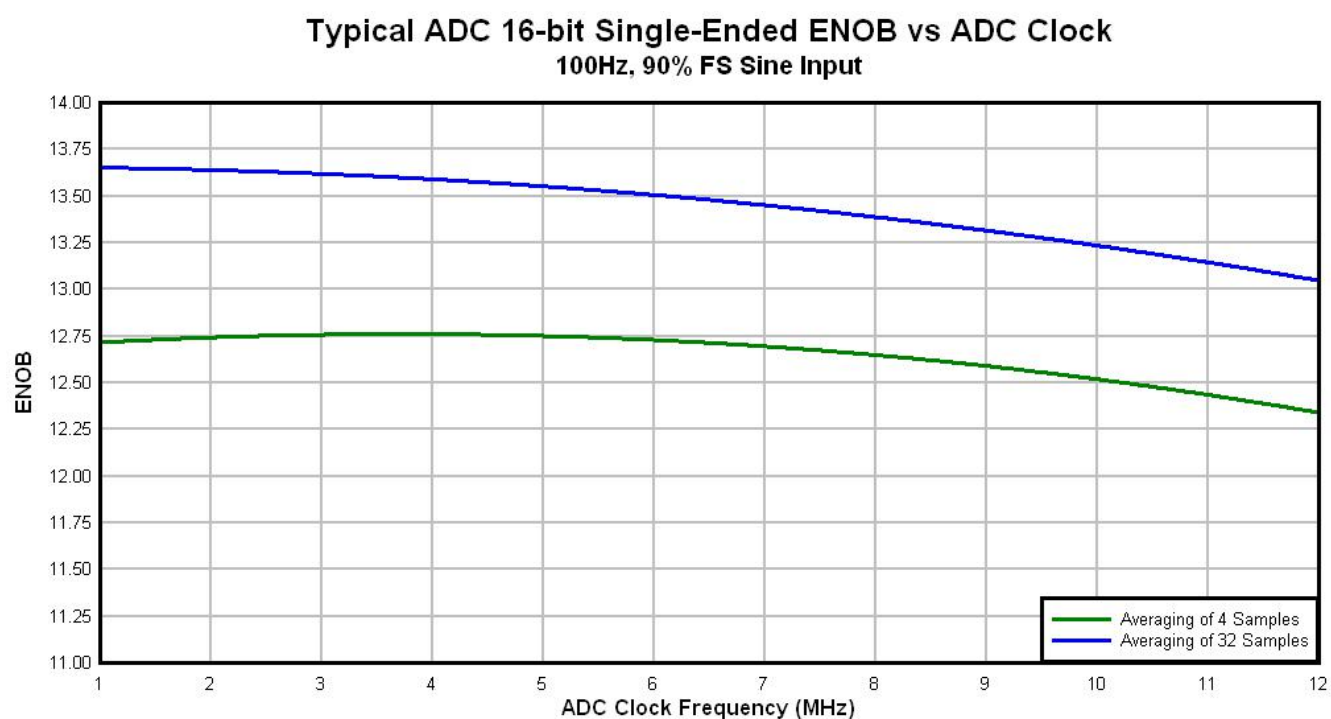


Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.3 16-bit ADC with PGA operating conditions

Table 27. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
V _{REFPGA}	PGA ref voltage		VREF_OUT T	VREF_OUT T	VREF_OUT T	V	2, 3
V _{ADIN}	Input voltage		V _{SSA}	—	V _{DDA}	V	
V _{CM}	Input Common Mode range		V _{SSA}	—	V _{DDA}	V	
R _{PGAD}	Differential input impedance	Gain = 1, 2, 4, 8 Gain = 16, 32 Gain = 64	— — —	128 64 32	— — —	kΩ	IN+ to IN- ⁴
R _{AS}	Analog source resistance		—	100	—	Ω	5
T _S	ADC sampling time		1.25	—	—	μs	6
C _{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	18.484	—	450	Ksps	7
		16 bit modes No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz	37.037	—	250	Ksps	8

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25μs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics

Table 28. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}} \left(\frac{(V_{REFPGA} \times 0.583) - V_{CM}}{(Gain+1)} \right)$			A	3
		Gain =1, V _{REFPGA} =1.2V, V _{CM} =0.5V	—	1.54	—	μA	
		Gain =64, V _{REFPGA} =1.2V, V _{CM} =0.1V	—	0.57	—	μA	
G	Gain ⁴	- PGAG=0 - PGAG=1 - PGAG=2 - PGAG=3 - PGAG=4 - PGAG=5 - PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		R _{AS} < 100Ω
BW	Input signal bandwidth	16-bit modes < 16-bit modes	—	—	4	kHz	
			—	—	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode rejection ratio	- Gain=1 - Gain=64	—	-84	—	dB	V _{CM} = 500mVpp, f _{VCM} = 50Hz, 100Hz
			—	-85	—	dB	
V _{OFS}	Input offset voltage		—	0.2	—	mV	Output offset = V _{OFS} *(Gain+1)
T _{GSW}	Gain switching settling time		—	—	10	μs	5
E _{IL}	Input leakage error	All modes	I _{in} × R _{AS}			mV	I _{in} = leakage current (refer to the MCU's voltage and current operating ratings)
V _{PP,DIFF}	Maximum differential input signal swing		$\left(\frac{(\min(V_X, V_{DDA} - V_X) - 0.2) \times 4}{Gain} \right)$ where V _X = V _{REFPGA} × 0.583			V	6
SNR	Signal-to-noise ratio	- Gain=1 - Gain=64	80	90	—	dB	16-bit differential mode, Average=32
			52	66	—	dB	

Table continues on the next page...

Table 28. 16-bit ADC with PGA characteristics (continued)

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
THD	Total harmonic distortion	• Gain=1	85	100	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	49	95	—	dB	
SFDR	Spurious free dynamic range	• Gain=1	85	105	—	dB	16-bit differential mode, Average=32, $f_{in}=100\text{Hz}$
		• Gain=64	53	88	—	dB	
ENOB	Effective number of bits	• Gain=1, Average=4	11.6	13.4	—	bits	16-bit differential mode, $f_{in}=100\text{Hz}$
		• Gain=64, Average=4	7.2	9.6	—	bits	
		• Gain=1, Average=32	12.8	14.5	—	bits	
		• Gain=2, Average=32	11.0	14.3	—	bits	
		• Gain=4, Average=32	7.9	13.8	—	bits	
		• Gain=8, Average=32	7.3	13.1	—	bits	
		• Gain=16, Average=32	6.8	12.5	—	bits	
		• Gain=32, Average=32	6.8	11.5	—	bits	
		• Gain=64, Average=32	7.5	10.6	—	bits	
SINAD	Signal-to-noise plus distortion ratio	See ENOB	$6.02 \times \text{ENOB} + 1.76$			dB	

1. Typical values assume $V_{DDA}=3.0\text{V}$, $\text{Temp}=25^{\circ}\text{C}$, $f_{ADCK}=6\text{MHz}$ unless otherwise stated.
2. This current is a PGA module adder, in addition to ADC conversion currents.
3. Between IN+ and IN-. The PGA draws a DC current from the input terminals. The magnitude of the DC current is a strong function of input common mode voltage (V_{CM}) and the PGA gain.
4. $\text{Gain} = 2^{\text{PGAG}}$
5. After changing the PGA gain setting, a minimum of 2 ADC+PGA conversions should be ignored.
6. Limit the input signal swing so that the PGA does not saturate during operation. Input signal swing is dependent on the PGA reference voltage and gain setting.

6.6.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOH}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	—	—	40	μ s
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD}-0.6$ V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. $1 \text{ LSB} = V_{\text{reference}}/64$

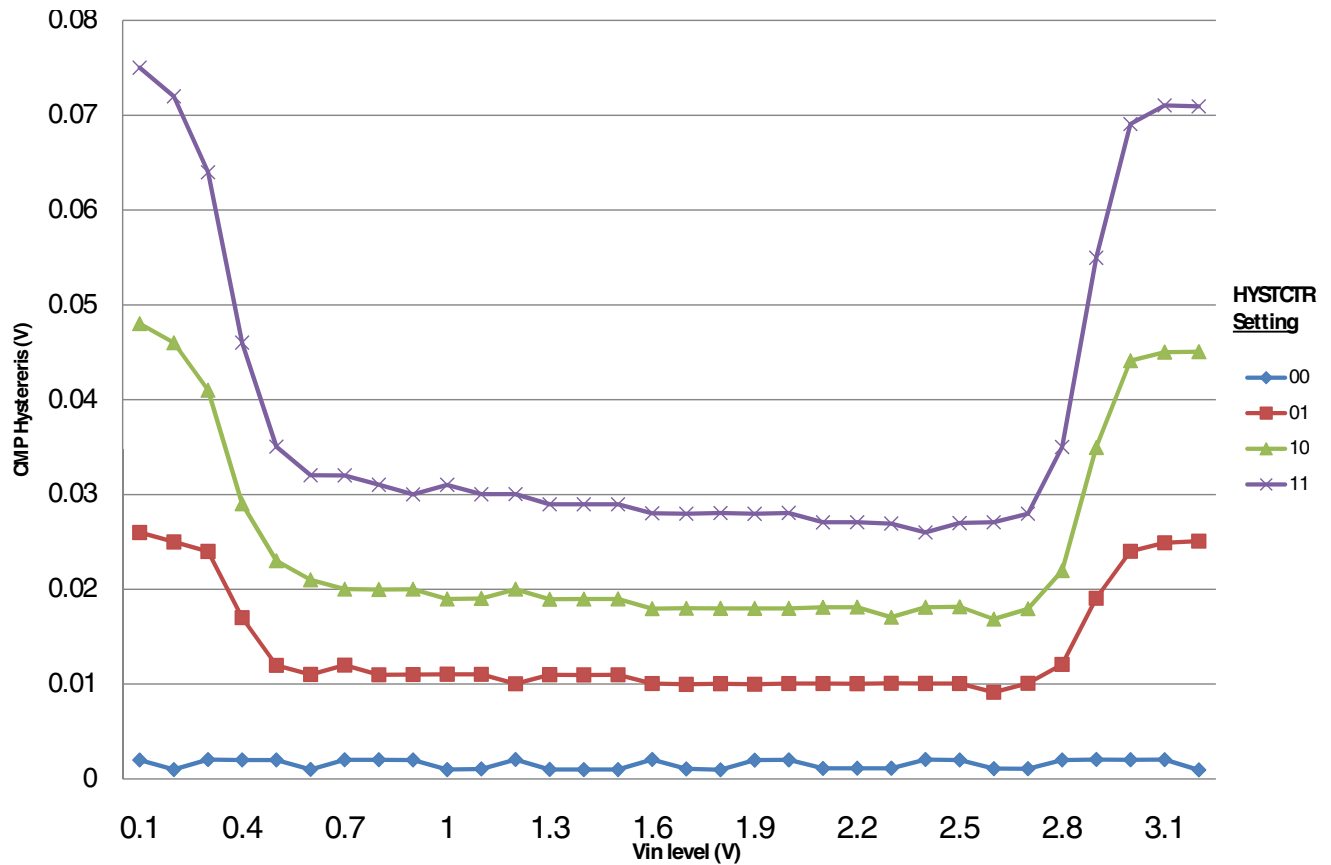


Figure 13. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=0)

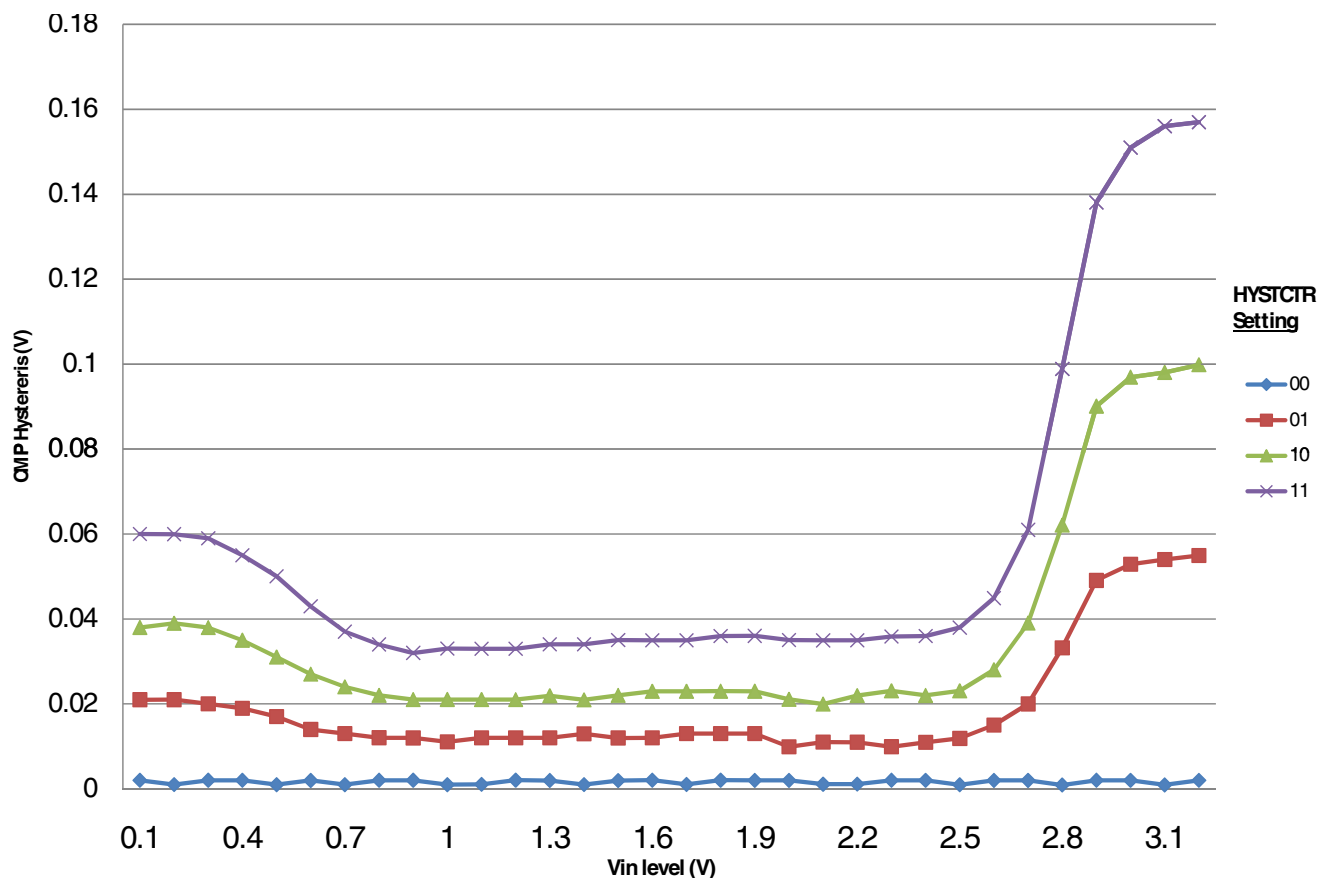


Figure 14. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements

Table 30. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	Operating temperature range of the device		°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

6.6.3.2 12-bit DAC operating behaviors

Table 31. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	± 8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	—	—	± 1	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF_OUT}$	—	—	± 1	LSB	4
V_{OFFSET}	Offset error	—	± 0.4	± 0.8	%FSR	5
E_G	Gain error	—	± 0.1	± 0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4$ V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	$\mu V/C$	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
R_{op}	Output resistance load = 3 k Ω	—	—	250	Ω	
SR	Slew rate -80h → F7Fh → 80h - High power (SP_{HP}) - Low power (SP_{LP})	1.2 0.05	1.7 0.12	— —	V/ μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth - High power (SP_{HP}) - Low power (SP_{LP})	550 40	— —	— —	kHz	

1. Settling within ± 1 LSB
2. The INL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
3. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV
4. The DNL is measured for 0 + 100 mV to $V_{DACR} - 100$ mV with $V_{DDA} > 2.4$ V
5. Calculated by a best fit curve from $V_{SS} + 100$ mV to $V_{DACR} - 100$ mV
6. $V_{DDA} = 3.0$ V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

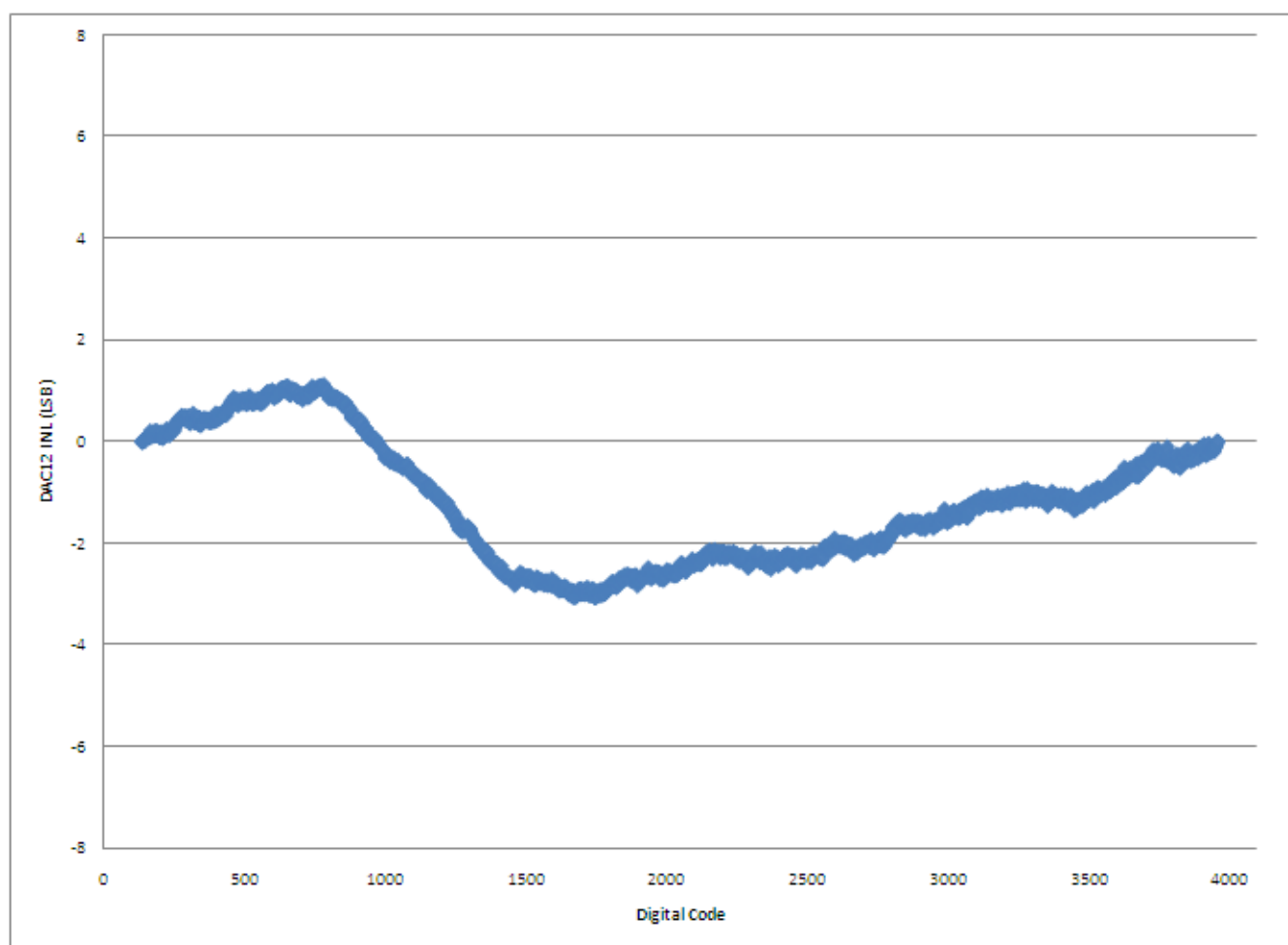


Figure 15. Typical INL error vs. digital code

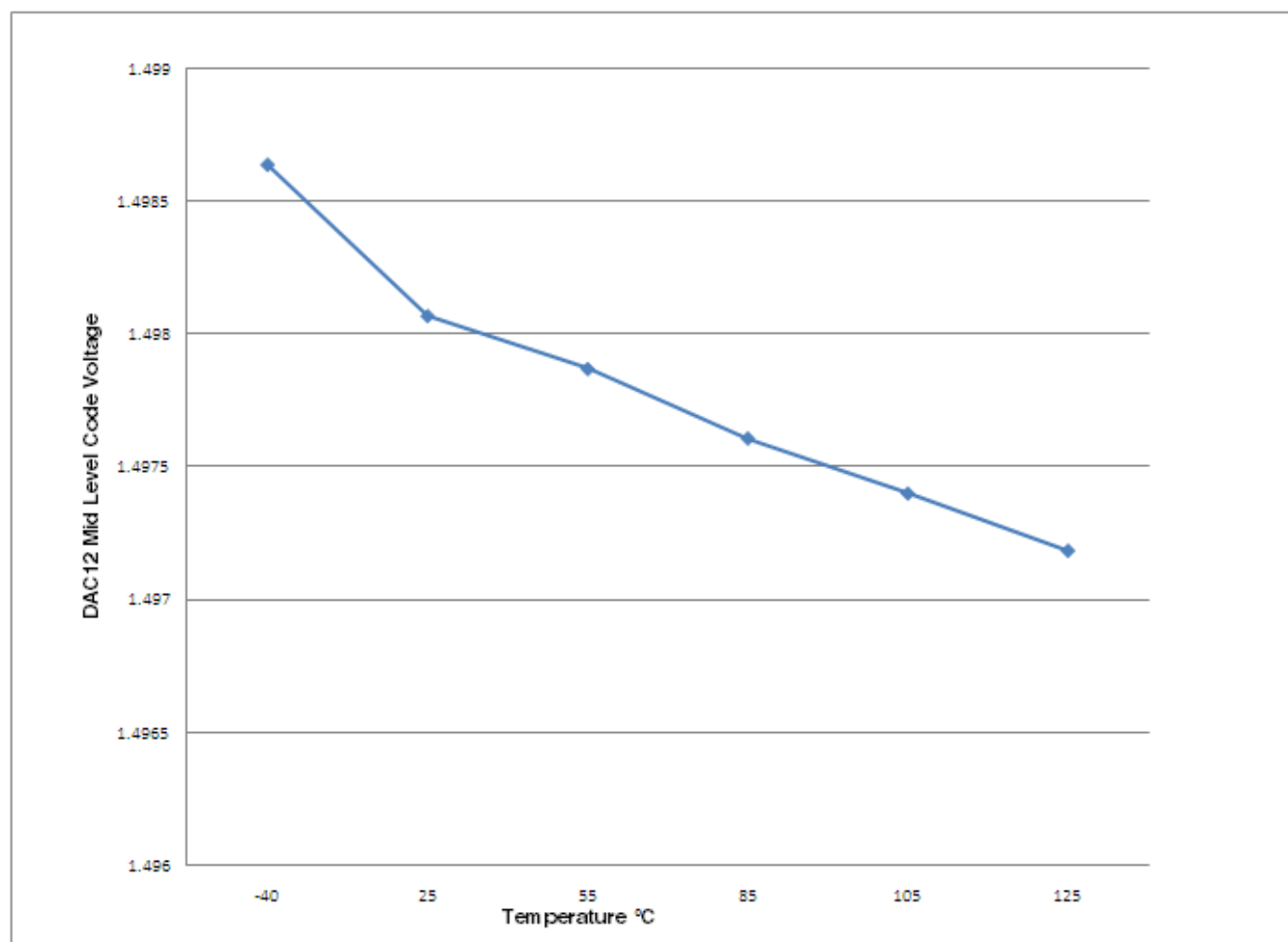


Figure 16. Offset at half scale vs. temperature

6.6.4 Voltage reference electrical specifications

Table 32. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71	3.6	V	
T _A	Temperature	Operating temperature range of the device		°C	
C _L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 33. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift ($V_{max} - V_{min}$ across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	μA	1
I_{lp}	Low-power buffer current	—	—	360	μA	1
I_{hp}	High-power buffer current	—	—	1	mA	1
ΔV_{LOAD}	Load regulation				mV	1, 2
	• current = + 1.0 mA	—	2	—		
	• current = - 1.0 mA	—	5	—		
T_{stup}	Buffer startup time	—	—	100	μs	
V_{vdrift}	Voltage drift ($V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

Table 34. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	$^{\circ}C$	

Table 35. VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

6.7 Timers

See [General switching specifications](#).

6.8 Communication interfaces

6.8.1 CAN switching specifications

See [General switching specifications](#).

6.8.2 DSPI switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 36. Master mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

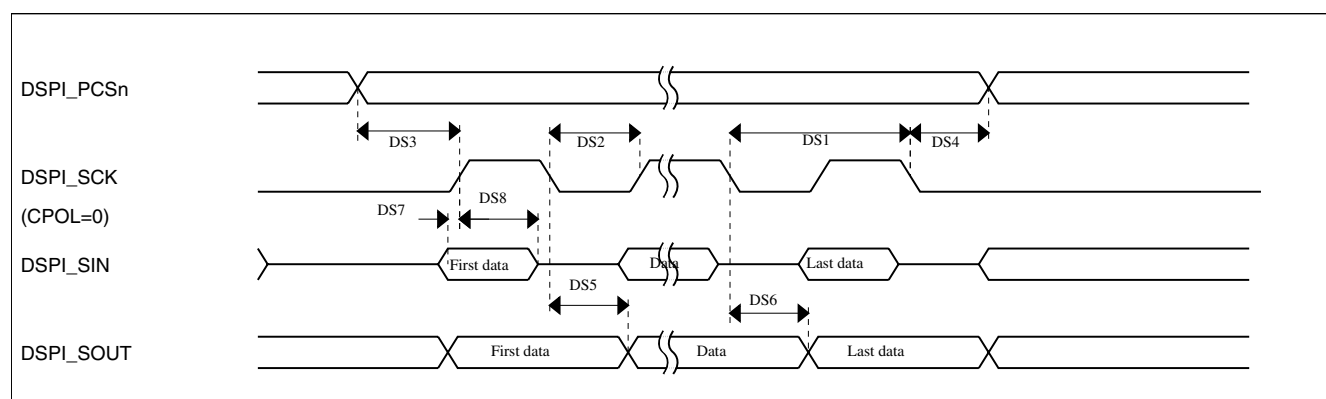
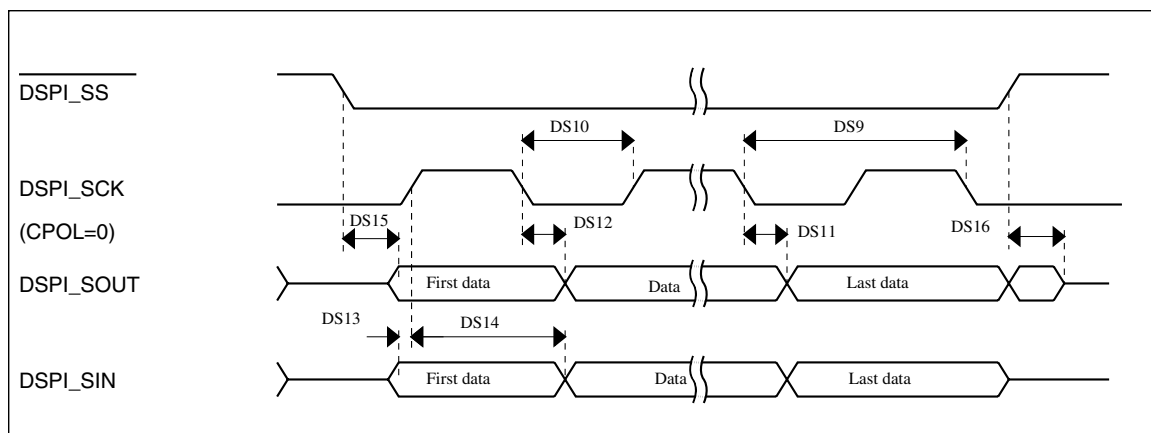


Figure 17. DSPI classic SPI timing — master mode

Table 37. Slave mode DSPI timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	14	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	14	ns

**Figure 18. DSPI classic SPI timing — slave mode**

6.8.3 DSPI switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Table 38. Master mode DSPI timing (full voltage range)

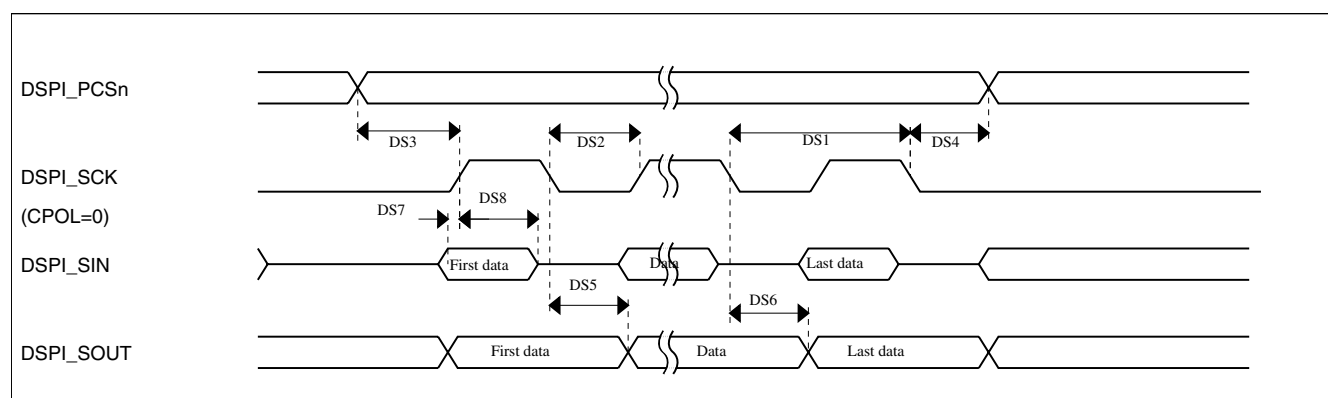
Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	

Table continues on the next page...

Table 38. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}/2}) - 4$	$(t_{\text{SCK}/2}) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{\text{BUS}} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 19. DSPI classic SPI timing — master mode****Table 39. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}/2}) - 4$	$(t_{\text{SCK}/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	19	ns

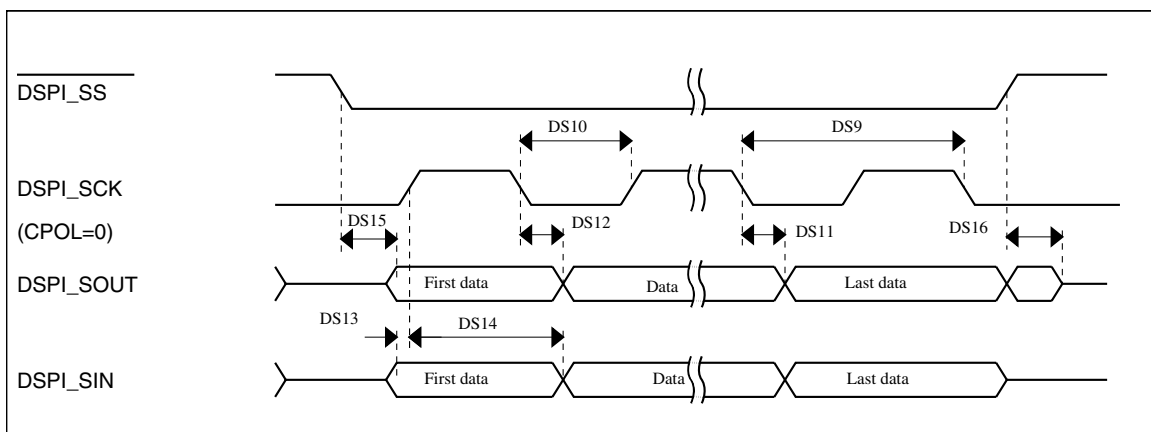


Figure 20. DSPI classic SPI timing — slave mode

6.8.4 Inter-Integrated Circuit Interface (I²C) timing

Table 40. I²C timing

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD}; STA$	4	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU}; STA$	4.7	—	0.6	—	μs
Data hold time for I ² C bus devices	$t_{HD}; DAT$	0 ¹	3.45 ²	0 ³	0.9 ¹	μs
Data set-up time	$t_{SU}; DAT$	250 ⁴	—	100 ^{2, 5}	—	ns
Rise time of SDA and SCL signals	t_r	—	1000	$20 + 0.1C_b$ ⁶	300	ns
Fall time of SDA and SCL signals	t_f	—	300	$20 + 0.1C_b$ ⁵	300	ns
Set-up time for STOP condition	$t_{SU}; STO$	4	—	0.6	—	μs
Bus free time between STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	N/A	N/A	0	50	ns

1. The master mode I²C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum $t_{HD}; DAT$ must be met only if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. Input signal Slew = 10ns and Output Load = 50pf
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I²C bus device can be used in a Standard mode I²C bus system, but the requirement $t_{SU}; DAT \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line $t_{rmax} + t_{SU}; DAT = 1000 + 250 = 1250$ ns (according to the Standard mode I²C bus specification) before the SCL line is released.

6. C_b = total capacitance of the one bus line in pF.

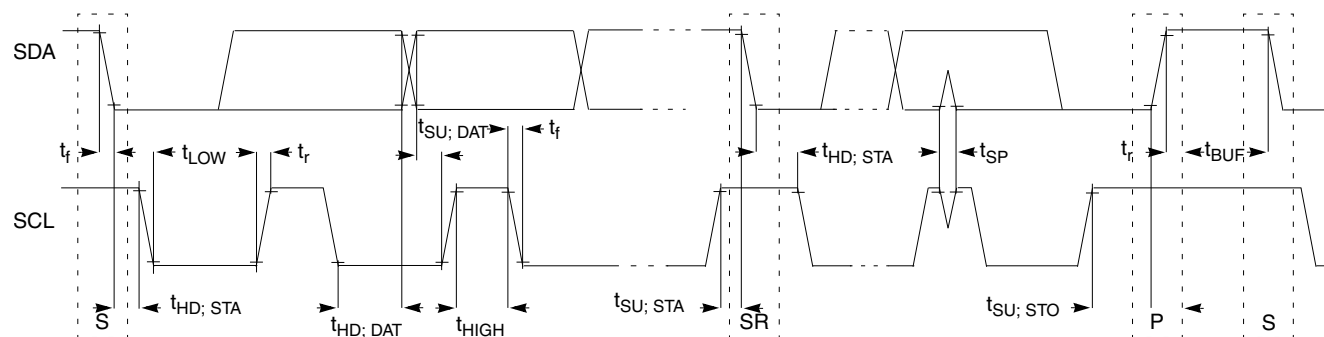


Figure 21. Timing definition for fast and standard mode devices on the I²C bus

6.8.5 UART switching specifications

See [General switching specifications](#).

6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 41. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
Card input clock					
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns
SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

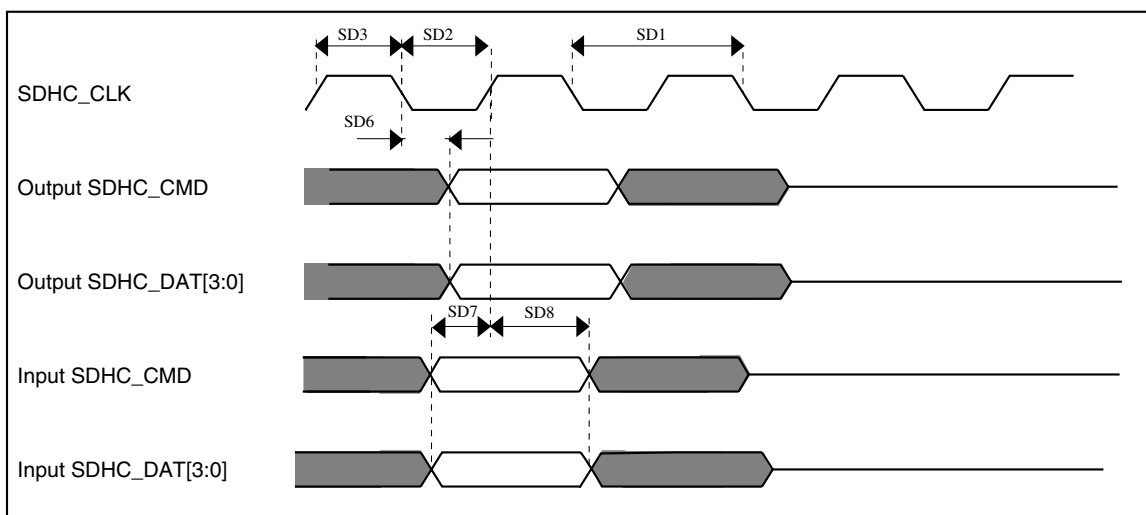


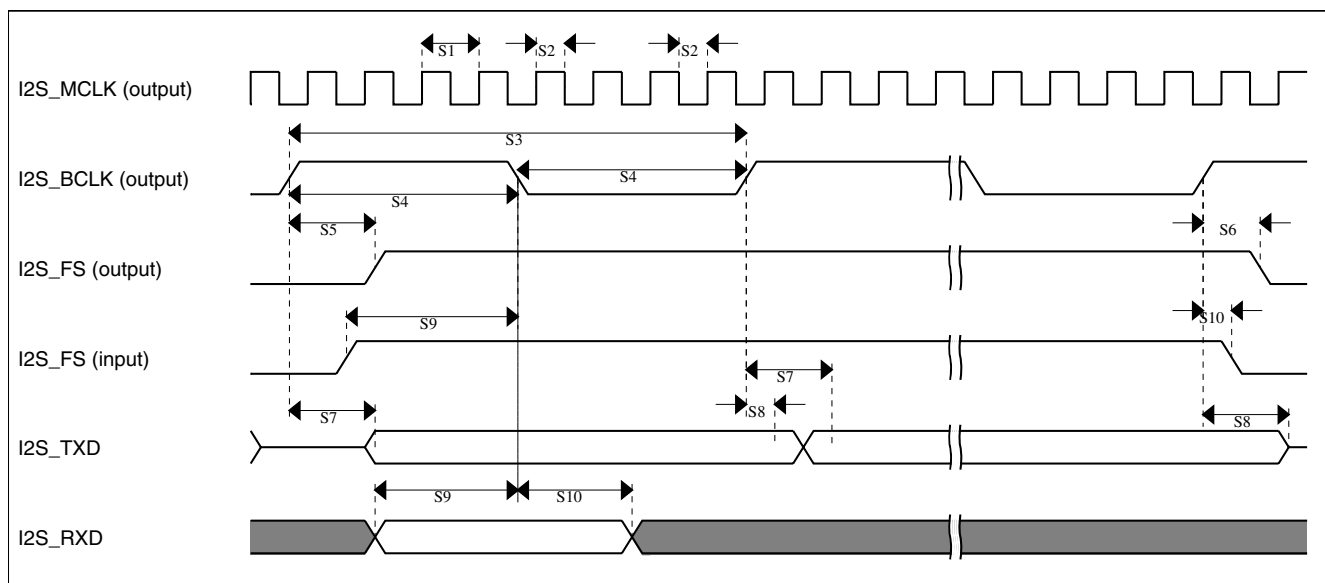
Figure 22. SDHC timing

6.8.7 I²S switching specifications

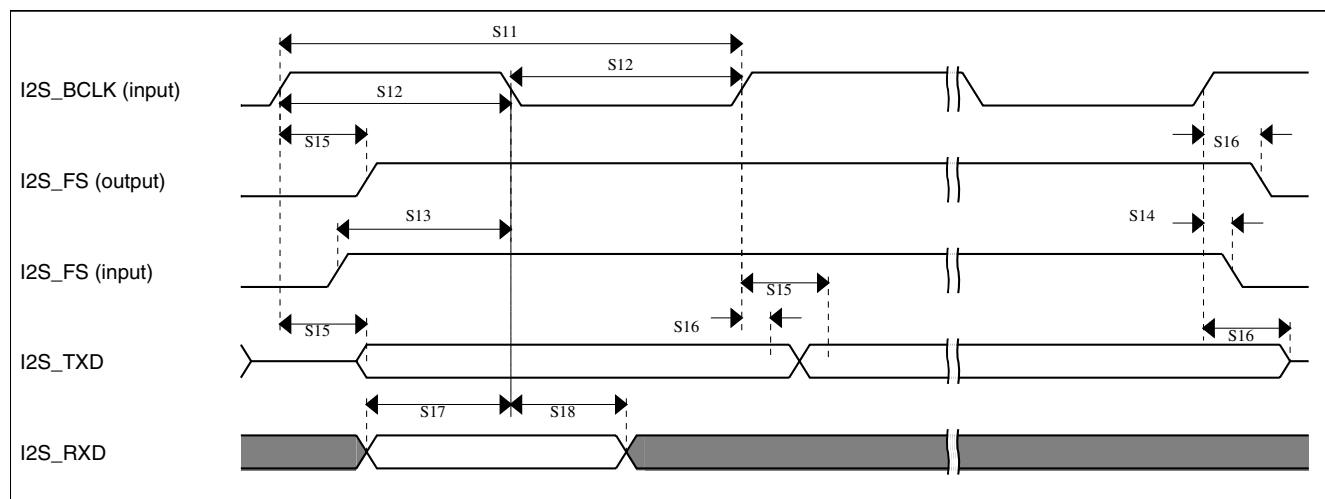
This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Table 42. I²S master mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t _{sys}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t _{sys}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Figure 23. I²S timing — master modeTable 43. I²S slave mode timing (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t _{sys}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	20	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

Figure 24. I²S timing — slave modesTable 44. I²S master mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	2 x t _{sys}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t _{sys}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-4.3	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-4.6	—	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	23.9	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0	—	ns

Table 45. I²S slave mode timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_BCLK cycle time (input)	8 x t _{sys}	—	ns
S12	I2S_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_FS input setup before I2S_BCLK	10	—	ns
S14	I2S_FS input hold after I2S_BCLK	3.5	—	ns
S15	I2S_BCLK to I2S_TXD/I2S_FS output valid	—	28.6	ns
S16	I2S_BCLK to I2S_TXD/I2S_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_BCLK	2	—	ns

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 46. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71	—	3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1
f _{REFmax}	Reference oscillator frequency	—	5.5	12.7	MHz	2
f _{ELEmax}	Electrode oscillator frequency	—	0.5	4.0	MHz	3
C _{REF}	Internal reference capacitor	0.5	1	1.2	pF	
V _{DELTA}	Oscillator delta voltage	100	600	760	mV	4
I _{REF}	Reference oscillator current source base current 1uA setting (REFCHRG=0) 32uA setting (REFCHRG=31)	— —	1.133 36	1.5 50	μA	3, 5
I _{ELE}	Electrode oscillator current source base current 1uA setting (EXTCHRG=0) 32uA setting (EXTCHRG=31)	— —	1.133 36	1.5 50	μA	3, 6
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	7
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
MaxSens	Maximum sensitivity	0.003	12.5	—	fF/count	10
Res	Resolution	—	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	11
I _{TSI_RUN}	Current added in run mode	—	55	—	μA	
I _{TSI_LP}	Low power mode current adder	—	1.3	2.5	μA	12

1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.
2. CAPTRM=7, DELVOL=7, and fixed external capacitance of 20 pF.
3. CAPTRM=0, DELVOL=2, and fixed external capacitance of 20 pF.
4. CAPTRM=0, EXTCHRG=9, and fixed external capacitance of 20 pF.
5. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.
6. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.
7. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; I_{ext} = 16.
8. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; I_{ext} = 16.
9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; I_{ext} = 16.
10. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes, it is equal to $(C_{ref} * I_{ext}) / (I_{ref} * PS * NSCN)$. Sensitivity depends on the configuration used. The typical value listed is based on the following configuration: I_{ext} = 5 μA, EXTCHRG = 4, PS = 128, NSCN = 2, I_{ref} = 16 μA, REFCHRG = 15, C_{ref} = 1.0 pF. The minimum sensitivity describes the smallest possible capacitance that can be measured by a single count (this is the best sensitivity but is described as a minimum because it's the smallest number). The minimum sensitivity parameter is based on the following configuration: I_{ext} = 1 μA, EXTCHRG = 0, PS = 128, NSCN = 32, I_{ref} = 32 μA, REFCHRG = 31, C_{ref} = 0.5 pF.
11. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, DELVOL = 2, EXTCHRG = 15.
12. CAPTRM=7, DELVOL=2, REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

6.9.2 LCD electrical characteristics

Table 47. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG} - HREFSEL=0, RVTRIM=1111 - HREFSEL=0, RVTRIM=1000 - HREFSEL=0, RVTRIM=0000 - HREFSEL=1, RVTRIM=1111 - HREFSEL=1, RVTRIM=1000 - HREFSEL=1, RVTRIM=0000	—	1.11	—	V	3
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
—	V_{IREG} ripple - HREFSEL = 0 - HREFSEL = 1	—	—	30	mV	
		—	—	50	mV	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	μA	4
I_{RBIAS}	RBIAS current adder - LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) - LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	10	—	μA	
		—	1	—	μA	
R_{RBIAS}	RBIAS resistor values - LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF) - LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	0.28	—	M Ω	
		—	2.98	—	M Ω	
V_{LL2}	V_{LL2} voltage - HREFSEL = 0 - HREFSEL = 1	2.0 – 5%	2.0	—	V	
		3.3 – 5%	3.3	—	V	
V_{LL3}	V_{LL3} voltage - HREFSEL = 0 - HREFSEL = 1	3.0 – 5%	3.0	—	V	
		5 – 5%	5	—	V	

1. The actual value used could vary with tolerance.

2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_IREG maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. 2000 pF load LCD, 32 Hz frame frequency

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
80-pin LQFP	98ASS23174W
81-pin MAPBGA	98ASA00344D

8 Pinout

8.1 K30 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

The 81-pin ballmap assignments are currently being developed.
The • in the entries in this package column indicate which signals are present on the package.

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E4	1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
E3	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
E2	3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_ b	SDHC0_DCLK				
F4	4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_ b	SDHC0_CMD				

Pinout

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E7	—	VDD	VDD	VDD								
F7	—	VSS	VSS	VSS								
H7	5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
G4	6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
E6	7	VDD	VDD	VDD								
G7	8	VSS	VSS	VSS								
F1	9	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
F2	10	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPT0_ALT3		
G1	11	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_ b	I2C0_SDA				
G2	12	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_ b	I2C0_SCL				
L6	—	VSS	VSS	VSS								
K1	13	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
K2	14	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
L1	15	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	16	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	17	VDDA	VDDA	VDDA								
G5	18	VREFH	VREFH	VREFH								
G6	19	VREFL	VREFL	VREFL								
F6	20	VSSA	VSSA	VSSA								
L3	21	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K5	22	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
L4	23	XTAL32	XTAL32	XTAL32								
L5	24	EXTAL32	EXTAL32	EXTAL32								
K6	25	VBAT	VBAT	VBAT								
J6	26	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
H8	27	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
J7	28	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSIO_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
H9	29	PTA3	JTAG_TMS/ SWD_DIO	TSIO_CH4	PTA3	UART0_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
J8	30	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSIO_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
K7	31	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_ BCLK	JTAG_TRST	
E5	—	VDD	VDD	VDD								
G3	—	VSS	VSS	VSS								
K8	32	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0			I2S0_TXD	FTM1_QD_ PHA	
L8	33	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1			I2S0_TX_FS	FTM1_QD_ PHB	
K9	34	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX			I2S0_TX_ BCLK		
L9	35	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX			I2S0_RXD		
J10	36	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_ b			I2S0_RX_FS		
H10	37	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_ b			I2S0_MCLK	I2S0_CLKIN	
L10	38	VDD	VDD	VDD								
K10	39	VSS	VSS	VSS								
L11	40	PTA18	EXTAL	EXTAL	PTA18		FTM0_FLT2	FTM_CLKIN0				
K11	41	PTA19	XTAL	XTAL	PTA19		FTM1_FLT0	FTM_CLKIN1		LPT0_ALT1		
J11	42	RESET_b	RESET_b	RESET_b								
G11	43	PTB0/ LLWU_P5	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	LCD_P0/ ADC0_SE8/ ADC1_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA	LCD_P0	
G10	44	PTB1	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	LCD_P1/ ADC0_SE9/ ADC1_SE9/ TSIO_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB	LCD_P1	
G9	45	PTB2	LCD_P2/ ADC0_SE12/ TSIO_CH7	LCD_P2/ ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	UART0_RTS_ b			FTM0_FLT3	LCD_P2	
G8	46	PTB3	LCD_P3/ ADC0_SE13/ TSIO_CH8	LCD_P3/ ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	UART0_CTS_ b			FTM0_FLT0	LCD_P3	
D11	47	PTB8	LCD_P8	LCD_P8	PTB8		UART3_RTS_ b				LCD_P8	
E10	48	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_PCS1	UART3_CTS_ b				LCD_P9	
D10	49	PTB10	LCD_P10/ ADC1_SE14	LCD_P10/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1	LCD_P10	

Pinout

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C10	50	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
B10	51	PTB16	LCD_P12/ TSIO_CH9	LCD_P12/ TSIO_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
E9	52	PTB17	LCD_P13/ TSIO_CH10	LCD_P13/ TSIO_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
D9	53	PTB18	LCD_P14/ TSIO_CH11	LCD_P14/ TSIO_CH11	PTB18	CAN0_TX	FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA	LCD_P14	
C9	54	PTB19	LCD_P15/ TSIO_CH12	LCD_P15/ TSIO_CH12	PTB19	CAN0_RX	FTM2_CH1	I2S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
B9	55	PTC0	LCD_P20/ ADC0_SE14/ TSIO_CH13	LCD_P20/ ADC0_SE14/ TSIO_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG	I2S0_TXD			LCD_P20	
D8	56	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSIO_CH14	LCD_P21/ ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0			LCD_P21	
C8	57	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSIO_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1			LCD_P22	
B8	58	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2			LCD_P23	
—	59	VSS	VSS	VSS								
A11	60	VLL3	VLL3	VLL3								
A10	61	VLL2	VLL2	VLL2								
A9	62	VLL1	VLL1	VLL1								
B11	63	VCAP2	VCAP2	VCAP2								
C11	64	VCAP1	VCAP1	VCAP1								
A8	65	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
D7	66	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK		LPT0_ALT2		CMP0_OUT	LCD_P25	
C7	67	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG				LCD_P26	
B7	68	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN					LCD_P27	
A7	69	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8		I2S0_MCLK	I2S0_CLKIN			LCD_P28	
D6	70	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0	LCD_P29	
C6	71	PTC10	LCD_P30/ ADC1_SE6b/ CMP0_IN4	LCD_P30/ ADC1_SE6b/ CMP0_IN4	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
C5	72	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		I2S0_RXD			LCD_P31	

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
D4	73	PTD0/ LLWU_P12	LCD_P40	LCD_P40	PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b				LCD_P40	
D3	74	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b				LCD_P41	
C3	75	PTD2/ LLWU_P13	LCD_P42	LCD_P42	PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX				LCD_P42	
B3	76	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_SIN	UART2_TX				LCD_P43	
A3	77	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4		EWM_IN	LCD_P44	
A2	78	PTD5	LCD_P45/ ADC0_SE6b	LCD_P45/ ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b	FTM0_CH5		EWM_OUT_b	LCD_P45	
B2	79	PTD6/ LLWU_P15	LCD_P46/ ADC0_SE7b	LCD_P46/ ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0	LCD_P46	
A1	80	PTD7	LCD_P47	LCD_P47	PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1	LCD_P47	
L7	—	RESERVED	RESERVED	RESERVED								
K3	—	NC	NC	NC								
H4	—	NC	NC	NC								
F3	—	NC	NC	NC								
H1	—	NC	NC	NC								
H2	—	NC	NC	NC								
J1	—	NC	NC	NC								
J2	—	NC	NC	NC								
J3	—	NC	NC	NC								
H3	—	NC	NC	NC								
K4	—	NC	NC	NC								
H5	—	NC	NC	NC								
J5	—	NC	NC	NC								
H6	—	NC	NC	NC								
J9	—	NC	NC	NC								
J4	—	NC	NC	NC								
H11	—	NC	NC	NC								
F11	—	NC	NC	NC								
E11	—	NC	NC	NC								
F10	—	NC	NC	NC								
F9	—	NC	NC	NC								
F8	—	NC	NC	NC								
E8	—	NC	NC	NC								
B6	—	NC	NC	NC								
A6	—	NC	NC	NC								
A5	—	NC	NC	NC								
B5	—	NC	NC	NC								
D5	—	NC	NC	NC								

Pinout

81 MAP BGA	80 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
C4	—	NC	NC	NC								
B4	—	NC	NC	NC								
A4	—	NC	NC	NC								
B1	—	NC	NC	NC								
C1	—	NC	NC	NC								
D1	—	NC	NC	NC								
E1	—	NC	NC	NC								
C2	—	NC	NC	NC								
D2	—	NC	NC	NC								

8.2 K30 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTD7	PTD5	PTD4	NC	NC	NC	PTC8	PTC4	VLL1	VLL2	VLL3	A
B	NC	PTD6	PTD3	NC	NC	NC	PTC7	PTC3	PTC0	PTB16	VCAP2	B
C	NC	NC	PTD2	NC	PTC11	PTC10	PTC6	PTC2	PTB19	PTB11	VCAP1	C
D	NC	NC	PTD1	PTD0	NC	PTC9	PTC5	PTC1	PTB18	PTB10	PTB8	D
E	NC	PTE2	PTE1	PTE0	VDD	VDD	VDD	NC	PTB17	PTB9	NC	E
F	PTE16	PTE17	NC	PTE3	VDDA	VSSA	VSS	NC	NC	NC	NC	F
G	PTE18	PTE19	VSS	PTE5	VREFH	VREFL	VSS	PTB3	PTB2	PTB1	PTB0	G
H	NC	NC	NC	NC	NC	NC	PTE4	PTA1	PTA3	PTA17	NC	H
J	NC	NC	NC	NC	NC	PTA0	PTA2	PTA4	NC	PTA16	RESET_b	J
K	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	NC	NC	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	VBAT	PTA5	PTA12	PTA14	VSS	PTA19	K
L	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	XTAL32	EXTAL32	VSS	RESERVED	PTA13	PTA15	VDD	PTA18	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 25. K30 81 MAPBGA Pinout Diagram

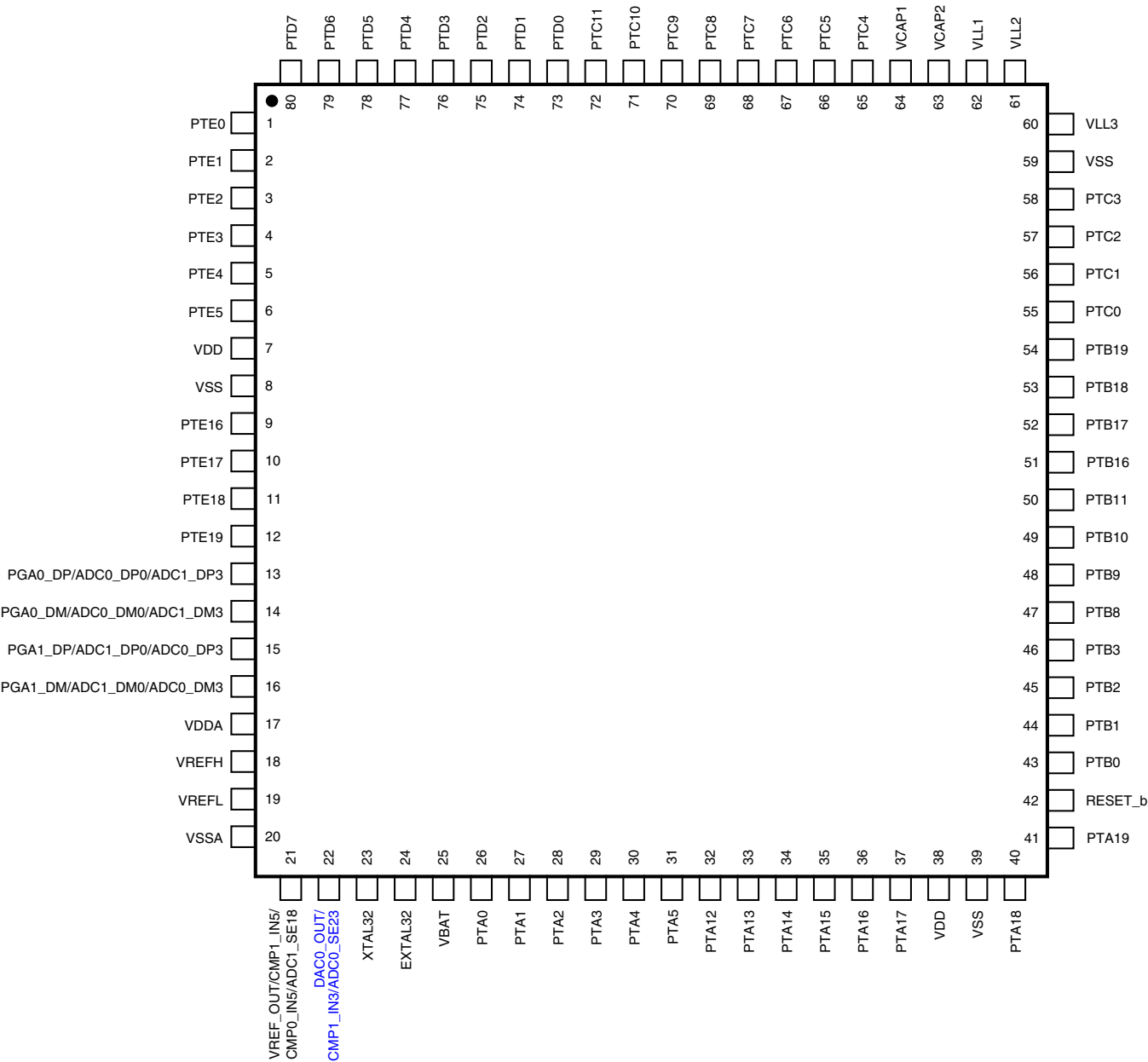


Figure 26. K30 80 LQFP Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 48. Revision History

Rev. No.	Date	Substantial Changes
1	11/2010	Initial public revision

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	3/2011	Many updates throughout Corrected 81- and 104-pin package codes
3	3/2011	Added sections that were inadvertently removed in previous revision
4	3/2011	Reworded I_{IC} footnote in "Voltage and Current Operating Requirements" table. Added paragraph to "Peripheral operating requirements and behaviors" section. Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.
5	6/2011	• Changed supported part numbers per new part number scheme • Changed <i>DC injection current</i> specs in "Voltage and current operating requirements" table • Changed <i>Input leakage current</i> and <i>internal pullup/pulldown resistor</i> specs in "Voltage and current operating behaviors" table • Split <i>Low power stop mode current</i> specs by temperature range in "Power consumption operating behaviors" table • Changed typical I_{DD_VBAT} spec in "Power consumption operating behaviors" table • Added LPTMR clock specs to "Device clock specifications" table • Changed <i>Minimum external reset pulse width</i> in "General switching specifications" table • Changed <i>PLL operating current</i> in "MCG specifications" table • Added footnote to <i>PLL period jitter</i> in "MCG specifications" table • Changed <i>Supply current</i> in "Oscillator DC electrical specifications" table • Changed <i>Crystal startup time</i> in "Oscillator frequency specifications" table • Changed <i>Operating voltage</i> in "EzPort switching specifications" table • Changed <i>ADC asynchronous clock source</i> specs in "16-bit ADC characteristics" table • Changed <i>Gain</i> spec in "16-bit ADC with PGA characteristics" table • Added typical <i>Input DC current</i> to "16-bit ADC with PGA characteristics" table • Changed <i>Input offset voltage</i> and <i>ENOB</i> notes field in "16-bit ADC with PGA characteristics" table • Changed <i>Analog comparator initialization delay</i> in "Comparator and 6-bit DAC electrical specifications" • Changed <i>Code-to-code settling time</i>, <i>DAC output voltage range low</i>, and <i>Temperature coefficient offset voltage</i> in "12-bit DAC operating behaviors" table • Changed <i>Temperature drift</i> and <i>Load regulation</i> in "VREF full-range operating behaviors" table • Changed <i>DSPI_SCK cycle time</i> specs in "DSPI timing" tables • Changed <i>DSPI_SS</i> specs in "Slave mode DSPI timing (low-speed mode)" table • Changed <i>DSPI_SCK to DSPI_SOUT valid</i> spec in "Slave mode DSPI timing (high-speed mode)" table • Changed <i>Reference oscillator current source base current</i> spec and added <i>Low-power current adder</i> footer in "TSI electrical specifications" table • Added <i>LCD glass capacitance</i> footnote

Table continues on the next page...

Table 48. Revision History (continued)

Rev. No.	Date	Substantial Changes
6	01/2012	- Added AC electrical specifications. - Replaced TBDs with silicon data throughout. - In "Power mode transition operating behaviors" table, removed entry times. - Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. - Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". - Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. - Updated I_{DD_RUN} numbers in 'Power consumption operating behaviors' section. - Clarified 'Diagram: Typical I_{DD_RUN} operating behavior' section and updated 'Run mode supply current vs. core frequency — all peripheral clocks disabled' figure. - In 'Voltage reference electrical specifications' section, updated C_L, V_{tdrift}, and V_{vdift} values. - In 'LCD electrical characteristics' section, updated V_{IREG} and Δ_{RTRIM} values.
7	02/2013	- In "ESD handling ratings", added a note for I_{LAT}. - Updated "Voltage and current operating requirements". - Updated "Voltage and current operating behaviors". - Updated "Power mode transition operating behaviors". - Updated "EMC radiated emissions operating behaviors" to add MAPBGA data. - In "MCG specifications", updated the description of f_{ints_t}. - In "16-bit ADC operating conditions", updated the max spec of V_{ADIN}. - In "16-bit ADC electrical characteristics", updated the temp sensor slope and voltage specs. - Updated "I2C switching specifications". - In "SDHC specifications", removed the operating voltage limits and updated the SD1 and SD6 specs. - In "I2S switching specifications", added separate specification tables for the full operating voltage range.

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