

T-46-09-05 00

**9300
93H00
93L00
93S00**

4-BIT UNIVERSAL SHIFT REGISTER

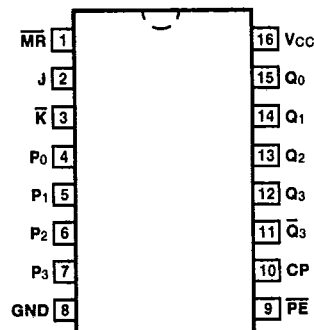
DESCRIPTION — The '00 is a 4-bit universal shift register. As a high speed multifunctional sequential logic block, it is useful in a wide variety of register and counter applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

- **ASYNCHRONOUS MASTER RESET**
- **J, K INPUTS TO FIRST STAGE**

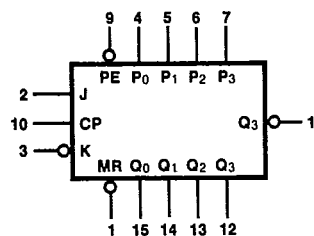
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	9300PC, 93H00PC 93L00PC, 93S00PC		9B
Ceramic DIP (D)	A	9300DC, 93H00DC 93L00DC, 93S00DC	9300DM, 93H00DM 93L00DM, 93S00DM	6B
Flatpak (F)	A	9300FC, 93H00FC 93L00FC, 93S00FC	9300FM, 93H00FM 93L00FM, 93S00FM	4L

**CONNECTION DIAGRAM
PINOUT A**



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

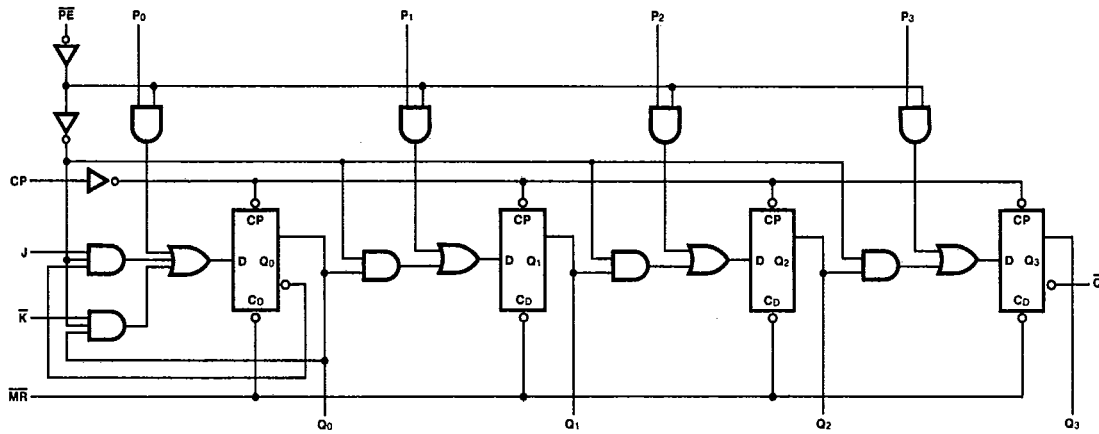
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93H (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
PE	Parallel Enable Input (Active LOW)	2.3/2.3	1.0/1.0	1.15/0.575	1.25/1.25
P ₀ — P ₃	Parallel Inputs	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
J	First Stage J Input (Active HIGH)	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
K	First Stage K Input (Active LOW)	1.0/1.0	1.0/1.0	0.5/0.25	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	2.0/2.0	1.0/0.5	2.5/2.5
MR	Master Reset Input	1.0/1.0	1.0/1.0	0.5/0.25	1.25/1.25
Q ₀ — Q ₃	Parallel Outputs	12/6.0	16/8.0	10/5.0 (3.0)	25/12.5
Q ₃ -bar	Complementary Last Stage Output	16/8.0	20/10	10/5.0 (3.0)	25/12.5

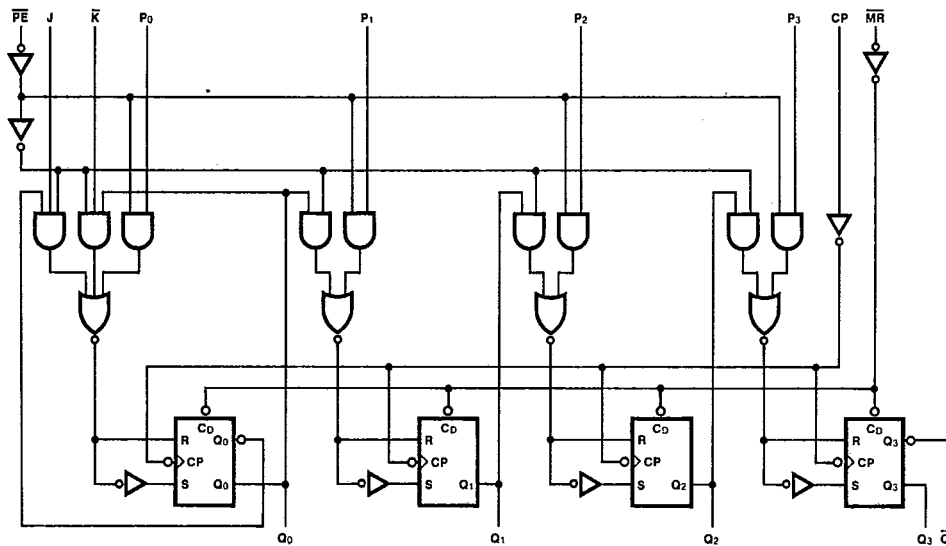
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LOGIC DIAGRAMS
'00, 'H00, 'L00



'S00



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FUNCTIONAL DESCRIPTION — The Logic Diagrams and Truth Table indicate the functional characteristics of the '00 4-bit shift register. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers.

The '00 has two primary modes of operation, shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ input is HIGH, serial data enters the first flip-flop Q_0 via the J and $\overline{K}$ inputs and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The $J\overline{K}$ inputs provide the flexibility of the JK type input for special applications, and the simple D-type input for general applications by tying the two pins together. When the $\overline{PE}$ input is LOW, the '00 appears as four common clocked D flip-flops. The data on the parallel inputs $P_0 - P_3$ is transferred to the respective $Q_0 - Q_3$ outputs following the LOW-to-HIGH clock transition. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the P_{n-1} inputs and holding the $\overline{PE}$ input LOW.

All serial and parallel data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. Since the '00 utilizes edge triggering, there is no restriction on the activity of the J, K, P_n and $\overline{PE}$ inputs for logic operation — except for the setup and release time requirements. A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition.

TRUTH TABLE

OPERATING MODE	INPUTS ($\overline{MR} = H$)							OUTPUTS @ $t_n + 1$				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
SHIFT MODE	H	L	L	X	X	X	X	L	Q_0	Q_1	Q_2	$\overline{Q_2}$
	H	L	H	X	X	X	X	Q_0	Q_0	Q_1	Q_2	$\overline{Q_2}$
	H	H	L	X	X	X	X	$\overline{Q_0}$	Q_0	Q_1	Q_2	$\overline{Q_2}$
	H	H	H	X	X	X	X	H	Q_0	Q_1	Q_2	$\overline{Q_2}$
PARALLEL ENTRY MODE	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

* $t_n + 1$ = Indicates state after next LOW-to-HIGH clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		93XX		93H		93L		93S		UNITS	CONDITIONS
			Min	Max	Min	Max	Min	Max	Min	Max		
Ios	Output Short Circuit Current		-20	-80	-30	-100					mA	Vcc = Max, VOUT = 0 V
Icc	Power Supply Current	XC	92		112		23		120		mA	Vcc = Max
		XM	86		102							

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93H		93L		93S		UNITS	CONDITIONS
		C _L = 15 pF		C _L = 15 pF		C _L = 15 pF		C _L = 15 pF			
		Min	Max	Min	Max	Min	Max	Min	Max		
f _{max}	Maximum Shift Frequency	30		45		10		70		MHz	Figs. 3-1, 3-8
t _{PLH}	Propagation Delay CP to Q _n	22		16		35		8.5		ns	Figs. 3-1, 3-8
t _{PHL}	CP to Q _n	26		21		51		12			
t _{PHL}	Propagation Delay MR to Q _n	40		28		60		23		ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	93XX		93H		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max	Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW, J, $\bar{K}$ and P ₀ — P ₃ to CP	20		12		60		6.0		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW, J, $\bar{K}$ and P ₀ — P ₃ to CP	0		0		0		0		ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW, $\bar{P}_E$ to CP	39		15		68		8.0		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW, $\bar{P}_E$ to CP	-10		0		-20		0		ns	
t _w (H) t _w (L)	CP Pulse Width HIGH or LOW	17		12		38		7.0		ns	Fig. 3-8
t _w (L)	$\bar{MR}$ Pulse Width LOW	25		19		53		12		ns	Fig. 3-16
t _{rec}	Recovery Time $\bar{MR}$ to CP	25		7.0		70		5.0		ns	

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