RL78/L12

RENESAS MCU

R01DS0157EJ0100
Rev.1.00
2013.01.31

Integrated LCD controller/driver, True Low Power Platform (as low as 62.5 μA/MHz, and 0.64 μA for RTC + LVD), 1.6 V to 5.5 V operation, 8 to 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All LCD Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA, (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.64 μA
- Supports snooze
- Operating: 62.5 μA/MHz
- LCD operating current (Capacitor split method): 0.12 μA
- LCD operating current (Internal voltage boost method): 0.63 μA (V_{DD} = 3.0 V)

16-bit RL78 CPU Core
- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory
- Density: 8 KB to 32 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with flash shield window function

Data Flash Memory
- Data flash with background operation
- Data flash size: 2 KB size
- Erase cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM
- 1 KB and 1.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 24 MHz with +/– 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (–20°C to 85°C)
- Pre-configured settings: 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz & 1 MHz

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

LCD Controller/Driver
- Up to 35 seg x 8 com or 39 seg x 4 com
- Supports capacitor split method, internal voltage boost method and resistance division method
- Supports waveform types A and B
- Supports LCD contrast adjustment (16 steps)
- Supports LCD blinking

Data Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 1 × I^2C multi-master
- Up to 2 × CSI/SPI (7-, 8-bit)
- Up to 1 × UART (7-, 8-, 9-bit)
- Up to 1 × LIN

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog
- ADC: Up to 10 channels, 10-bit resolution, 2.1 μs conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock frequency detection
- ADC self-test

General Purpose I/O
- 5V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Standard: –40 °C to +85 °C

Package Type and Pin Count
From 7mm x 7mm to 12mm x 12mm
QFP: 32, 44, 48, 52, 64
QFN: 64

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/L12				
			32 pins	44 pins	48 pins	52 pins	64 pins
32 KB	2 KB	1.5 KB[Note]	R5F10RBC	R5F10RFC	R5F10RGC	R5F10RJC	R5F10RLC
16 KB	2 KB	1 KB[Note]	R5F10RBA	R5F10RFA	R5F10RGA	R5F10RJA	R5F10RLA
8KB	2 KB	1 KB[Note]	R5F10RB8	R5F10RF8	R5F10RG8	R5F10RJ8	–

Note In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 Ordering Information

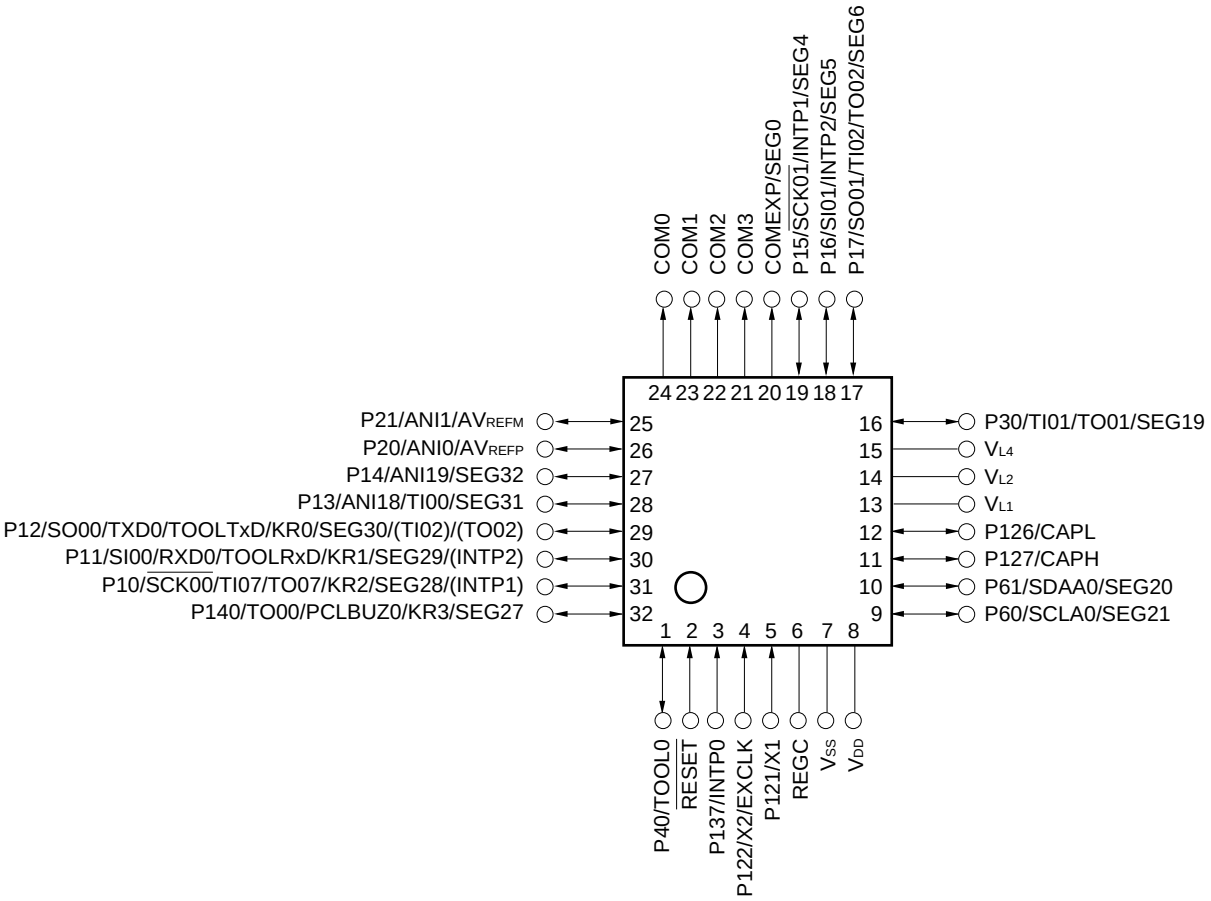
- **Flash memory version (lead-free product)**

Pin count	Package	Part Number
32 pins	32-pin plastic LQFP (7 × 7)	R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP
44 pins	44-pin plastic LQFP (10 × 10)	R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB
52 pins	52-pin plastic LQFP (10 × 10)	R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA
64 pins	64-pin plastic WQFN (8 × 8)	R5F10RLAANB, R5F10RLCANB
	64-pin plastic LQFP (fine pitch) (10 × 10)	R5F10RLAAFB, R5F10RLCAFB
	64-pin plastic LQFP (12 × 12)	R5F10RLAAFA, R5F10RLCAFA

1.3 Pin Configuration (Top View)

1.3.1 32-pin products

- 32-pin plastic LQFP (7 × 7)



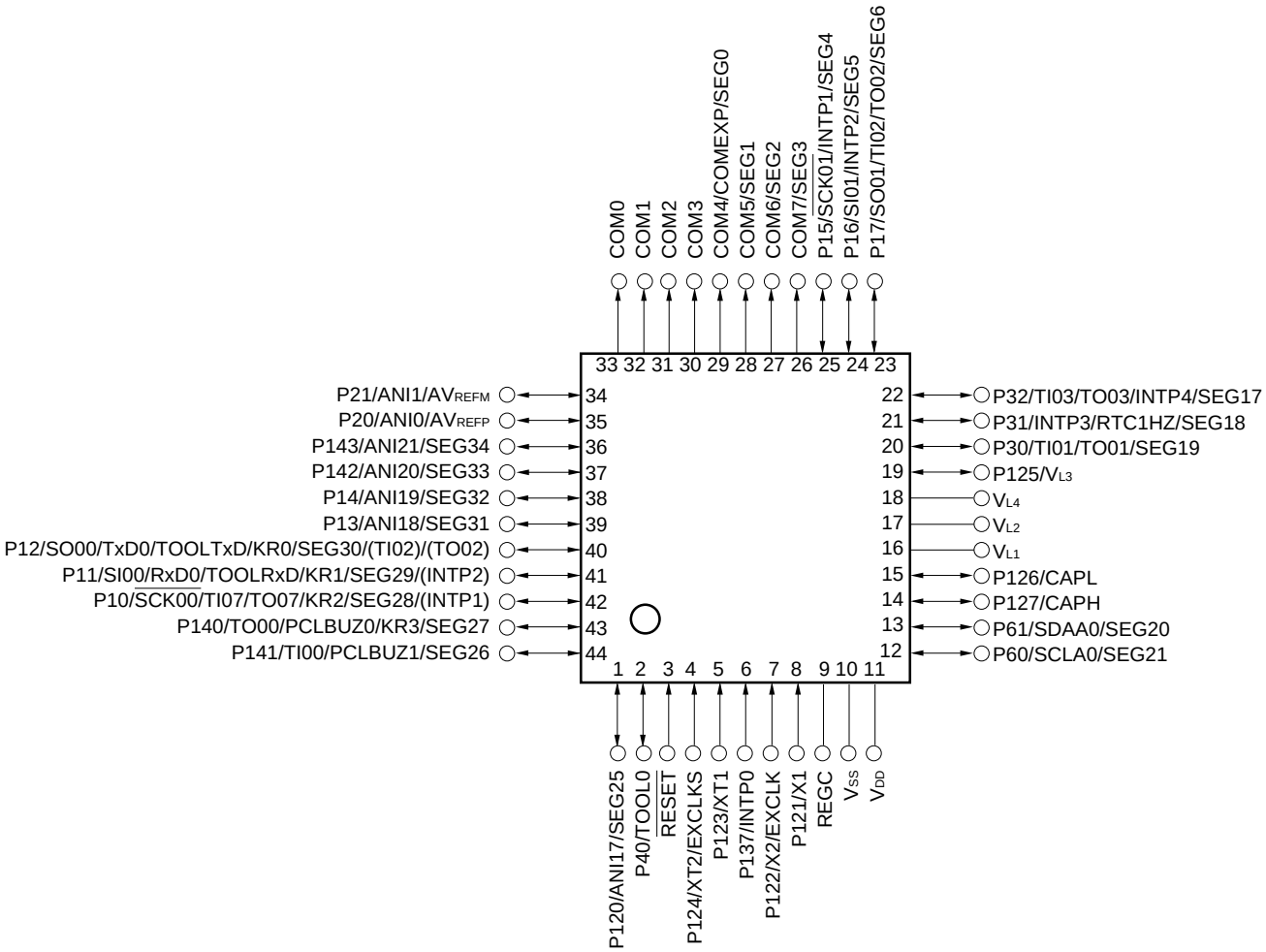
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.3.2 44-pin products

- 44-pin plastic LQFP (10 × 10)



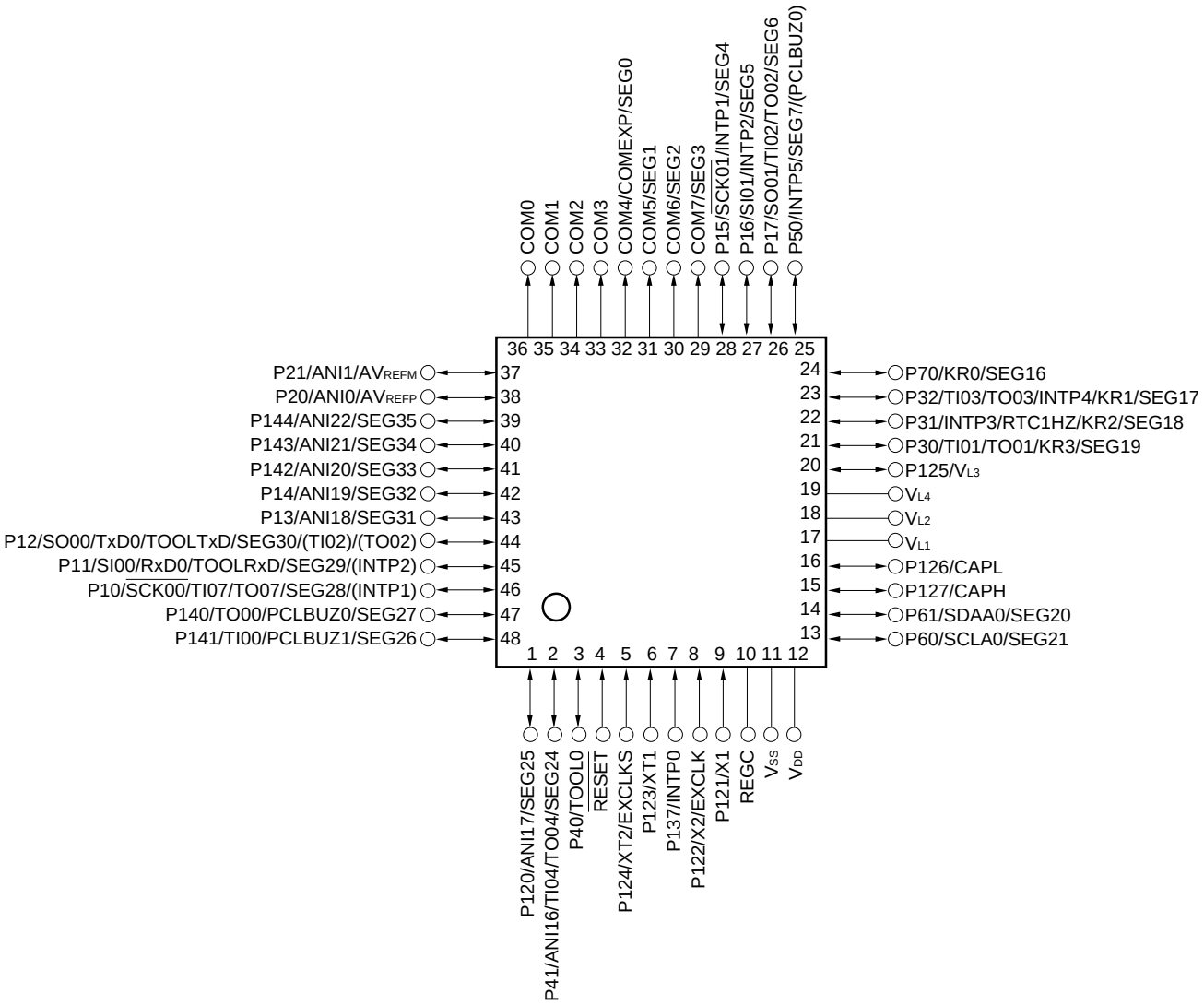
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.3.3 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)



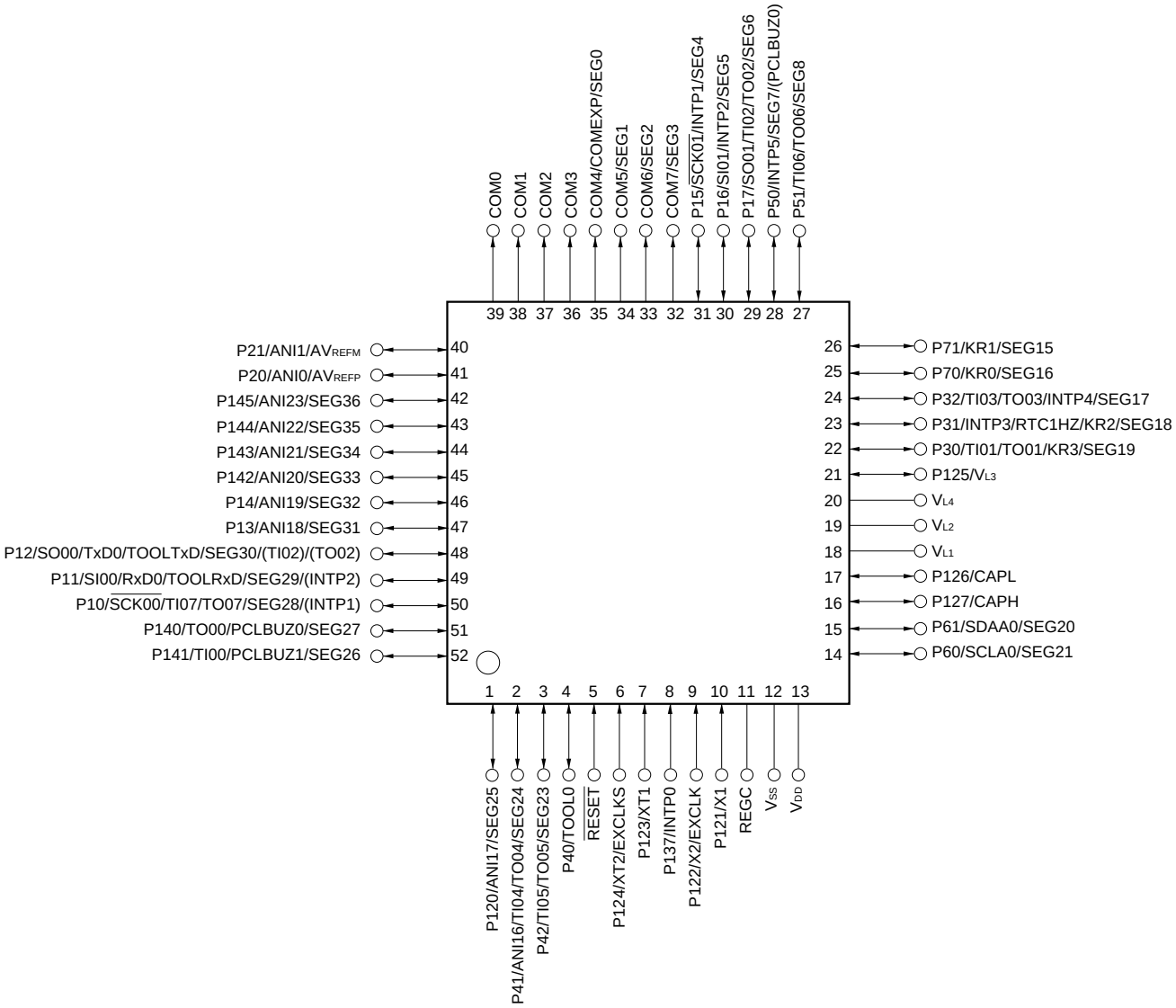
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.3.4 52-pin products

- 52-pin plastic LQFP (10 × 10)



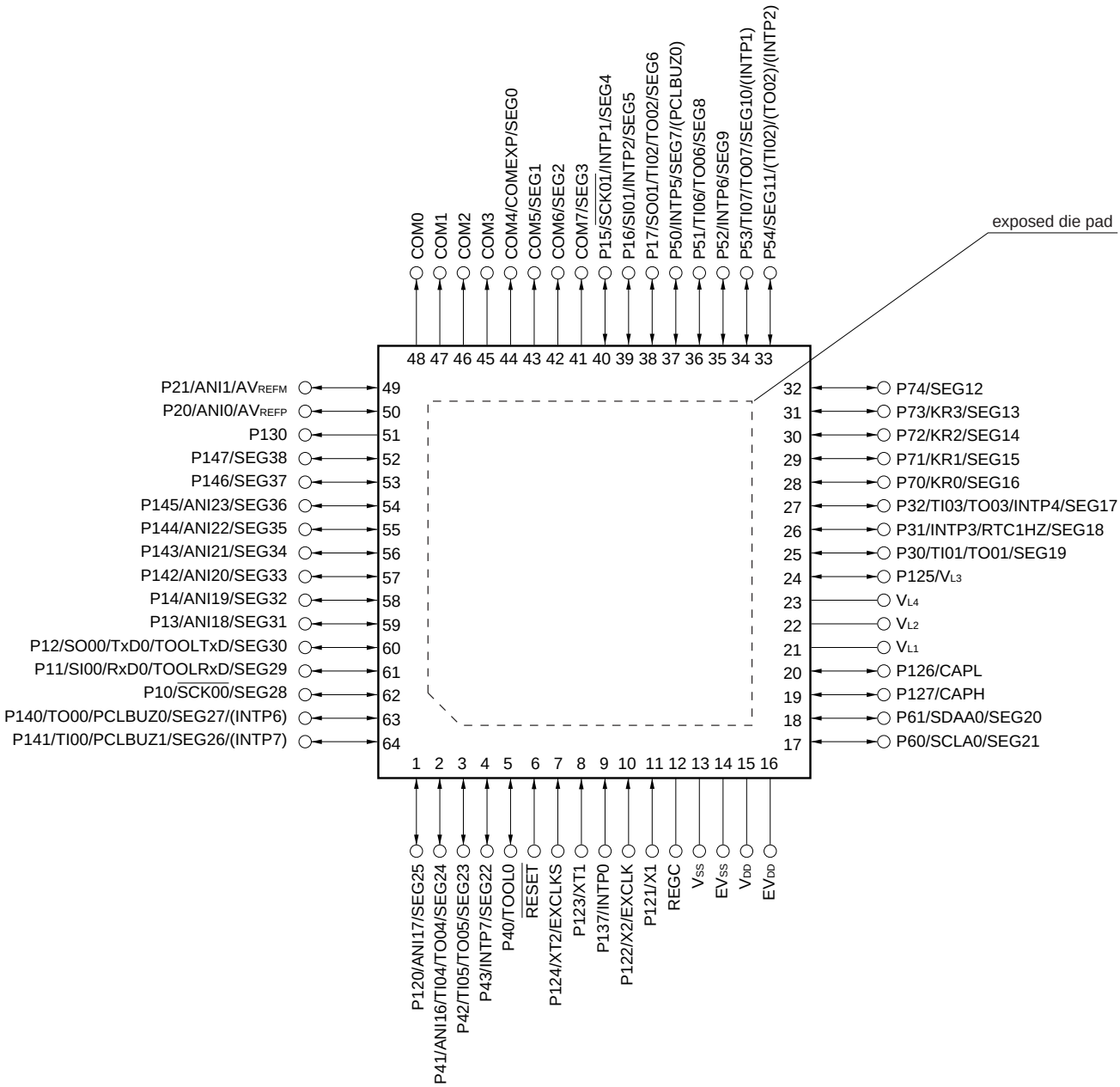
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.3.5 64-pin products

- 64-pin plastic WQFN (8 × 8)



Cautions 1. Make EV_{SS} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the same potential as EV_{DD} pin.

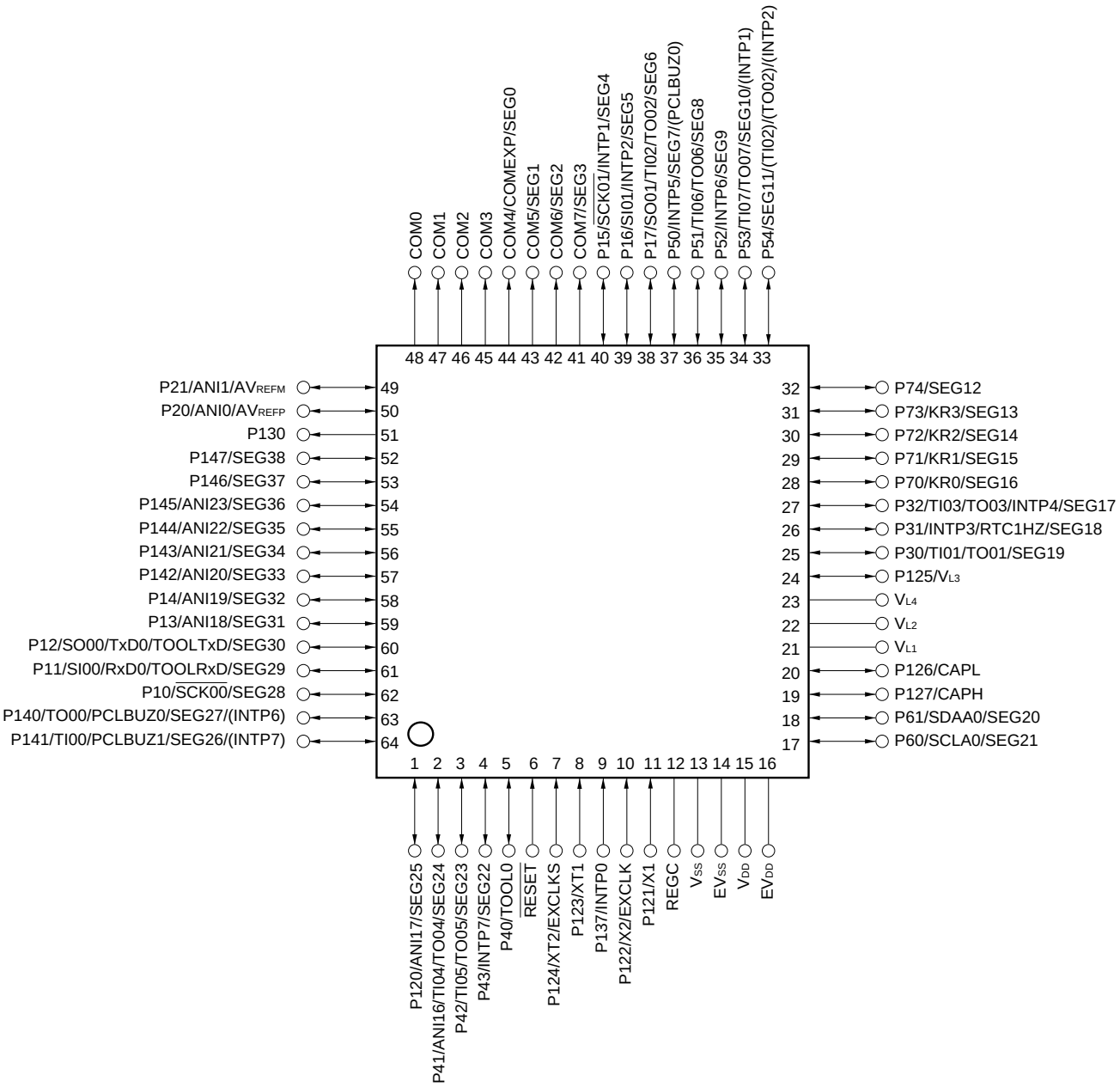
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic LQFP (12 × 12)



Cautions 1. Make EV_{SS} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the same potential as EV_{DD} pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD} pins and connect the V_{SS} and EV_{SS} pins to separate ground lines.

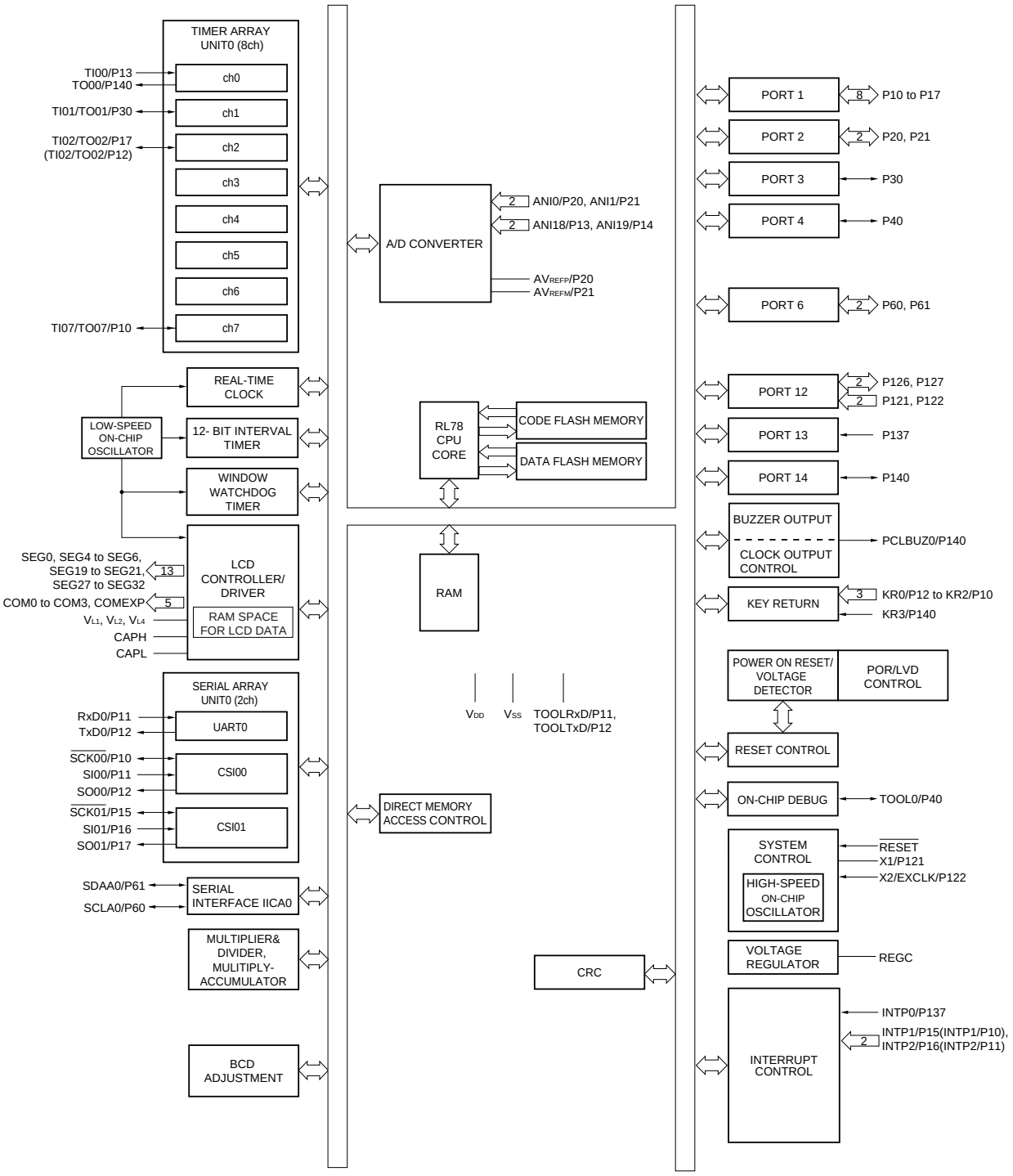
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.4 Pin Identification

ANI0, ANI1, ANI16 to ANI23:	Analog Input
AV_{REFM}:	Analog Reference Voltage Minus
AV_{REFP}:	Analog Reference Voltage Plus
CAPH, CAPL:	Capacitor for LCD
COM0 to COM7, COMEXP:	LCD Common Output
EV_{DD}:	Power Supply for Port
EV_{SS}:	Ground for Port
EXCLK:	External Clock Input (Main System Clock)
EXCLKS:	External Clock Input (Subsystem Clock)
INTP0 to INTP7:	Interrupt Request From Peripheral
KR0 to KR3:	Key Return
P10 to P17:	Port 1
P20, P21:	Port 2
P30 to P32:	Port 3
P40 to P43:	Port 4
P50 to P54:	Port 5
P60, P61:	Port 6
P70 to P74:	Port 7
P120 to P127:	Port 12
P130, P137:	Port 13
P140 to P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
REGC:	Regulator Capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
RxD0:	Receive Data
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$:	Serial Clock Input/Output
SCLA0:	Serial Clock Input/Output
SDAA0:	Serial Data Input/Output
SEG0 to SEG38:	LCD Segment Output
SI00, SI01:	Serial Data Input
SO00, SO01:	Serial Data Output
TI00 to TI07:	Timer Input
TO00 to TO07:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0:	Transmit Data
V_{DD}:	Power Supply
V_{L1} to V_{L4}:	LCD Power Supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

1.5.1 32-pin products



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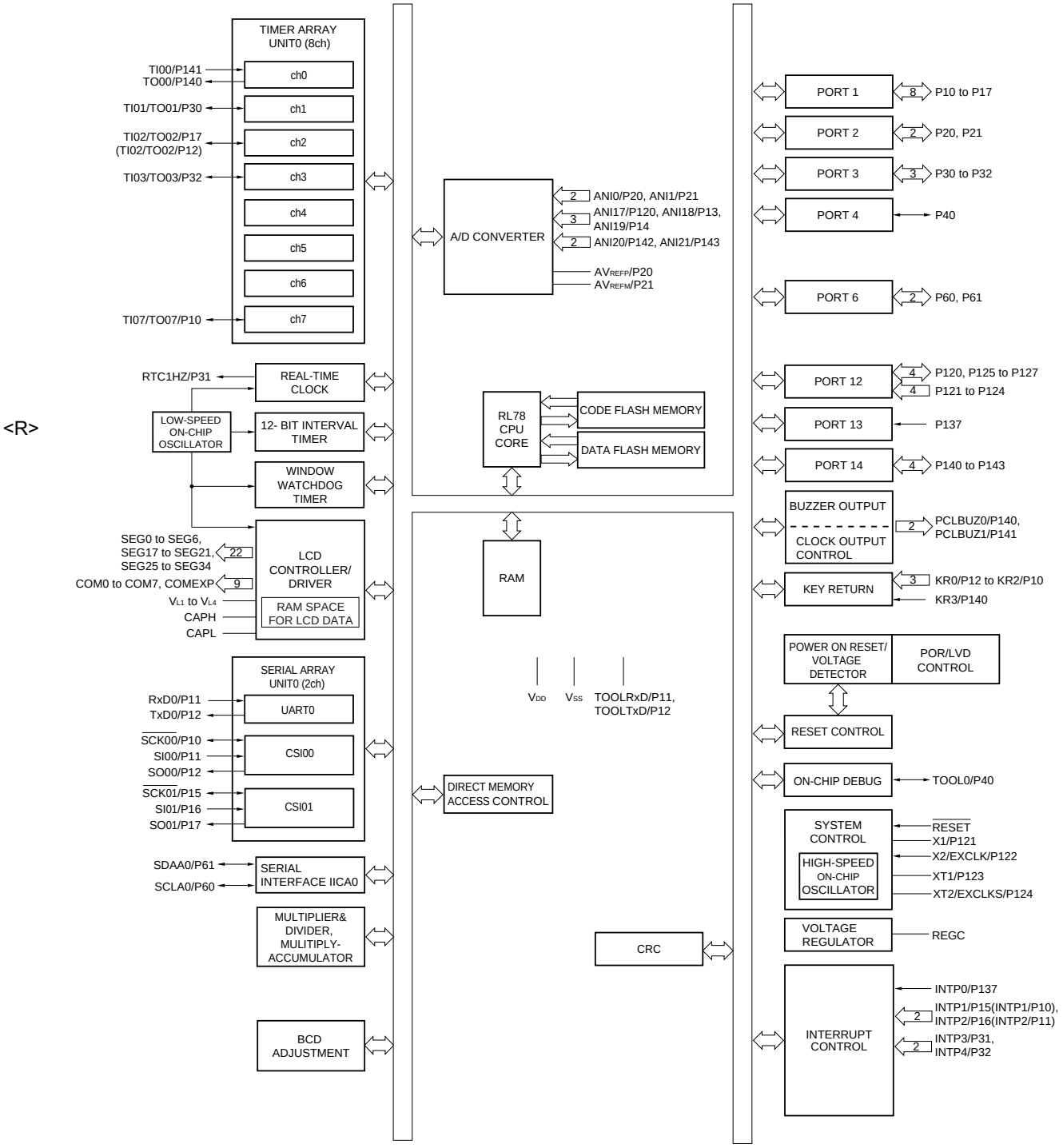
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.2 44-pin products



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Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.3 48-pin products

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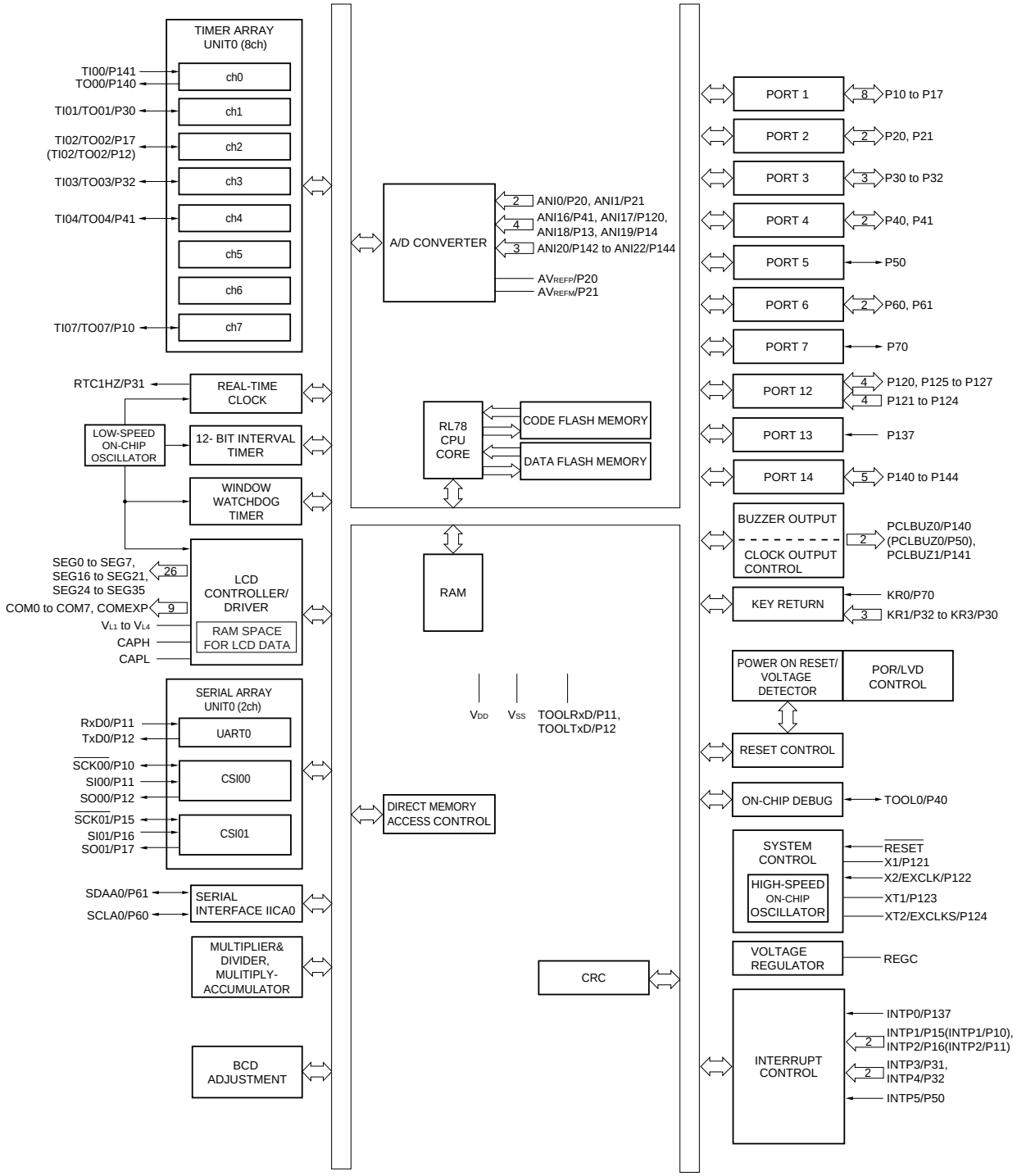

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.4 52-pin products

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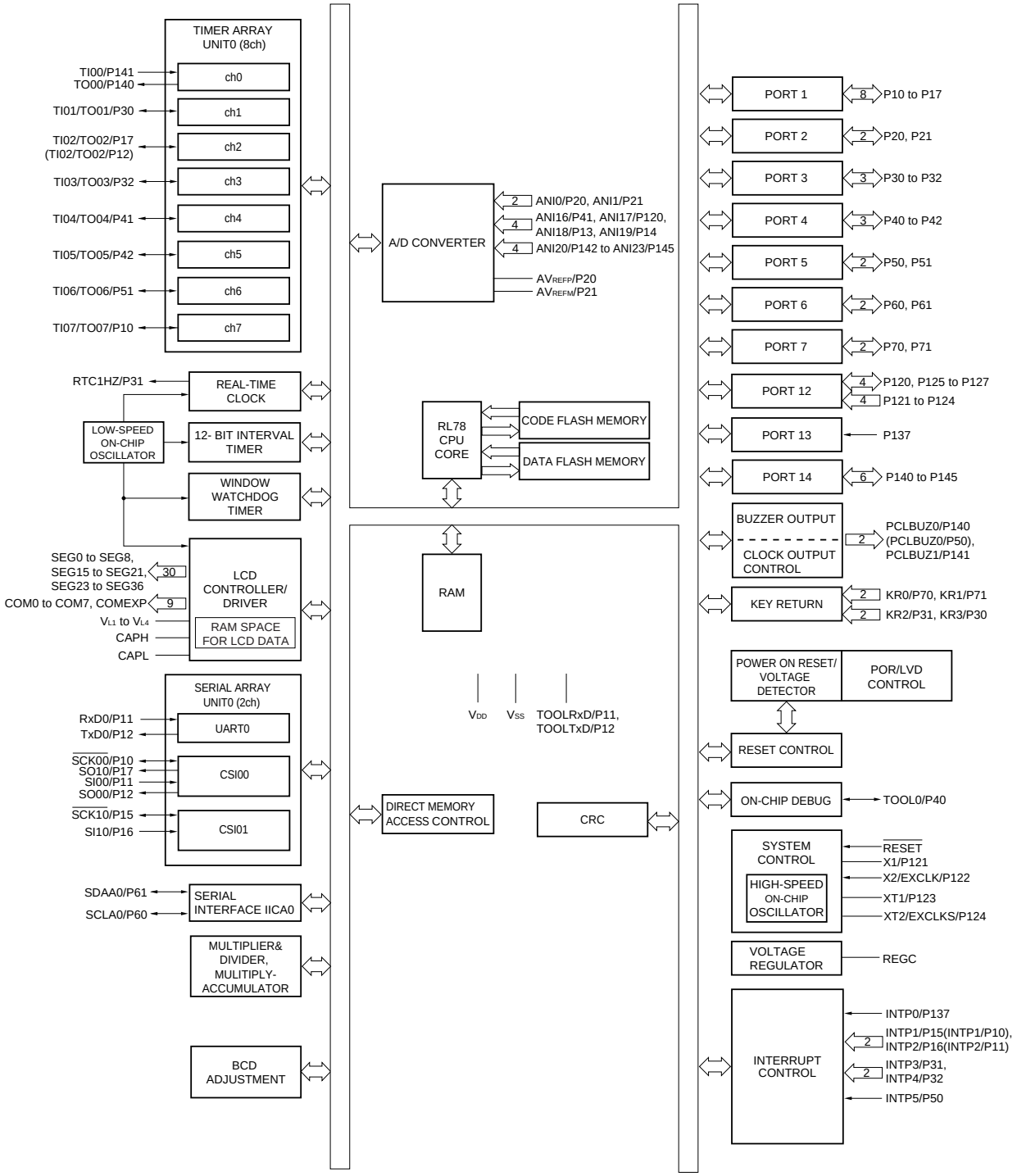
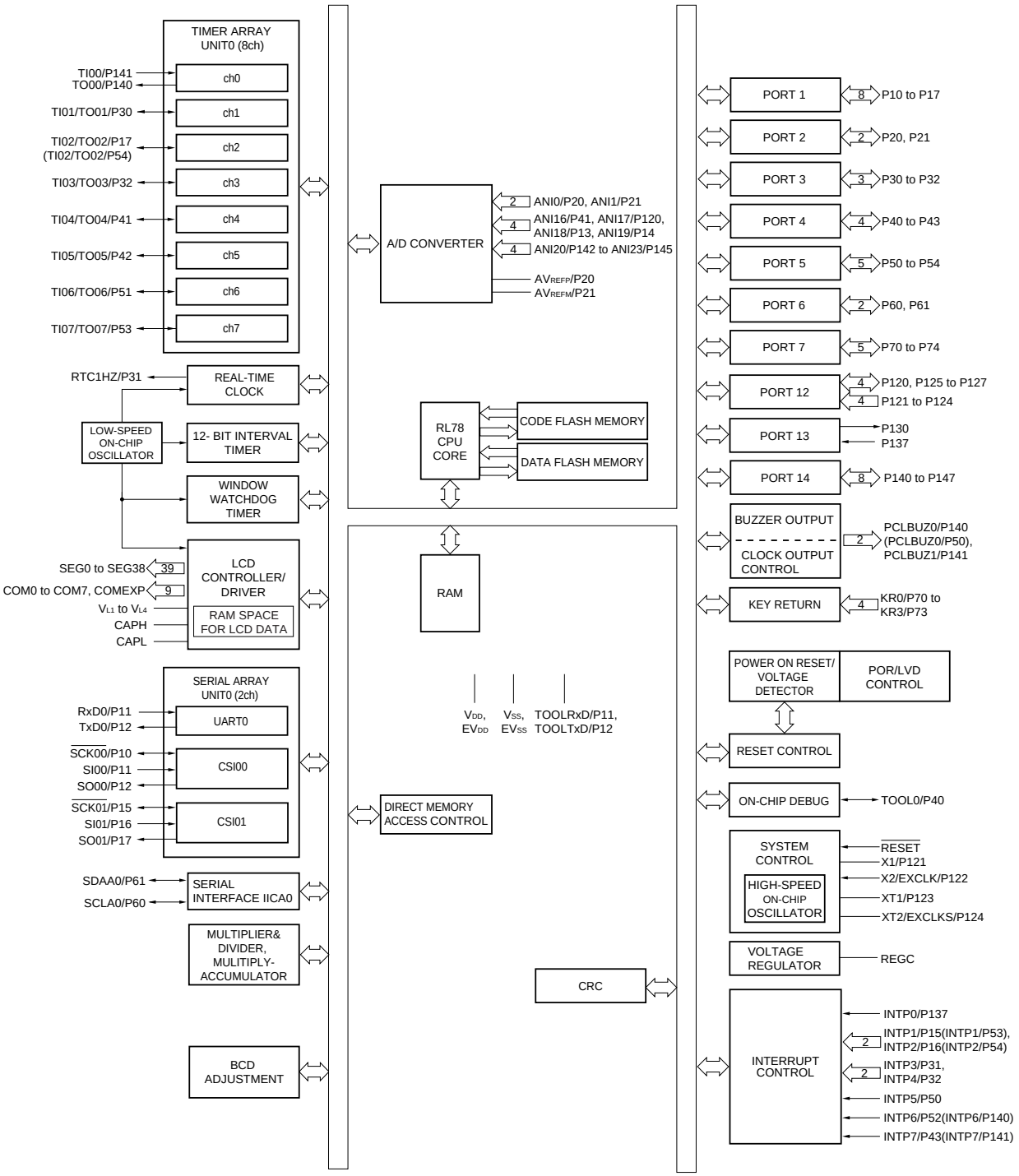


Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.5.5 64-pin products



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Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR)

1.6 Outline of Functions

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Code flash memory (KB)		8 to 32	8 to 32	8 to 32	8 to 32	16, 32
Data flash memory (KB)		2	2	2	2	2
RAM (KB)		1, 1.5 Note 1	1, 1.5 Note 1	1, 1.5 Note 1	1, 1.5 Note 1	1, 1.5 Note 1
Memory space		1 MB				
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V				
	High-speed on-chip oscillator clock	HS (high-speed main) operation: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) operation: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (low-speed main) operation: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (low-voltage main) operation: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)				
Subsystem clock		–	XT1 (crystal) oscillation , external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.6 to 5.5 V			
Low-speed on-chip oscillator clock		Internal oscillation 15 kHz (TYP.): V_{DD} = 1.6 to 5.5 V				
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)				
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)				
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)				
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.				
I/O port	Total	20	29	33	37	47
	CMOS I/O	15	22	26	30	39
	CMOS input	3	5	5	5	5
	CMOS output	–	–	–	–	1
	N-ch open-drain I/O (EV_{DD} tolerance)	2	2	2	2	2
Timer	16-bit timer	8 channels	8 channels (with 1 channel remote control output function)			
	Watchdog timer	1 channel				
	Real-time clock (RTC)	1 channel				
	12-bit interval timer (IT)	1 channel				
	Timer output	4 channels (PWM outputs: 3 Note 2)	5 channels (PWM outputs: 4 Note 2)	6 channels (PWM outputs: 5 Note 2)	8 channels (PWM outputs: 7 Note 2)	
	RTC output	–	1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz or)			

Notes 1. In the case of the 1 KB, and 1.5 KB, this is 630 bytes when the self-programming function and data flash function is used.

<R> **2.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

(2/2)

Item		32-pin	44-pin	48-pin	52-pin	64-pin
		R5F10RBx	R5F10RFx	R5F10RGx	R5F10RJx	R5F10RLx
Clock output/buzzer output		1	2			
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)				
8/10-bit resolution A/D converter		4 channels	7 channels	9 channels	10 channels	10 channels
Serial interface		• CSI: 2 channel/UART (LIN-bus supported): 1 channel				
	I^2C bus	1 channel	1 channel	1 channel	1 channel	1 channel
LCD controller/driver		Internal voltage boosting method, capacitor split method, and external resistance division method are switchable.				
	Segment signal output	13	22 (18) Note 1	26 (22) Note 1	30 (26) Note 1	39 (35) Note 1
	Common signal output	4	4 (8) Note 1			
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)				
DMA controller		2 channels				
Vectored interrupt sources	Internal	23	23	23	23	23
	External	4	6	7	7	9
Key interrupt		4				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access				
<R> Power-on-reset circuit		• Power-on-reset: 1.51 ±0.04 V • Power-down-reset: 1.50 ±0.04 V				
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 1.6 to 5.5 V				
Operating ambient temperature		T_A = –40 to +85 °C				

Notes 1. The values in parentheses are the number of signal outputs when 8 com is used.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R> 2. ELECTRICAL SPECIFICATIONS

Cautions 1. The RL78/L12 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

<R> **2. With products not provided with an EV_{DD}, or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.**

3. The pins mounted depend on the product. Refer to 1.3.1 32-pin products to 1.3.5 64-pin products.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/3)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	EV_{DD}	V_{DD} = EV_{DD}	−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I3}	P20, P21, P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20, P21	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI23	−0.3 to EV_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V
	V_{AI2}	ANI0, ANI1	−0.3 to V_{DD} +0.3 and −0.3 to $AV_{REF(+)}$ +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF(+)}$: + side reference voltage of the A/D converter.

Absolute Maximum Ratings (T_A = 25°C) (2/3)

Parameter	Symbols	Conditions	Ratings	Unit
<R> LCD voltage	V_{L1}	V_{L1} voltage[Note]	–0.3 to +2.8	V
	V_{L2}	V_{L2} voltage[Note]	–0.3 to +6.5	V
	V_{L3}	V_{L3} voltage[Note]	–0.3 to +6.5	V
	V_{L4}	V_{L4} voltage[Note]	–0.3 to +6.5	V
	V_{L5}	CAPL, CAPH voltage[Note]	–0.3 to +6.5	V
	V_{L6}	COM0 to COM7, SEG0 to SEG38, COMEXP output voltage	–0.3 to +6.5	V

<R> **Note** This value only indicates the absolute maximum ratings when applying voltage to the V_{L1}, V_{L2}, V_{L3}, and V_{L4} pins; it does not mean that applying voltage to these pins is recommended. When using the internal voltage boosting method or capacitance split method, connect these pins to V_{SS} via a capacitor (0.47 μF ± 30%) and connect a capacitor (0.47 μF ± 30%) between the CAPL and CAPH pins.

<R> **Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Absolute Maximum Ratings (T_A = 25°C) (3/3)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	−70	mA
			P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127	−100	mA
	I_{OH2}	Per pin	P20, P21	−0.5	mA
		Total of all pins		−1	mA
Output current, low	I_{OL1}	Per pin	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P10 to P14, P40 to P43, P120, P130, P140 to P147	70	mA
			P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127	100	mA
	I_{OL2}	Per pin	P20, P21	1	mA
		Total of all pins		2	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

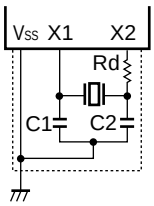
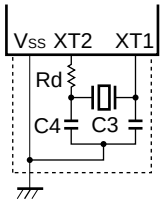
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

<R> 2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	MHz
			1.6 V ≤ V_{DD} <1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator			32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to **2.4 AC Characteristics** for instruction execution time.

Cautions 1. When using the X1 oscillator, XT1 oscillator,wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

3. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1	f_{IH}			1		24	MHz
High-speed on-chip oscillator clock frequency accuracy Note 2		–20 to +85 °C	1.8 V≤V_{DD}≤5.5 V	–1		+1	%
			1.6 V≤V_{DD}≤1.8 V	–5		+5	%
		–40 to –20 °C	1.8 V≤V_{DD}≤5.5 V	–1.5		+1.5	%
			1.6 V≤V_{DD}≤1.8 V	–5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to **2.4 AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(1/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147					–10.0 [Note 3]	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70%[Note 2])		4.0 V ≤ EV_{DD} ≤ 5.5 V			–40.0	mA
				2.7 V ≤ EV_{DD} < 4.0 V			–8.0	mA
				1.8 V ≤ EV_{DD} < 2.7 V			–4.0	mA
				1.6 V ≤ EV_{DD} < 1.8 V			–2.0	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P70 to P74, P125 to P127 (When duty = 70%[Note 2])		4.0 V ≤ EV_{DD} ≤ 5.5 V			–60.0	mA
				2.7 V ≤ EV_{DD} < 4.0 V			–15.0	mA
				1.8 V ≤ EV_{DD} < 2.7 V			–8.0	mA
				1.6 V ≤ EV_{DD} < 1.8 V			–4.0	mA
		Total of all pins (When duty = 70%[Note 2])					–100.0	mA
	I_{OH2}	P20, P21	Per pin				–0.1[Note 3]	mA
			Total of all pins (When duty = 70%[Note 2])	1.6 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD}, EV_{DD} pins to an output pin.

2. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 50% and I_{OH} = –10.0 mA
  Total output current of pins = (–10.0 × 0.7)/(50 × 0.01) = –14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Do not exceed the total current value.

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(2/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147					20.0 [Note 3]	mA
		Per pin for P60, P61					15.0 [Note 3]	mA
		Total of P10 to P14, P40 to P43, P120, P130, P140 to P147 (When duty = 70% [Note 2])		4.0 V ≤ EV_{DD} ≤ 5.5 V			70.0	mA
				2.7 V ≤ EV_{DD} < 4.0 V			15.0	mA
				1.8 V ≤ EV_{DD} < 2.7 V			9.0	mA
				1.6 V ≤ EV_{DD} < 1.8 V			4.5	mA
		Total of P15 to P17, P30 to P32, P50 to P54, P60, P61, P70 to P74, P125 to P127 (When duty = 70% [Note 2])		4.0 V ≤ EV_{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ EV_{DD} < 4.0 V			35.0	mA
				1.8 V ≤ EV_{DD} < 2.7 V			20.0	mA
				1.6 V ≤ EV_{DD} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70% [Note 2])					150.0	mA
	I_{OL2}	P20, P21	Per pin for				0.4 [Note 3]	mA
			Total of all pins (When duty = 70% [Note 2])	1.6 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS} and V_{SS} pin.

2. Specification under conditions where the duty factor is 70%.

The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(50 × 0.01) = 14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

3. Do not exceed the total current value.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(3/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	2.2		EV_{DD}	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	2.0		EV_{DD}	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	1.50		EV_{DD}	V
	V_{IH3}	P20, P21		0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60, P61		0.7EV_{DD}		EV_{DD}	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV_{DD}	V
	V_{IL2}	P10, P11, P15, P16	TTL input buffer 4.0 V ≤ EV_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD} < 3.3 V	0		0.32	V
	V_{IL3}	P20, P21		0		0.3V_{DD}	V
	V_{IL4}	P60, P61		0		0.3EV_{DD}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of P10, P12, P15, P17 is EV_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(4/5)**

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –10 mA	EV_{DD}–1.5			V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	EV_{DD}–0.7			V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	EV_{DD}–0.6			V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	EV_{DD}–0.5			V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OH1} = –1.0 mA	EV_{DD}–0.5			V
	V_{OH2}	P20, P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD}–0.5			V
Output voltage, low	V_{OL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P70 to P74, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 20 mA			1.3	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20, P21	1.6 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60, P61	4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD} < 5.5 V, I_{OL3} = 1.0 mA			0.4	V

Caution P10, P12, P15, P17 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(5/5)**

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{DD}				1	μA
	I_{LIH2}	P20, P21, P137, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P10 to P17, P30 to P32, P40 to P43, P50 to P54, P60, P61, P70 to P74, P120, P125 to P127, P140 to P147	V_I = EV_{SS}				–1	μA
	I_{LIL2}	P20, P21, P137, $\overline{RESET}$	V_I = V_{SS}				–1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pll-up resistance	R_{U1}	V_I = EV_{SS}	SEGxx port					
			2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V		10	20	100	kΩ
			1.6 V ≤ EV_{DD} = V_{DD} < 2.4 V		10	30	100	kΩ
	R_{U2}		Ports other than above (Except for P60, P61, and P130)		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(1/3)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.5		mA
						V_{DD} = 3.0 V		1.5		mA
					Normal operation	V_{DD} = 5.0 V		3.3	5.0	mA
						V_{DD} = 3.0 V		3.3	5.0	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.5	3.7	mA
						V_{DD} = 3.0 V		2.5	3.7	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.8	4.4	mA
						Resonator connection		3.0	4.6	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.8	2.6	mA
						Resonator connection		1.8	2.6	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = –40°C	Normal operation	Square wave input		3.5	4.9	μA
						Resonator connection		3.6	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		3.6	4.9	μA
						Resonator connection		3.7	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		3.7	5.5	μA
						Resonator connection		3.8	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		3.8	6.3	μA
						Resonator connection		3.9	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.1	7.7	μA
						Resonator connection		4.2	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral operation current (except for back ground operation (BGO)). However, not including the current flowing
<R> into the watchdog timer, 12-bit interval timer, A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and LCD controller driver.

<R> **2.** When high-speed on-chip oscillator and subsystem clock are stopped. When real-time clock is stopped.

<R> **3.** When high-speed system clock and subsystem clock are stopped. When real-time clock is stopped.

<R> **4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time clock, serial interface IICA, multiplier and divider/multiply-accumulator, and DMA contoroller are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 24 MHz
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\ V \le V_{DD} \le 5.5\ V$@1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (2/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.44	1.28	mA
					V_{DD} = 3.0 V		0.44	1.28	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 5.0 V		0.40	1.00	mA
					V_{DD} = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	μA
			LV (low-voltage main) mode Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	μA
			HS (high-speed main) mode Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40C	Square wave input		0.31	0.57	μA
					Resonator connection		0.50	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.37	0.57	μA
					Resonator connection		0.56	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.46	1.17	μA
					Resonator connection		0.65	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.57	1.97	μA
					Resonator connection		0.76	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.85	3.37	μA
					Resonator connection		1.04	3.56	μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.17	0.50	μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.32	1.10	μA
			T_A = +70°C				0.43	1.90	μA
			T_A = +85°C				0.71	3.30	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. The values below the MAX. column include the peripheral
<R> operation current (except for back ground operation (BGO)). However, not including the current flowing into the watchdog timer, 12-bit interval timer, A/D converter, LVD circuit, I/O port, on-chip pull-up/pull-down resistors, and LCD controller driver.

2. During HALT instruction execution by flash memory.

<R> **3.** When high-speed on-chip oscillator and subsystem clock are stopped. When real-time clock and multiplier and divider/multiply-accumulator are stopped.

<R> **4.** When high-speed system clock and subsystem clock are stopped. When real-time clock and multiplier and divider/multiply-accumulator are stopped.

5. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1). When
<R> high-speed on-chip oscillator and high-speed system clock are stopped. When real-time clock, serial interface IICA, multiplier and divider/multiply-accumulator, and DMA contoroller are stopped. The values below the MAX. column include the leakage current.

<R> **6.** When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When real-time clock, serial interface IIC, multiplier and divider/multiply-accumulator, and DMA contoroller are stopped. The values below the MAX. column include the leakage current.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 24 MHz
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\ V \le V_{DD} \le 5.5\ V$@1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

<R> **8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(3/3)**

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{MAIN} is stopped				0.08 Note 12		μA
12-bit inteval timer current	I_{IT} Notes 1, 2	f_{MAIN} is stopped				0.08 Note 12		μA
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 15 kHz, f_{MAIN} is stopped				0.24		μA
A/D converter operating current	I_{ADC} Note 4	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V			1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V			0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}					75.0		μA
Temperature sensor operating current	I_{TMPS}					75.0		μA
LVD operating current	I_{LVD} Note 5					0.08		μA
BGO operating current	I_{BGO} Notes 6, 7					2.00	12.20	mA
Flash self-programming operating current	I_{FSP} Note 8					2.00	12.20	mA
LCD operating current	I_{LCD1} Notes 9, 10	External resistance division method		V_{DD} = E_{DD} = 5.0 V V_{L4} = 5.0 V		0.04	0.2	μA
	I_{LCD2} Note 9	Internal voltage boosting method		V_{DD} = E_{DD} = 5.0 V V_{L4} = 5.1 V (VLCD = 12H)		1.12	3.7	μA
				V_{DD} = E_{DD} = 3.0 V V_{L4} = 3.0 V (VLCD = 04H)		0.63	2.2	μA
	I_{LCD3} Note 9	Capacitor split method		V_{DD} = E_{DD} = 3.0 V V_{L4} = 3.0 V		0.12	0.5	μA
SNOOZE operating current	I_{SNOZ}	ADC operation	The mode is performed Note 11			0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V			1.20	1.44	mA
		CSI/UART operation				0.70	0.84	mA

(**Note**, **Caution** and **Remark** are lisited on the next page)

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/L12 is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time clock operating current. However, I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

2. When high-speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 15 kHz low-speed on-chip oscillator). The supply current value of the RL78/L12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

4. Current flowing only to the A/D converter. The supply current value of the RL78/L12 is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVD circuit. The supply current value of the RL78/L12 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit operates.

6. Current flowing only when the BGO operates. The supply current value of the RL78/L12 is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.

<R> **7.** Current flowing during data flash programming (not including the CPU operating current). The TYP. value indicates the averaged current for repeated writing and erasing of contiguous 1 KB on the flash memory. The MAX. value indicates the inrush current that flows during flash programming.

<R> **8.** Current flowing during code flash programming (not including the CPU operating current). The TYP. value indicates the averaged current for repeated writing and erasing of contiguous 1 KB on the flash memory. The MAX. value indicates the inrush current that flows during flash programming.

<R> **9.** Current flowing only to the LCD controller/driver (V_{DD} pin). The supply current value of the RL78/L12 microcontrollers is the sum of the LCD operating current (I_{LCD1}, I_{LCD2} or I_{LCD3}) to the supply current (I_{DD1}, or I_{DD2}) when the LCD controller/driver operates in an operation mode or HALT mode. Not including the current that flows through the LCD panel.

The TYP. value and MAX. value are following conditions.

- Set 20 pins as a segment function, all lighting
- When f_{SUB} is selected for system clock, LCD clock = 128 Hz (LCDC0 = 07H)
- 4-Time-Slice, 1/3 Bias Method

10. Not including the current that flows through the external divider resistor when the external resistance division method is used.

<R> **11.** For shift time to the SNOOZE mode, see **19.3.3 SNOOZE mode** in the **RL78/L12 User's Manual: Hardware (R01UH0330E)**.

<R> **12.** Add 200 nA when using f_{IL}.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

2.4 AC Characteristics

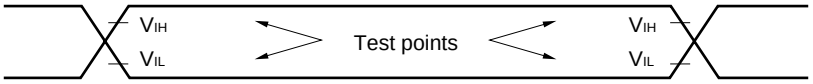
2.4.1 Basic operation

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

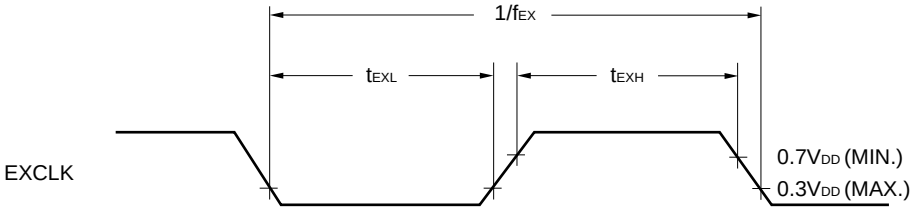
Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low voltage main) mode	1.6 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.04167		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			LV (low voltage main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 5.5 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V			1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		1.8 V ≤ V_{DD} < 2.7 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns
TO00 to TO07 output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V				12	MHz
			2.7 V ≤ EV_{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV_{DD} < 2.7 V				4	MHz
		LV (low voltage main) mode	1.6 V ≤ EV_{DD} ≤ 5.5 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V ≤ EV_{DD} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV_{DD} < 4.0 V				8	MHz
			2.4 V ≤ EV_{DD} < 2.7 V				4	MHz
		LV (low voltage main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V				4	MHz
			1.6 V ≤ EV_{DD} < 1.8 V				2	MHz
		LS (high-speed main) mode	1.8 V ≤ EV_{DD} ≤ 5.5 V				4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	1.6 V ≤ V_{DD} ≤ 5.5 V		1			μs
		INTP1 to INTP7	1.6 V ≤ EV_{DD} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR3	1.8 V ≤ EV_{DD} ≤ 5.5 V		250			ns
			1.6 V ≤ EV_{DD} < 1.8 V		1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

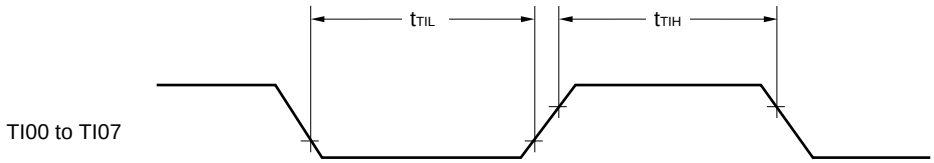
<R> **AC Timing Test Points**

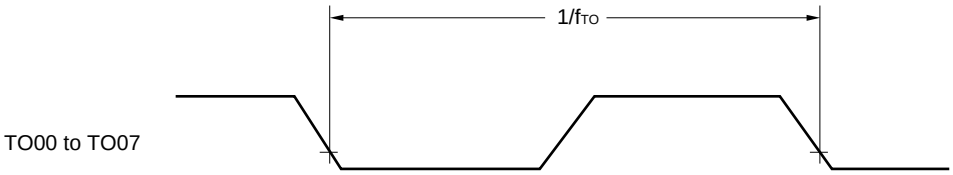


External System Clock Timing

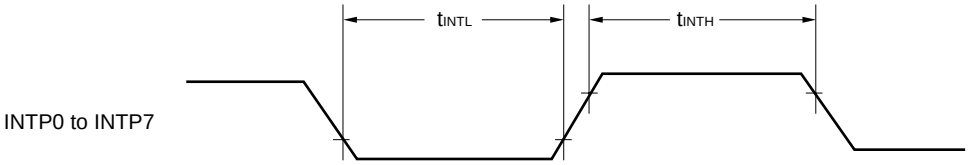


TI/TO Timing

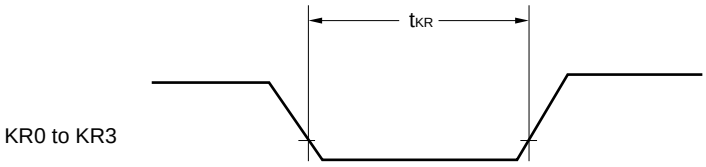




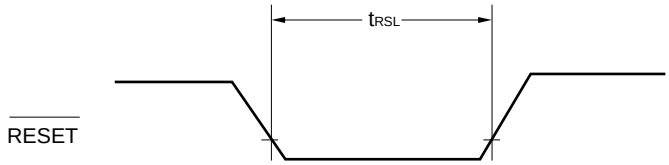
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

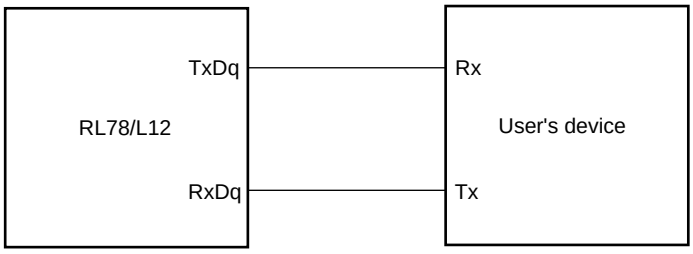
2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

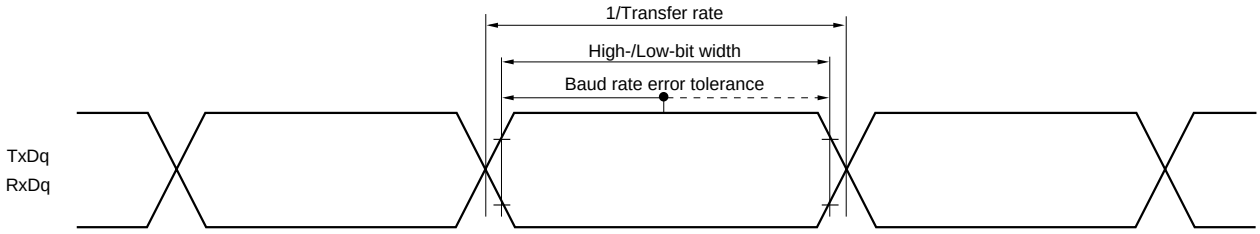
<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		2.4 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V		f_{MCK}/6 Note 4		f_{MCK}/6 Note 4		f_{MCK}/6 Note 4	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 5		4.0		1.3		0.7	Mbps
		1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V				f_{MCK}/6 Note 4		f_{MCK}/6 Note 4	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 5				1.3		0.7	Mbps
		1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V						f_{MCK}/6 Note 4	bps
		Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 5						0.7	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



<R> **Notes 1.** HS is condition of HS (high-speed main) mode.
<R> **2.** LS is condition of LS (low-speed main) mode.
<R> **3.** LV is condition of LV (low-voltage main) mode.
4. Transfer rate in the SNOOZE mode is max. 9600 bps, min. 4800 bps.
<R> **5.** f_{CLK} in each operating mode is as below.
HS (high-speed main) mode: f_{CLK} = 24 MHz
LS (low-speed main) mode: f_{CLK} = 8 MHz
LV (low-voltage main) mode: f_{CLK} = 4 MHz

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(2) During communication at same potential (CSI mode) (master mode (f_{MCK}/2, f_{MCK}/4), $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD} ≤ 5.5 V		167 Note 4		500 Note 4		1000 Note 4		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		250 Note 4		500 Note 4		1000 Note 4		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V				500 Note 4		1000 Note 4		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V						1000 Note 4		ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –12		t_{KCY1}/2 –50		t_{KCY1}/2 –100		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –18		t_{KCY1}/2 –50		t_{KCY1}/2 –100		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY1}/2 –38		t_{KCY1}/2 –50		t_{KCY1}/2 –100		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V				t_{KCY1}/2 –50		t_{KCY1}/2 –100		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V						t_{KCY1}/2 –100		ns
SIp setup time (to $\overline{SCKp}$↑) Note 5	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V		44		110		220		ns
		2.7 V ≤ EV_{DD} ≤ 5.5 V		44		110		220		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V		75		110		220		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V				110		220		ns
		1.6 V ≤ EV_{DD} ≤ 5.5 V						220		ns
SIp hold time (from $\overline{SCKp}$↑) Note 6	t_{KSI1}	2.4 V ≤ EV_{DD} ≤ 5.5 V		19		19		19		ns
		1.8 V ≤ EV_{DD} ≤ 5.5 V				19		19		
		1.6 V ≤ EV_{DD} ≤ 5.5 V						19		
Delay time from $\overline{SCKp}$↓ to SOp output Note 7	t_{KSO1}	C = 30 pF Note 8	2.4 V ≤ EV_{DD} ≤ 5.5 V		25		25		25	ns
			1.8 V ≤ EV_{DD} ≤ 5.5 V				25		25	
			1.6 V ≤ EV_{DD} ≤ 5.5 V						25	

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. For CSI00, set a cycle of 2/f_{MCK} or longer. For CSI01, set a cycle of 4/f_{MCK} or longer.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

8. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

(3) During communication at same potential (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCKp}}$ cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}						ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}						ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 2.7 V	12 MHz < f_{MCK}	8/f_{MCK}						ns
			f_{MCK} ≤ 12 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 2.4 V				6/f_{MCK}		6/f_{MCK}		ns
		1.6 V ≤ EV_{DD} < 1.8 V						6/f_{MCK}		ns
$\overline{\text{SCKp}}$ high-/low-level width	t_{KH2}, t_{KL2}	4..0 V ≤ EV_{DD} ≤ 5.5 V		t_{KCY2}/2 –7		t_{KCY2}/2 –7		t_{KCY2}/2 –7		ns
		2.7 V ≤ EV_{DD} < 4.0 V		t_{KCY2}/2 –8		t_{KCY2}/ –-8		t_{KCY2}/2 –8		ns
		2.4 V ≤ EV_{DD} < 2.7 V		t_{KCY2}/2 –18		t_{KCY2}/2 –18		t_{KCY2}/2 –18		ns
		1.8 V ≤ EV_{DD} < 2.4 V				t_{KCY2}/2 –18		t_{KCY2}/2 –18		ns
		1.6 V ≤ EV_{DD} < 1.8 V						t_{KCY2}/2 –66		ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 5	t_{SIK2}	2.7 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} +20		1/f_{MCK} +30		1/f_{MCK} +30		ns
		2.4 V ≤ EV_{DD} < 2.7 V		1/f_{MCK} +30		1/f_{MCK} +30		1/f_{MCK} +30		
		1.8 V ≤ EV_{DD} < 2.4 V				1/f_{MCK} +30		1/f_{MCK} +30		ns
		1.6 V ≤ EV_{DD} < 1.8 V						1/f_{MCK} +40		ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 6	t_{KSI2}	2.4 V ≤ EV_{DD} ≤ 5.5 V		1/f_{MCK} +31		1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.8 V ≤ EV_{DD} < 2.4 V				1/f_{MCK} +31		1/f_{MCK} +31		ns
		1.6 V ≤ EV_{DD} < 1.8 V						1/f_{MCK}+ 250		ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Note 7	t_{KSO2}	C = 30 pF Note 8	4.0 V ≤ EV_{DD} ≤ 5.5 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.7 V ≤ EV_{DD} < 4.0 V		2/f_{MCK} +44		2/f_{MCK} +110		2/f_{MCK} +110	ns
			2.4 V ≤ EV_{DD} < 2.7 V		2/f_{MCK} +75		2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.8 V ≤ EV_{DD} < 2.4 V				2/f_{MCK} +110		2/f_{MCK} +110	ns
			1.6 V ≤ EV_{DD} < 1.8 V						2/f_{MCK}+ 220	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{\text{SCKp}}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{\text{SCKp}}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

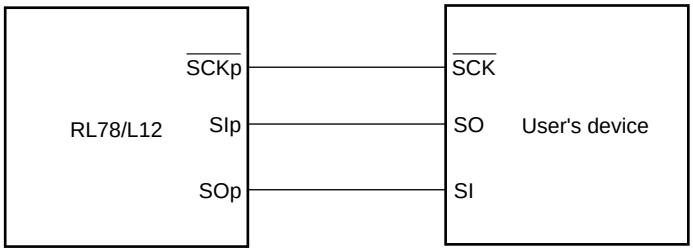
8. C is the load capacitance of the SOp output lines.

<R> **Caution Select the normal input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

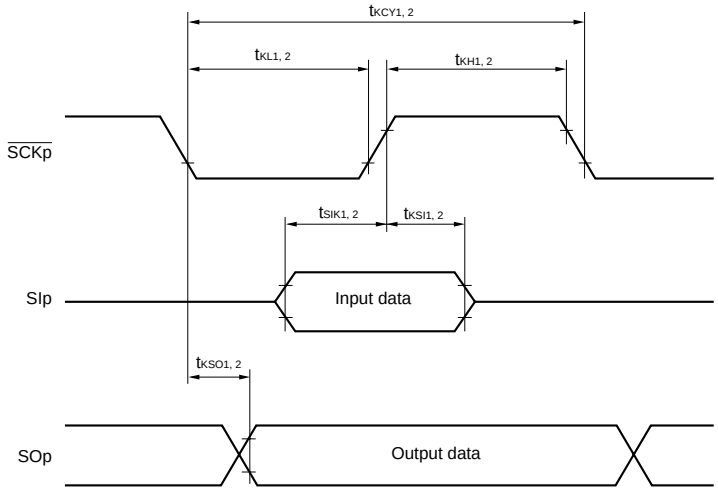
Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0),
n: Channel number (n = 0, 1), g: PIM number (g = 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

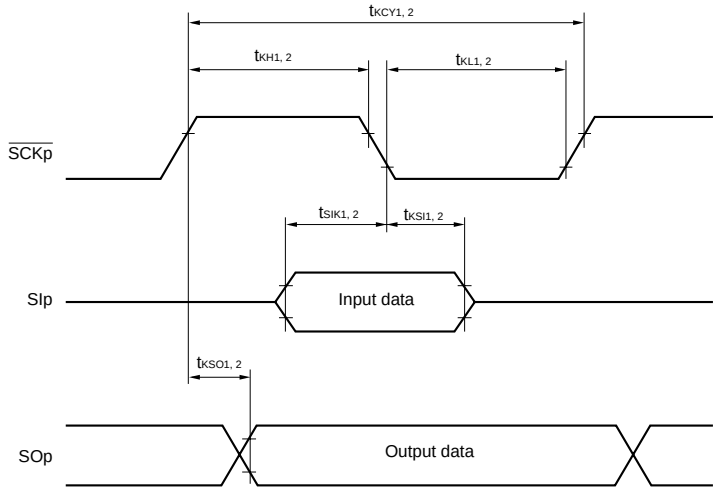
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01)

2. m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions			HS Note 1		LS Note 2		LV Note 3		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		reception	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			f_{MCK}/6 Note 4		f_{MCK}/6 Notes 4, 5		f_{MCK}/6 Notes 4, 5	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 6		4.0		1.3		0.7	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			f_{MCK}/6 Note 4		f_{MCK}/6 Notes 4, 5		f_{MCK}/6 Notes 4, 5	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 6		4.0		1.3		0.7	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			f_{MCK}/6 Note 4		f_{MCK}/6 Notes 4, 5		f_{MCK}/6 Notes 4, 5	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 6		4.0		1.3		0.7	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V					f_{MCK}/6 Notes 4, 5		f_{MCK}/6 Notes 4, 5	bps
				Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 6				1.3		0.7	Mbps

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

5. Use it with EV_{DD}≥V_b.

<R> **6.** f_{CLK} in each operating mode is as below.

HS (high-speed main) mode: f_{CLK} = 24 MHz

LS (low-speed main) mode: f_{CLK} = 8 MHz

LV (low-voltage main) mode: f_{CLK} = 4 MHz

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

(4) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions			HS Note 1		LS Note 2		LV Note 3		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		transmission	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Notes 4, 5**		**Notes 4, 5**		**Notes 4, 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 6		2.8 Note 6		2.8 Note 6	Mbps
			2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Notes 5, 7**		**Notes 5, 7**		**Notes 5, 7**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ V_b = 2.3 V		1.2 Note 8		1.2 Note 8		1.2 Note 8	Mbps
			2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Notes 5, 9, 10**		**Notes 5, 9, 10**		**Notes 5, 9, 10**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ V_b = 1.6 V		0.43 Note 11		0.43 Note 11		0.43 Note 11	Mbps
			1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V					**Notes 5, 9, 10**		**Notes 5, 9, 10**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V				0.43 Note 11		0.43 Note 11	Mbps

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

5. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Notes 7. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

9. Use it with $EV_{DD} \geq V_b$.

10. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

11. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 10 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/E_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

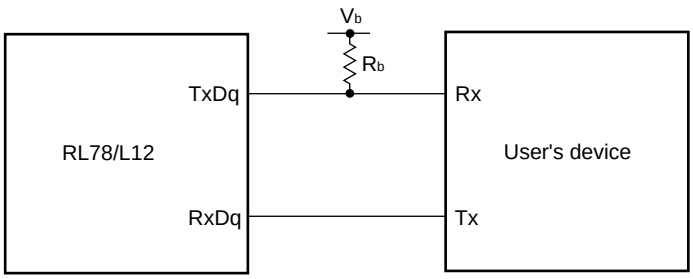
Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)

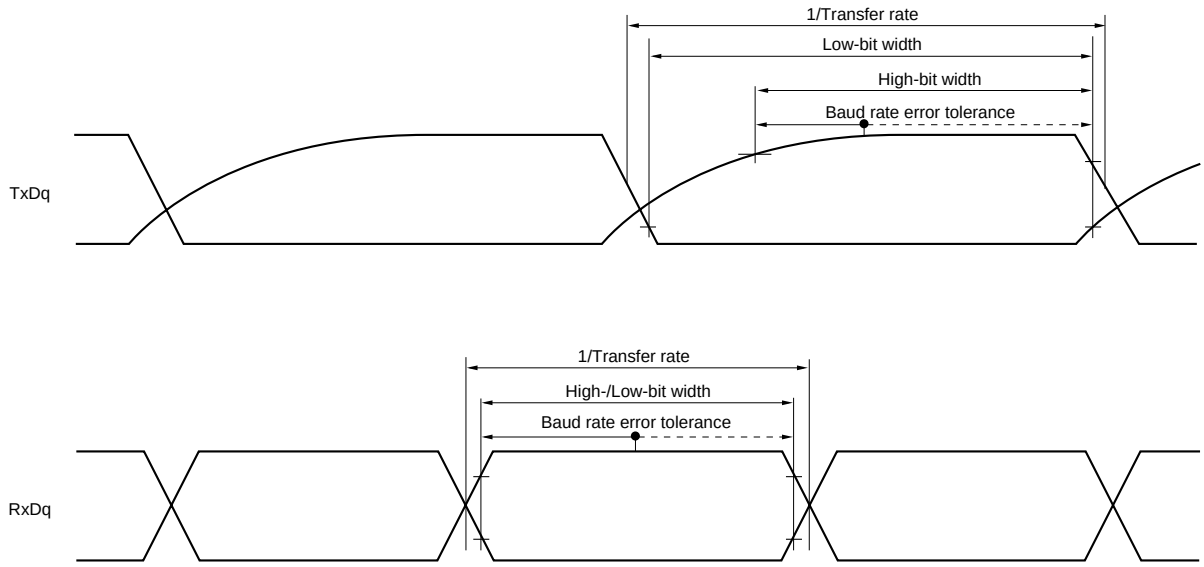
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

<R>

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance, V_b[V]: Communication line voltage

2. q: UART number (q = 0), g: PIM and POM number (g = 1)

(5) Communication at different potential (2.5 V, 3 V) (f_{MCK}/2) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output, corresponding CSI00 only)

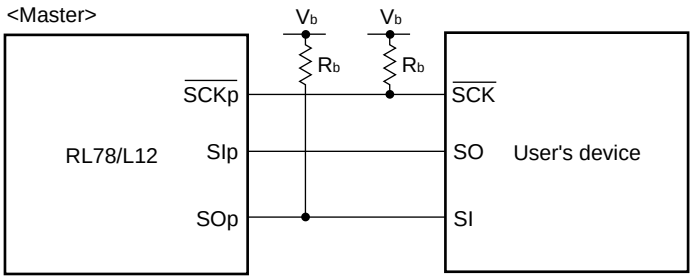
(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200 Note 4		1150 Note 4		1150 Note 4		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300 Note 4		1150 Note 4		1150 Note 4		ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		t_{KCY1}/2 – 120		ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 7		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
SIp setup time (to $\overline{SCKp}$↑) Note 5	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	121		479		479		ns
SIp hold time (from $\overline{SCKp}$↑) Note 5	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 5	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		130		130		130	ns
SIp setup time (to $\overline{SCKp}$↓) Note 6	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33		110		110		ns
SIp hold time (from $\overline{SCKp}$↓) Note 6	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10		10		10		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 6	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. The value must also be $2/f_{MCK}$ or more.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

6. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01)

<R>

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300 Note 4		1150 Note 4		1150 Note 4		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note 4		1150 Note 4		1150 Note 4		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note 4		1150 Note 4		1150 Note 4		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			1150 Note 4		1150 Note 4		ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns

<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. The value must also be 4/f_{MCK} or more.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/E_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with EV_{DD} ≥ V_b.

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

<R>

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (f_{MCK}/4) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

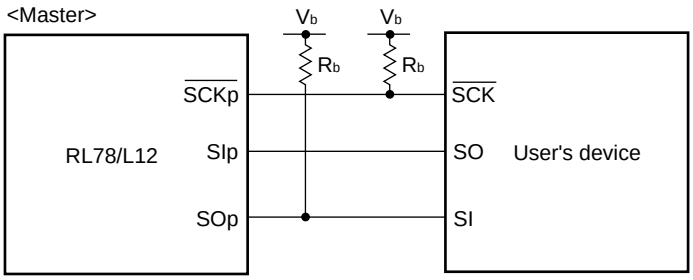
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions	HS Note 1		LS Note 2		LV Note 3		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to $\overline{SCKp}$↑) Note 4	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177		479		479		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479		479		479		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			479		479		ns
SIp hold time (from $\overline{SCKp}$↑) Note 4	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		195		195		195	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		483		483		483	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				483		483	ns
SIp setup time (to $\overline{SCKp}$↓) Note 5	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	110		110		110		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			110		110		ns
SIp hold time (from $\overline{SCKp}$↓) Note 5	t_{KSI1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		2.4 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			19		19		ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 5	t_{KSO1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ				25		25	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

5. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

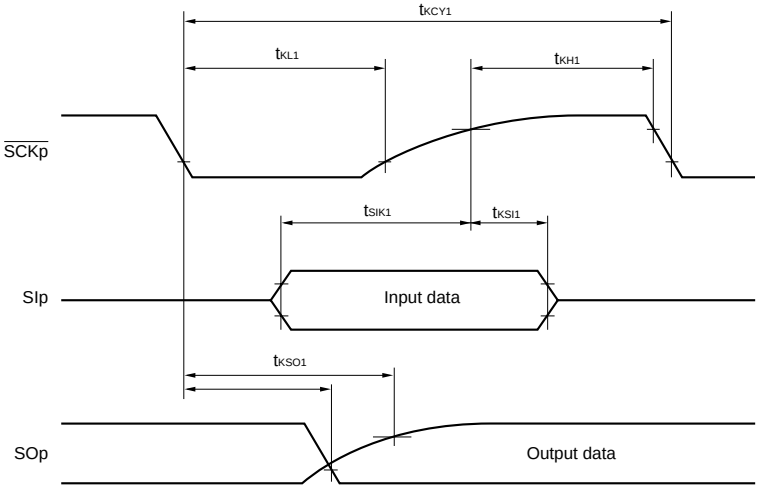
Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/E_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with $EV_{DD} \geq V_b$.

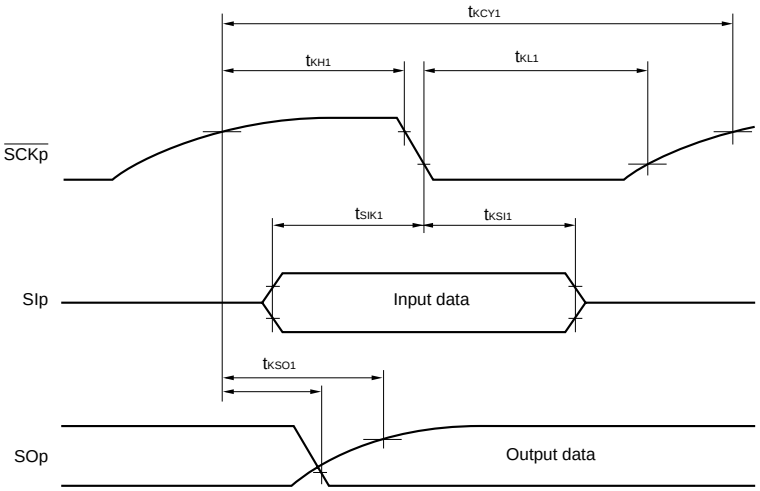
Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, $\overline{\text{SCKp}}$... external clock input)

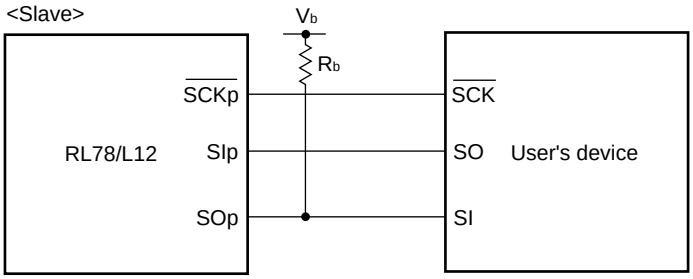
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

<R>

Parameter	Symbol	Conditions		HS Note 1		LS Note 2		LV Note 3		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{\text{SCKp}}$ cycle time Note 4	t_{KCY2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}						ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 5	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}						ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}						ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}						ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 5	4 MHz < f_{MCK} ≤ 8 MHz			16/f_{MCK}				ns
			f_{MCK} ≤ 4 MHz			10/f_{MCK}		10/f_{MCK}		ns
$\overline{\text{SCKp}}$ high-/low-level width Note 5	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 12		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to $\overline{\text{SCKp}}$↑) Note 6	t_{SIK2}	2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from $\overline{\text{SCKp}}$↑) Note 7	t_{KSI2}	2.7 V ≤ EV_{DD} < 5.5 V, 2.3 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		2.4 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from $\overline{\text{SCKp}}$↓ to SOp output Notes 5, 8	t_{KSO2}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.4 V ≤ EV_{DD} < 4.0 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ					2/f_{MCK} + 573		2/f_{MCK} + 573	ns

(**Note**, **Caution** and **Remark** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



<R> **Notes 1.** HS is condition of HS (high-speed main) mode.

<R> **2.** LS is condition of LS (low-speed main) mode.

<R> **3.** LV is condition of LV (low-voltage main) mode.

4. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

5. Use it with $EV_{DD} \geq V_b$.

6. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

7. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

8. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

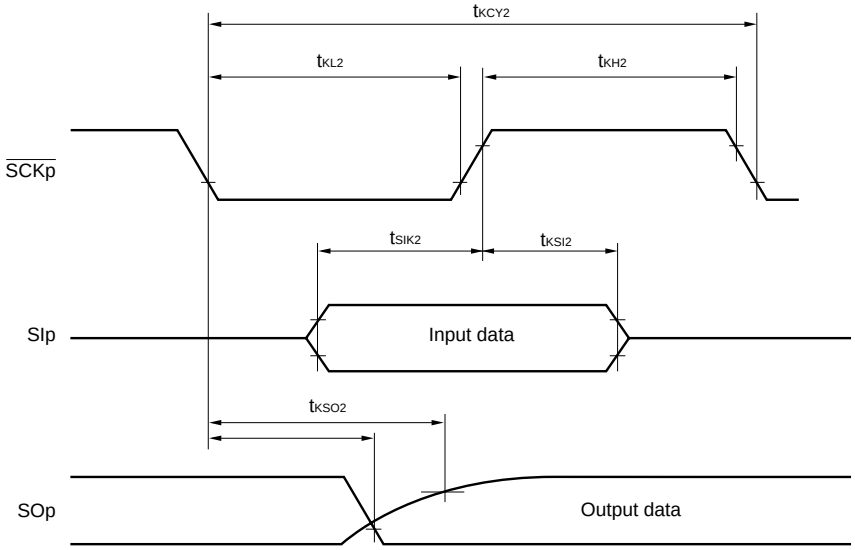
Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/E_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

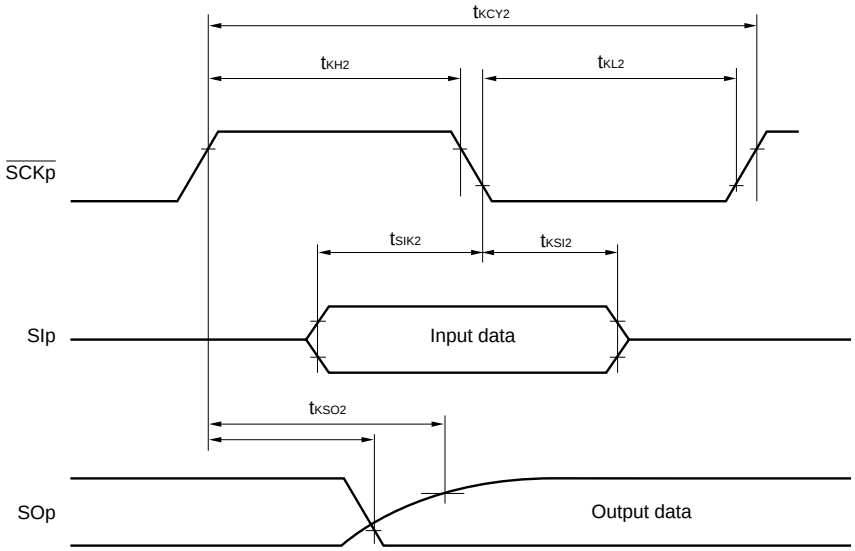
2. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance (32-pin to 52-pin products)/EV_{DD} tolerance (64-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1),
g: PIM and POM number (g = 1)

2.5.2 Serial interface IICA

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(1/2)**

<R>

Parameter	Symbol	Conditions	Standard Mode Note 1						Unit
			HS Note 2		LS Note 3		LV Note 4		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	kHz
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0	100	0	100	0	100	
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0	100	0	100	
		1.6 V ≤ EV_{DD} ≤ 5.5 V					0	100	
Setup time of restart condition Note 5	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.7		
Hold time	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.0		
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.7		
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.0		
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	250		250		250		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	250		250		250		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			250		250		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					250		
Data hold time (transmission) Note 6	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0	3.45	0	3.45	
		1.6 V ≤ EV_{DD} ≤ 5.5 V					0	3.45	
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.0		4.0		4.0		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.0		4.0		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.0		
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	4.7		4.7		4.7		
		1.8 V ≤ EV_{DD} ≤ 5.5 V			4.7		4.7		
		1.6 V ≤ EV_{DD} ≤ 5.5 V					4.7		

(**Note** and **Remark** are listed on the next page.)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) **(2/2)**

<R>

Parameter	Symbol	Conditions	Fast Mode Note 7						Fast Mode Plus Note 8		Unit
			HS Note 2		LS Note 3		LV Note 4		HS Note 2		
			MIN.	MAX.	MIN.	MIN.	MAX.	MIN.	MAX.	MIN.	
SCLA0 clock frequency	f_{SCL}	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400	0	1000	kHz
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0	400	0	400	0	400			
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0	400	0	400			
Setup time of restart condition Note 5	$t_{SU:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6		0.26		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0.6		0.6				
Hold time	$t_{HD:STA}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6		0.26		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0.6		0.6				
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD} ≤ 5.5 V	1.3		1.3		1.3		0.5		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	1.3		1.3		1.3				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			1.3		1.3				
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6		0.26		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0.6		0.6				
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	100		100		100		50		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V	100		100		100				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			100		100				
Data hold time (transmission) Note 6	$t_{HD:DAT}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	0	0.9	0	0.9	0	0.9	0	450	μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0	0.9	0	0.9	0	0.9			
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0	0.9	0	0.9			
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6		0.26		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	0.6		0.6		0.6				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			0.6		0.6				
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD} ≤ 5.5 V	1.3		1.3		1.3		0.5		μs
		2.4 V ≤ EV_{DD} ≤ 5.5 V	1.3		1.3		1.3				
		1.8 V ≤ EV_{DD} ≤ 5.5 V			1.3		1.3				

<R> **Notes 1.** In normal mode, use it with f_{CLK} ≥ 1 MHz, 1.6 V ≤ EV_{DD} ≤ 5.5 V.

<R> **2.** HS is condition of HS (high-speed main) mode.

<R> **3.** LS is condition of LS (low-speed main) mode.

<R> **4.** LV is condition of LV (low-voltage main) mode.

5. The first clock pulse is generated after this period when the start/restart condition is detected.

6. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

<R> **7.** In fast mode, use it with f_{CLK} ≥ 3.5 MHz, 1.8 V ≤ EV_{DD} ≤ 5.5 V.

<R> **8.** In fast mode plus, use it with f_{CLK} ≥ 10 MHz, 2.7 V ≤ EV_{DD} ≤ 5.5 V.

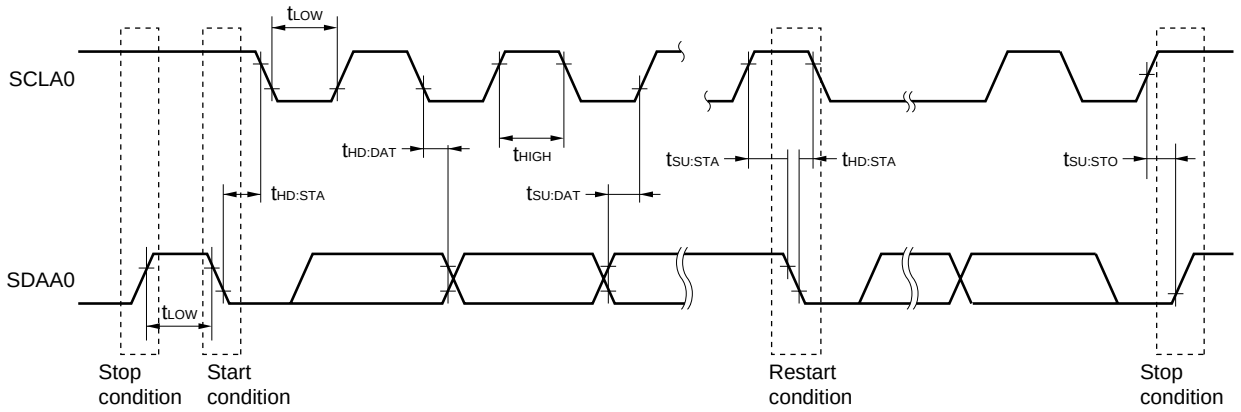
Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



2.5.3 On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI16 to ANI23 (supply ANI pin to EV_{DD})

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution AV_{REFP} = V_{DD}	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD}	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Reference voltage (+)	AV_{REFP}			1.6		V_{DD}	V
Analog input voltage	V_{AIN}			0		AV_{REFP} and EV_{DD}	V
	V_{BGR}	Select internal reference voltage output, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode only		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target ANI pin : ANI0, ANI1, ANI16 to ANI23

(T_A = –40 to +85°C, 1.6 V ≤ $EV_{DD} = V_{DD}$ ≤ 5.5 V, $V_{SS} = EV_{SS}$ = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V		1.2	±10.5	LSB
Conversion time	t_{CONV}	10-bit resolution	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V			±0.85	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V_{DD} ≤ 5.5 V			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V			±6.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.8 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Analog input voltage	V_{AIN}	ANI0, ANI1		0		V_{DD}	V
		ANI16 to ANI23		0		EV_{DD}	V
	V_{BGR}	Select internal reference voltage output, 2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode only		1.38	1.45	1.5	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When $AV_{REF(+)}$ = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI0, ANI16 to ANI23

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V, Reference voltage (+) = V_{BGR}, Reference voltage (–) = AV_{REFM} = 0 V) (HS (high-speed main) mode only)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V) (HS (high-speed main) mode only)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
<R> Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time					350	μs

2.6.4 LVD circuit characteristics

(T_A = –40 to +85°C, $V_{PDR} \leq EV_{DD} = V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \le EV_{DD} = V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD13}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V_{LVD12}		LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVD11}		LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVD4}		LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD11}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V_{LVD10}		LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVD9}		LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVD2}		LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVD8}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V_{LVD7}		LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVD6}		LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVD1}		LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.68	3.75	3.82	V
				Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVD5}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V_{LVD4}		LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD3}		LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVD0}		LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.98	4.06	4.14	V
				Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Supply voltage rise time

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} rise slope (V_{DD} : 0 V to V_{DD} (MIN.)[Note])	SV_{DD}				54	V/ms

<R> **Note** V_{DD} (MIN.) in each operating mode is as below.

HS (high-speed main) mode: 2.7 V@1 MHz to 24 MHz
2.4 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V@1 MHz to 4 MHz

<R> **Caution When LVD off, be sure to use external $\overline{\text{RESET}}$ pin.**

2.7 LCD Characteristics

2.7.1 Resistance division method

(1) Static display mode

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.0		V_{DD}	V

(2) 1/2 bias method, 1/4 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.7		V_{DD}	V

(3) 1/3 bias method

(T_A = –40 to +85°C, V_{L4} (MIN.) ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{L4}		2.5		V_{DD} Note	V

Note 5.5 V (MAX) when driving a memory-type liquid crystal (the MLCDEN bit of the MLCD register = 1).

2.7.2 Internal voltage boosting method

(1) 1/3 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C4[Note 1] = 0.47 μF[Note 2]	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C4[Note 1] = 0.47 μF		2 V_{L1} –0.1	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L4}	C1 to C4[Note 1] = 0.47 μF		3 V_{L1} –0.15	3 V_{L1}	3 V_{L1}	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C4[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = 0.47 pF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

(2) 1/4 bias method

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
LCD output voltage variation range	V_{L1}	C1 to C5[Note 1] = 0.47 μF[Note 2]	VLCD = 04H	0.90	1.00	1.08	V
			VLCD = 05H	0.95	1.05	1.13	V
			VLCD = 06H	1.00	1.10	1.18	V
			VLCD = 07H	1.05	1.15	1.23	V
			VLCD = 08H	1.10	1.20	1.28	V
			VLCD = 09H	1.15	1.25	1.33	V
			VLCD = 0AH	1.20	1.30	1.38	V
			VLCD = 0BH	1.25	1.35	1.43	V
			VLCD = 0CH	1.30	1.40	1.48	V
			VLCD = 0DH	1.35	1.45	1.53	V
			VLCD = 0EH	1.40	1.50	1.58	V
			VLCD = 0FH	1.45	1.55	1.63	V
			VLCD = 10H	1.50	1.60	1.68	V
			VLCD = 11H	1.55	1.65	1.73	V
			VLCD = 12H	1.60	1.70	1.78	V
			VLCD = 13H	1.65	1.75	1.83	V
Doubler output voltage	V_{L2}	C1 to C5[Note 1] = 0.47 μF		2 V_{L1}–0.08	2 V_{L1}	2 V_{L1}	V
Tripler output voltage	V_{L3}	C1 to C5[Note 1] = 0.47 μF		3 V_{L1}–0.12	3 V_{L1}	3 V_{L1}	V
Quadruply output voltage	V_{L4}	C1 to C5[Note 1] = 0.47 μF		4 V_{L1}–0.16	4 V_{L1}	4 V_{L1}	V
Reference voltage setup time[Note 2]	t_{VWAIT1}			5			ms
Voltage boost wait time[Note 3]	t_{VWAIT2}	C1 to C5[Note 1] = 0.47 μF		500			ms

Notes 1. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between V_{L1} and GND
C3: A capacitor connected between V_{L2} and GND
C4: A capacitor connected between V_{L3} and GND
C5: A capacitor connected between V_{L4} and GND
C1 = C2 = C3 = C4 = C5 = 0.47 pF±30 %

2. This is the time required to wait from when the reference voltage is specified by using the VLCD register (or when the internal voltage boosting method is selected [by setting the MDSET1 and MDSET0 bits of the LCDM0 register to 01B] if the default value reference voltage is used) until voltage boosting starts (VLCON = 1).

3. This is the wait time from when voltage boosting is started (VLCON = 1) until display is enabled (LCDON = 1).

2.7.3 Capacitor split method

(1) 1/3 bias method

(T_A = –40 to +85°C, 2.2 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
V_{L4} voltage	V_{L4}	C1 to C4 = 0.47 μF[Note 2]		V_{DD}		V
V_{L2} voltage	V_{L2}	C1 to C4 = 0.47 μF[Note 2]	2/3 V_{L4} –0.1	2/3 V_{L4}	2/3 V_{L4} +0.1	V
V_{L1} voltage	V_{L1}	C1 to C4 = 0.47 μF[Note 2]	1/3 V_{L4} –0.1	1/3 V_{L4}	1/3 V_{L4} +0.1	V
Capacitor split wait time[Note 1]	t_{VWAIT}		100			ms

Notes 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).

2. This is a capacitor that is connected between voltage pins used to drive the LCD.

C1: A capacitor connected between CAPH and CAPL

C2: A capacitor connected between V_{L1} and GND

C3: A capacitor connected between V_{L2} and GND

C4: A capacitor connected between V_{L4} and GND

C1 = C2 = C3 = C4 = 0.47 pF±30 %

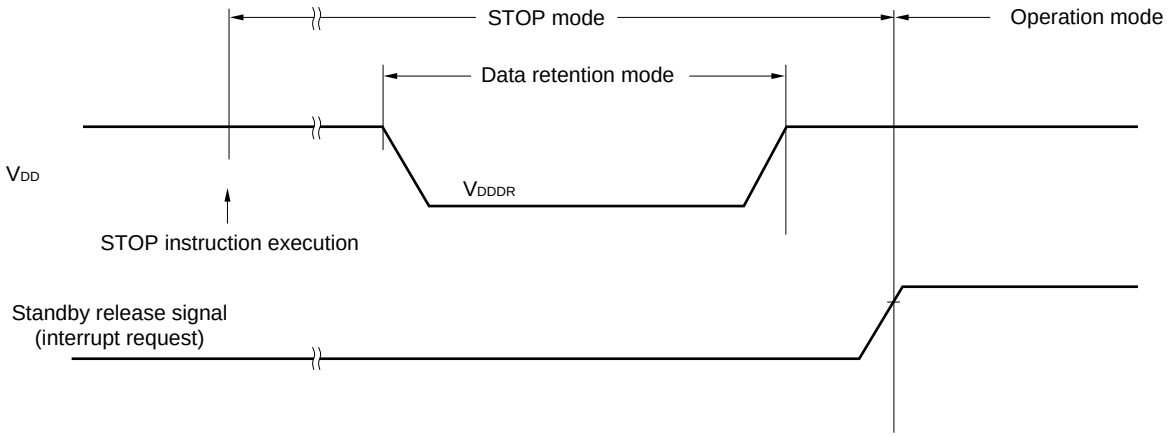
2.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C)

<R>

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



<R> 2.9 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD} = V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V		1		24	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years	T_A = 85°C Note 3	1,000			Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year	T_A = 25°C Note 3		1,000,000		
		Retained for 5 years	T_A = 85°C Note 3	100,000			
		Retained for 20 years	T_A = 85°C Note 3	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

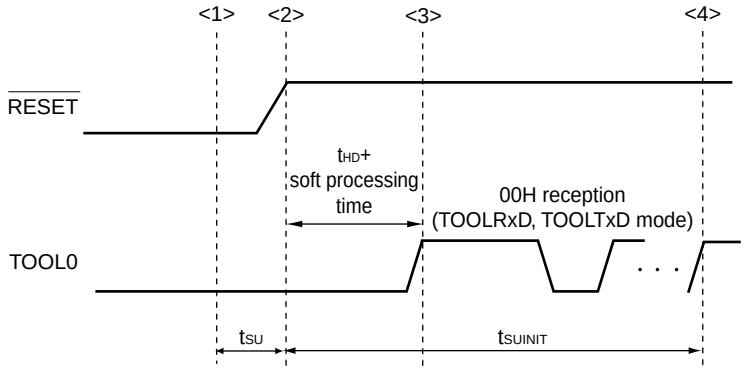
3. This characteristic indicates the flash memory characteristic and based on Renesas Electronics reliability test.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Timing Specifications for Switching Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms

<R>



<1> The low level is input to the TOOL0 pin.

<2> The pins reset ends. (POR and LVD reset must end before the pin reset ends.)

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and completion of the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the reset ends.

t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs)

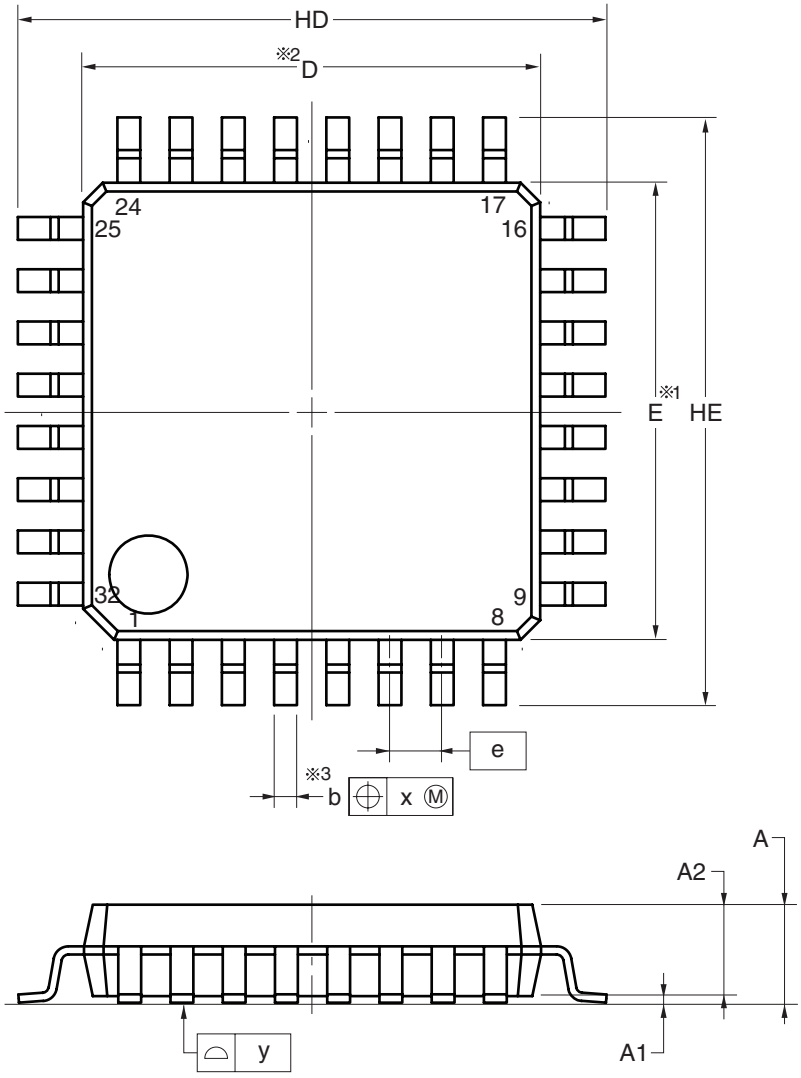
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external or internal resets ends (except software processing time)

3. PACKAGE DRAWINGS

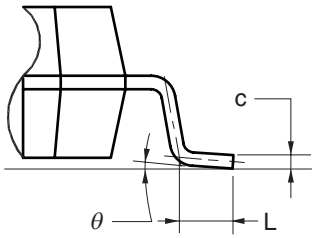
3.1 32-pin products

R5F10RB8AFP, R5F10RBAAFP, R5F10RBCAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

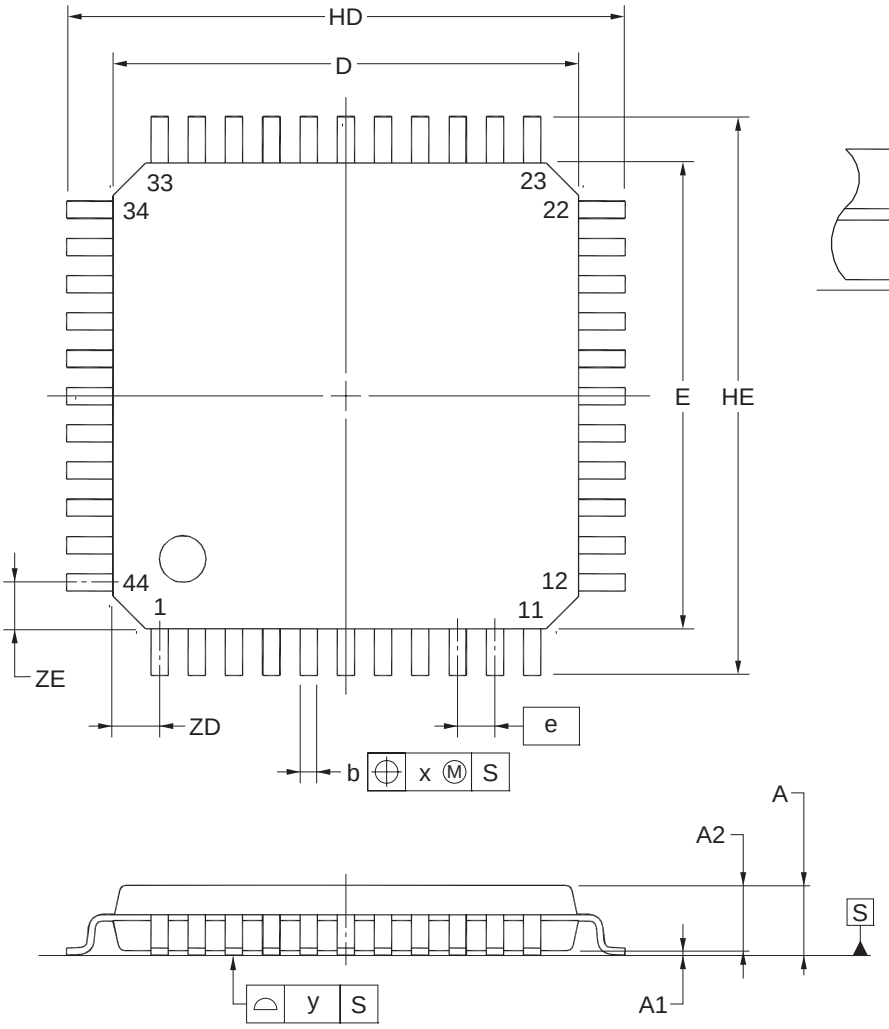
1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

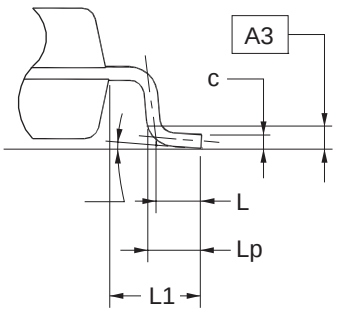
3.2 44-pin products

R5F10RF8AFP, R5F10RFAAFP, R5F10RFCAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.37^{+0.08}_{0.07}$
c	$0.145^{+0.055}_{0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3^{\circ}{}^{+5^{\circ}}_{3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

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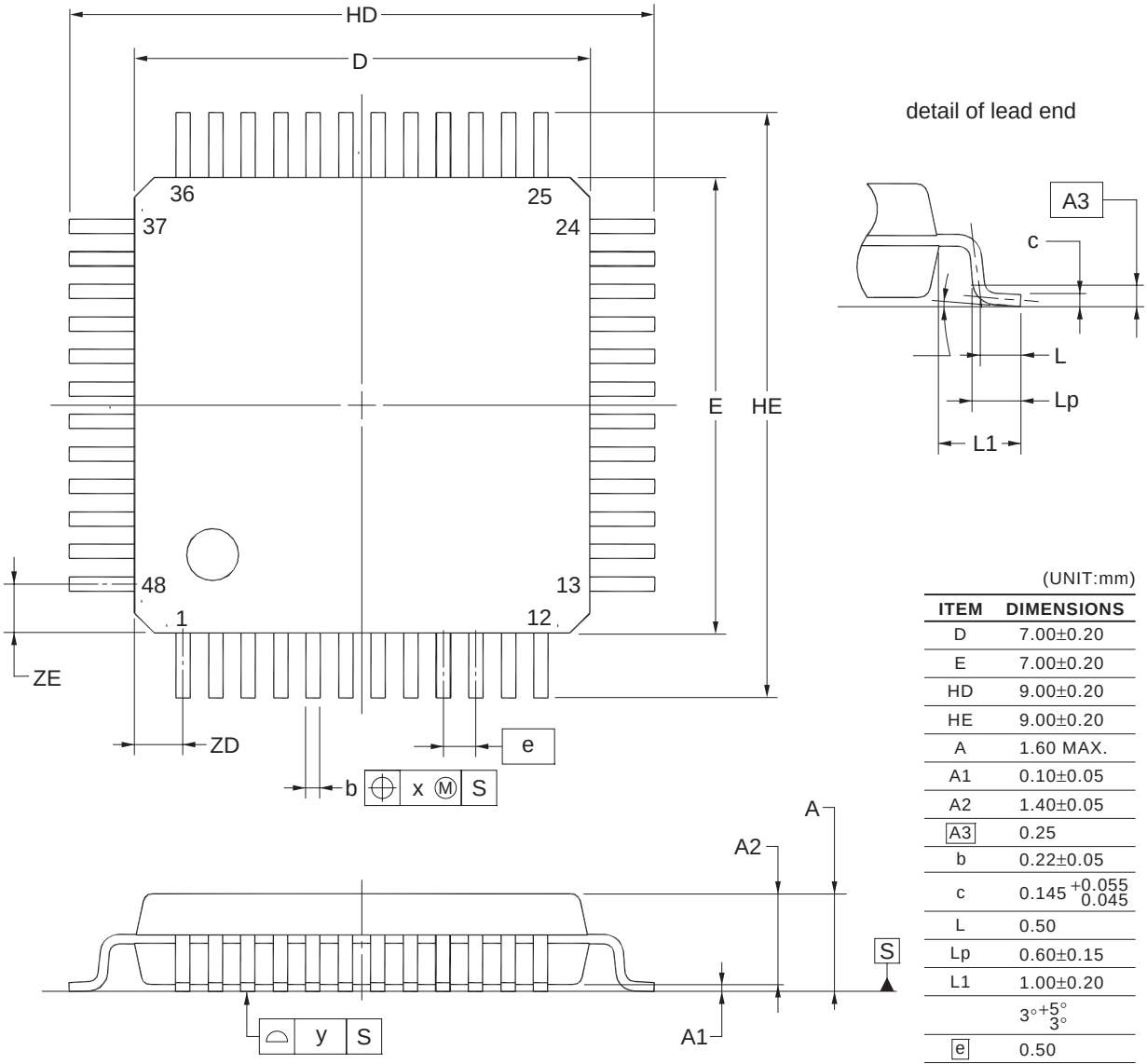
3.3 48-pin products

R5F10RG8AFB, R5F10RGAAFB, R5F10RGCAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3^{\circ}{}^{+5^{\circ}}_{3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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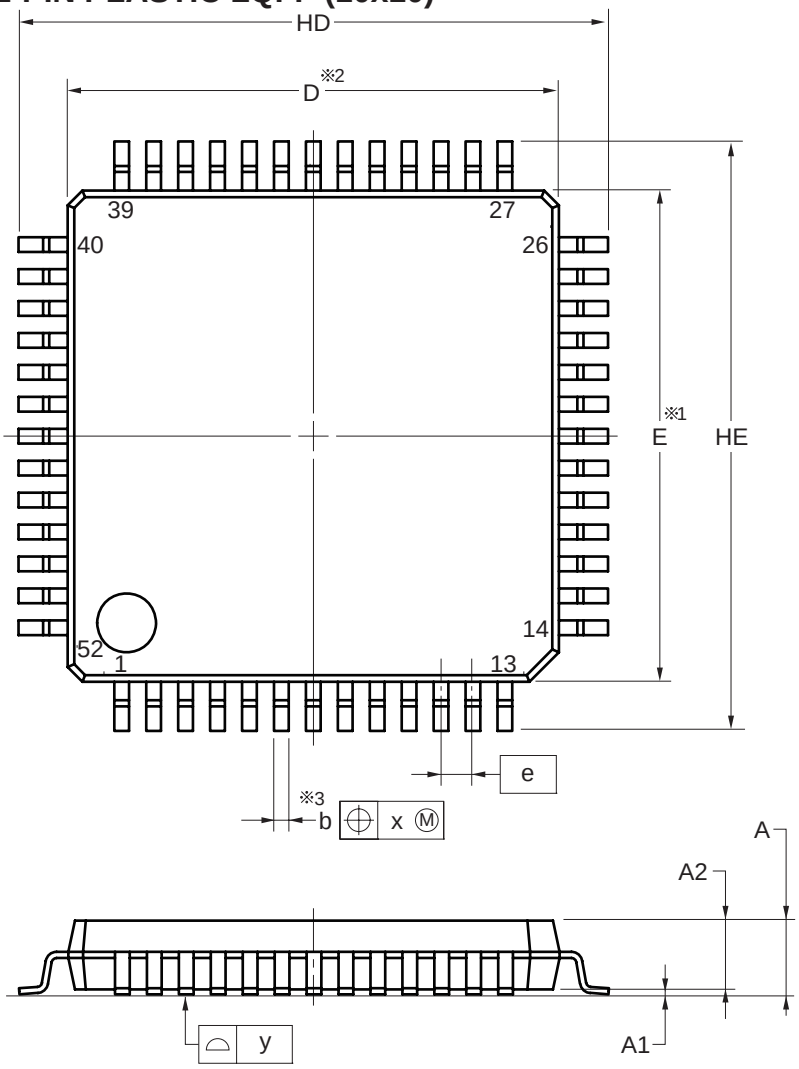
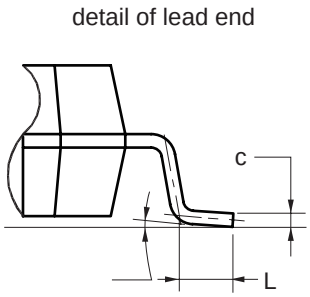
3.4 52-pin products

R5F10RJ8AFA, R5F10RJAAFA, R5F10RJCAFA

52-PIN PLASTIC LQFP (10x10)





(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
	0° to 8°
e	0.65
x	0.13
y	0.10

P52GB-65-GBS

NOTE

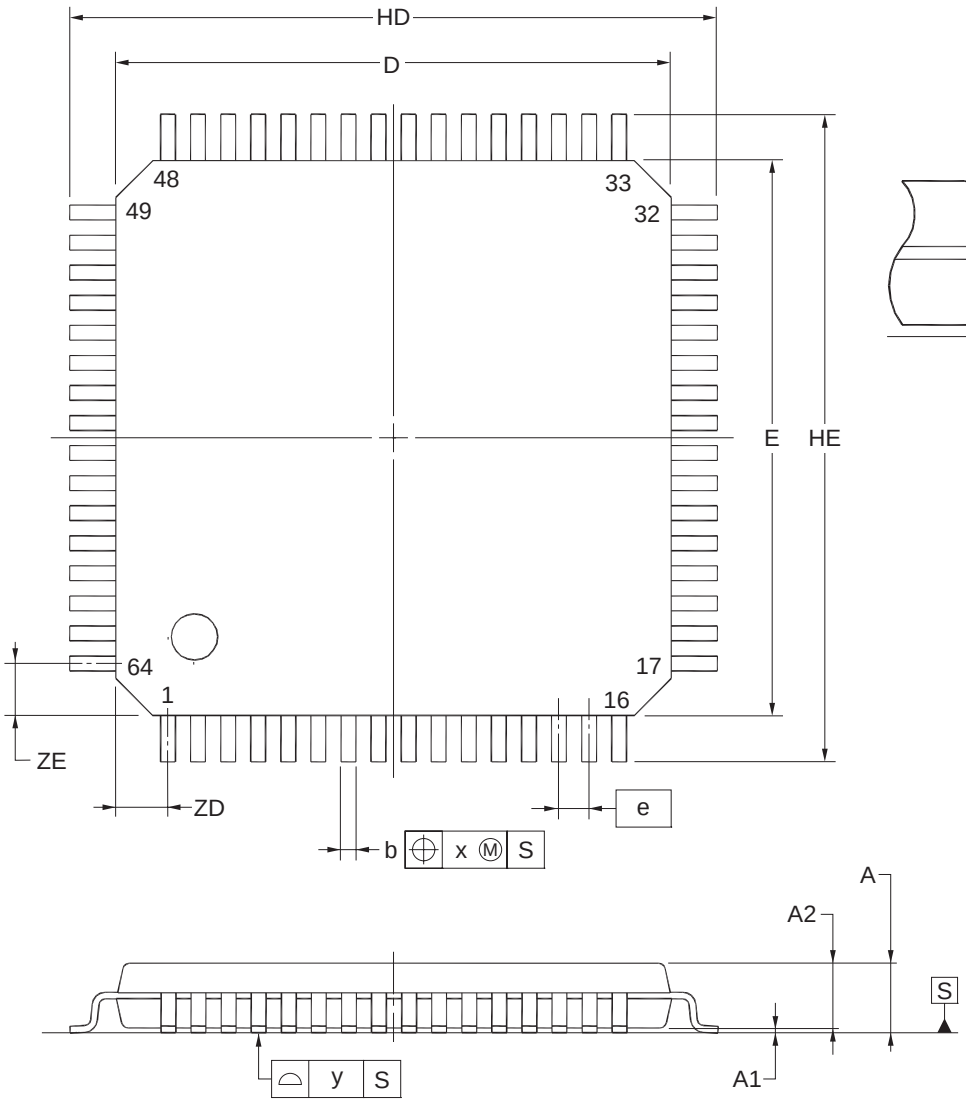
1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

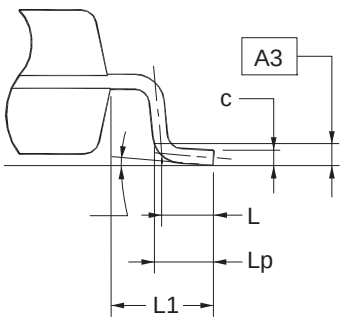
3.5 64-pin products

R5F10RLAAFA, R5F10RLCAFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{0.07}$
c	$0.145^{+0.055}_{0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3^{\circ}{}^{+5^{\circ}}_{3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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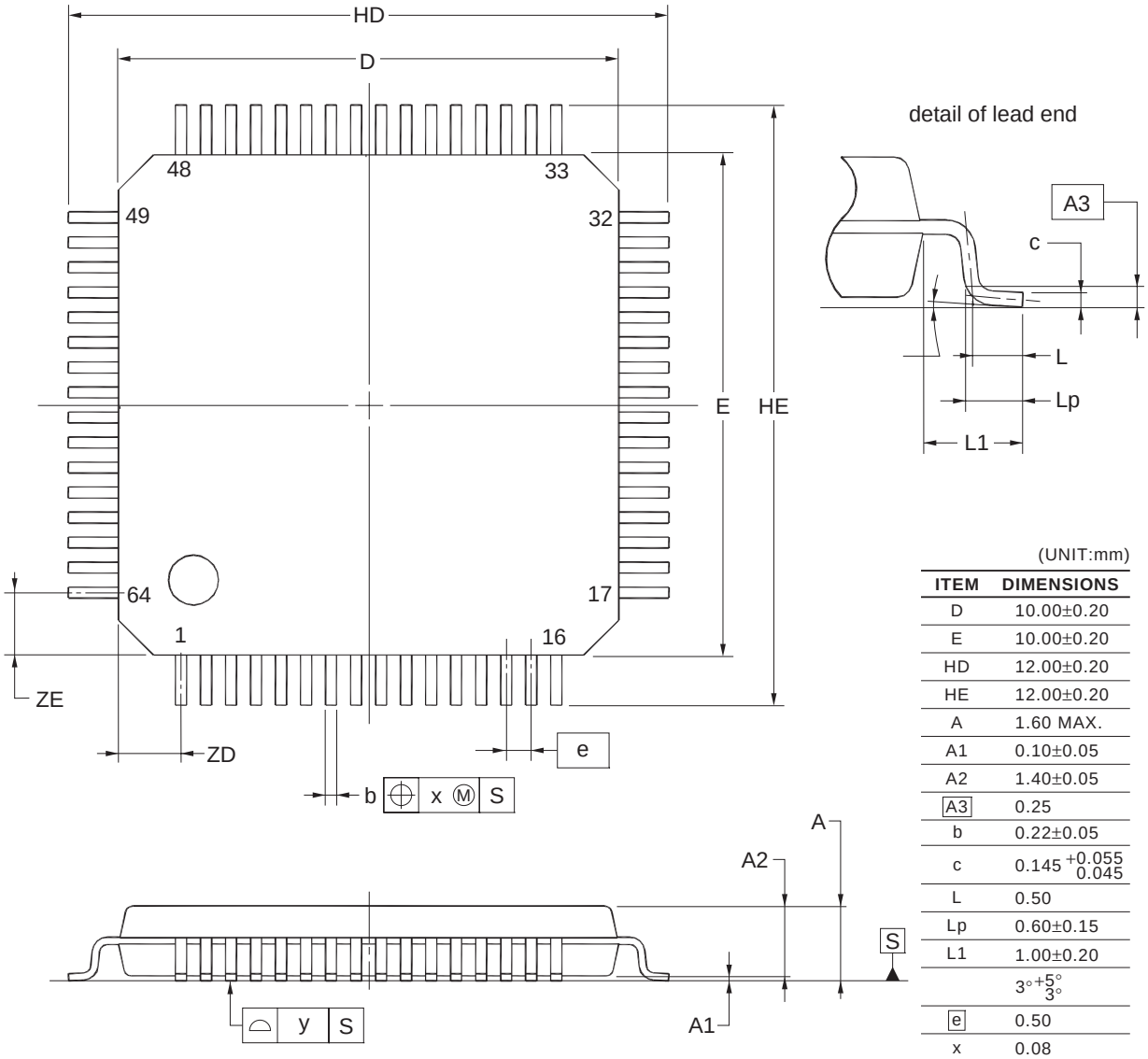
R5F10RLAAFB, R5F10RLCAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
	$3^{\circ}{}^{+5^{\circ}}_{3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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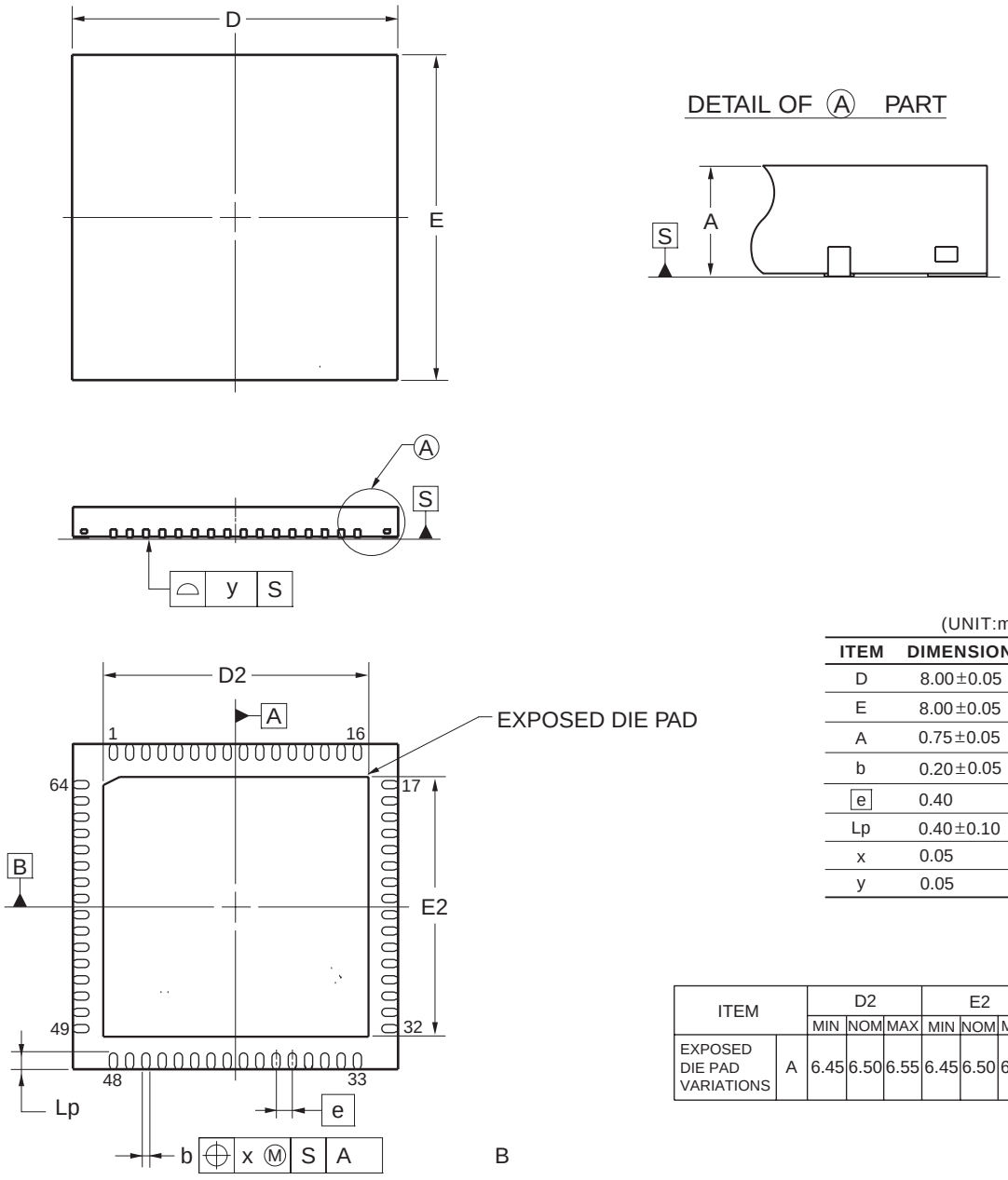
R5F10RLAANB, R5F10RLCANB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN64-8x8-0.40	PWQN0064LA-A	P64K8-40-9B5-1	0.16



(UNIT:mm)

ITEM	DIMENSIONS
D	8.00±0.05
E	8.00±0.05
A	0.75±0.05
b	0.20±0.05
e	0.40
Lp	0.40±0.10
x	0.05
y	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	6.45	6.50	6.55	6.45	6.50	6.55

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Revision History	RL78/L12 Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Feb 20, 2012	-	First Edition issued
0.02	Sep 26, 2012	7, 8	Modification of **caution 2** in **1.3.5 64-pin products**
		15	Modification of **I/O port** in **1.6 Outline of Functions**
		-	Modification of **2. ELECTRICAL SPECIFICATIONS (TARGET)**
		-	Update of package drawings in **3. PACKAGE DRAWINGS**
1.00	Jan 31, 2013	11 to 15	Modification of **1.5 Block Diagram**
		16	Modification of **Note 2** in **1.6 Outline of Functions**
		17	Modification of **1.6 Outline of Functions**
		-	Deletion of target in **2. ELECTRICAL SPECIFICATIONS**
		18	Addition of **caution 2** to **2. ELECTRICAL SPECIFICATIONS**
		19	Addition of description, **note 3**, and **remark 2** to **2.1 Absolute Maximum Ratings**
		20	Modification of description and addition of **note** to **2.1 Absolute Maximum Ratings**
		22, 23	Modification of **2.2 Oscillator Characteristics**
		30	Modification of **notes 1 to 4** in **2.3.2 Supply current characteristics**
		32	Modification of **notes 1, 3 to 6, 8** in **2.3.2 Supply current characteristics**
		34	Modification of **notes 7, 9, 11,** and addition of **notes 8, 12** to **2.3.2 Supply current characteristics**
		36	Addition of description to **2.4 AC Characteristics**
		38, 40 to 42, 44 to 46, 48 to 52, 54, 55	Modification of **2.5.1 Serial array unit**
		57, 58	Modification of **2.5.2 Serial interface IICA**
		62	Modification of **2.6.2 Temperature sensor/internal reference voltage characteristics**
		64	Addition of **note** and **caution** in **2.6.5 Supply voltage rise time**
		69	Modification of **2.8 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics**
		69	Modification of conditions in **2.9 Timing Specs for Switching Flash Memory Programming Modes**
		70	Modification of **2.10 Timing Specifications for Switching Flash Memory Programming Modes**

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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