



MOTOROLA

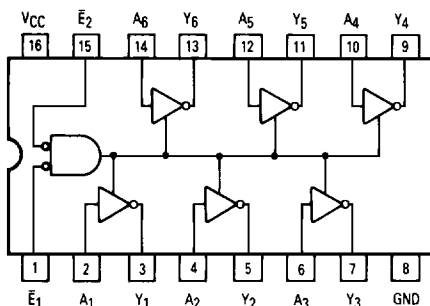
Hex Inverter, Common Enable, 3-State Outputs

**ELECTRICALLY TESTED PER:
MIL-M-38510/32202**

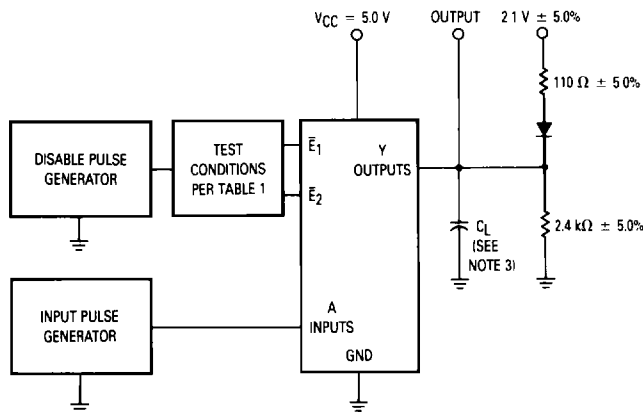
This device is a high-speed hex buffer with 3-state outputs. It is organized as a single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

LOGIC DIAGRAM



AC TEST CIRCUIT



Military 54LS366A



AVAILABLE AS:

- 1) JAN: JM38510/32202BXA
- 2) SMD: *
- 3) 883C: 54LS366A/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

***Call Factory for latest update**

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
E ₁	1	1	2	GND
A ₁	2	2	3	GND
Y ₁	3	3	4	VCC
A ₂	4	4	5	GND
Y ₂	5	5	7	VCC
A ₃	6	6	8	GND
Y ₃	7	7	9	VCC
GND	8	8	10	GND
Y ₄	9	9	12	VCC
A ₄	10	10	13	GND
Y ₅	11	11	14	VCC
A ₅	12	12	15	GND
Y ₆	13	13	17	VCC
A ₆	14	14	18	GND
E ₂	15	15	19	GND
VCC	16	16	20	VCC

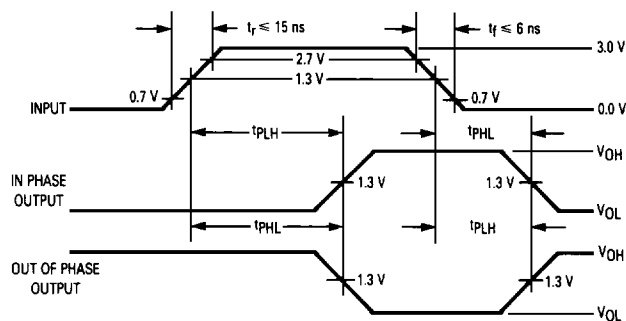
BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

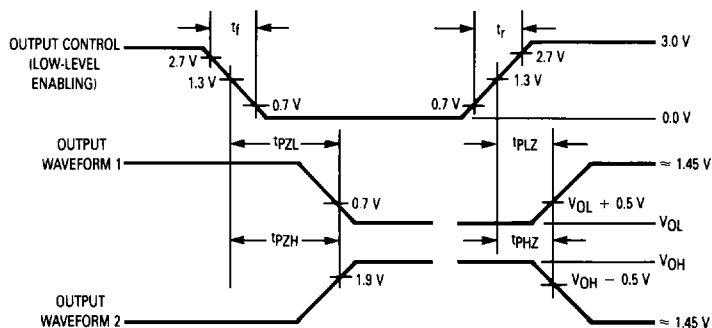
Inputs			Output
E ₁	E ₂	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

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WAVEFORMS



Voltage Waveforms Propagation Delay Times



Voltage Waveforms Enable and Disable Times, Three-State Outputs

NOTES:

1. Pulse generator has the following characteristics:
 $t_r \leq 15$ ns, $t_f \leq 6.0$ ns.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance.
4. Voltage measurements are to be made with respect to network ground terminal.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical “1” Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = − 1.0 mA, V _{IL} = 0.7 V, E _n = 0.7 V, other inputs are open.
V _{OL}	Logical “0” Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IH} = 2.0 V, E _n = 0.7 V, other inputs are open.
V _{IC}	Input Clamping Voltage		− 1.5					V	V _{CC} = 4.5 V, I _{IN} = − 18 mA, other inputs are open.
I _{IH}	Logical “1” Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH}	Logical “1” Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IL}	Logical “0” Input Current	− 160	− 400	− 160	− 400	− 160	− 400	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, E _n = 0.4 V, other inputs are open.
I _{IL(E_n)}	Logical “0” Input Current	− 160	− 400	− 160	− 400	− 160	− 400	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V (E _n), other inputs are open.
I _{OS}	Output Short Circuit Current	− 30	− 130	− 30	− 130	− 30	− 130	mA	V _{CC} = 5.5 V, V _{OUT} = GND, E _n = 0.7 V, other inputs are open.
I _{OZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.0 V, E _n = 2.0 V or 0.7 V, V _{IL} = 0.7 V, V _{OUT} = 2.4 V, other inputs are open.
I _{OZL}	Output Off Current Low		− 20		− 20		− 20	μA	V _{CC} = 5.5 V, V _{IL} = 0.7 V, E _n = 2.0 V or 0.7 V, V _{IH} = 2.0 V, V _{OUT} = 0.4 V, other inputs are open.
I _{CC}	Power Supply Current		21		21		21	mA	V _{CC} = 5.5 V, V _{IN} = GND, E _n = 4.5 V.
V _{IH}	Logical “1” Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical “0” Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V. V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Switching Parameters	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL} t _{PHL}	Propagation Delay :Data-Output Output High-Low	2.0	18 18	2.0	23 23	2.0	23 23	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PLH} t _{PLH}	Propagation Delay :Data-Output Output Low-High	2.0	15 15	2.0	20 19	2.0	20 19	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PZH} t _{PZH}	Propagation Delay :Data-Output Output High-Low	2.0	35 35	2.0	45 44	2.0	45 44	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PZL} t _{PZL}	Propagation Delay :Data-Output Output Low-High	2.0	45 45	2.0	58 56	2.0	58 56	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω.
t _{PHZ} t _{PHZ}	Propagation Delay :Data-Output Output High-Low	2.0	32 32	2.0	42 40	2.0	42 40	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 667 Ω.
t _{PLZ} t _{PLZ}	Propagation Delay :Data-Output Output Low-High	2.0	35 35	2.0	45 44	2.0	45 44	ns ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω ± 5.0%, V _{CC} = 5.0 V, C _L = 5.0 pF, R _L = 667 Ω.

NOTE:

1. The limits specified for C_L = 45 pF and C_L = 5.0 pF are guaranteed but not tested.