

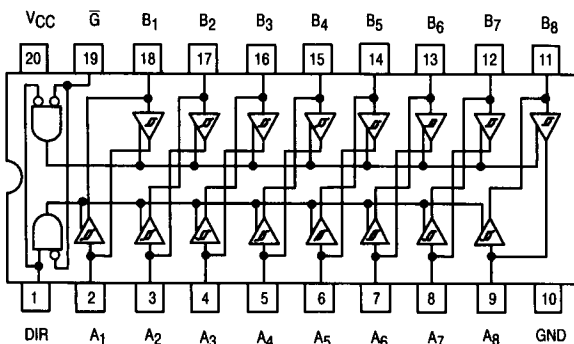


Octal Bus Transceivers With 3-State Outputs (Non-Inverting)

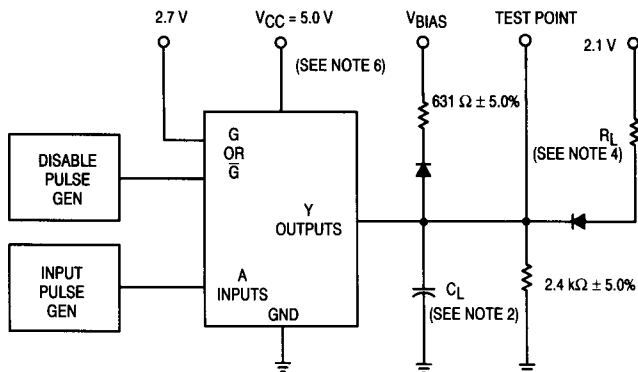
ELECTRICALLY TESTED PER:
MPG54LS645

The 54LS645 is designed for asynchronous two-way communication between data buses. Control function implementation minimizes external timing requirements. The 54LS645 allows data transmission from A bus to B or from the B bus depending upon the logic level of the direction control (DIR) input. Enable input ($\bar{G}$) can disable the device so that the buses are effectively isolated.

LOGIC DIAGRAM



AC TEST CIRCUIT



REFERENCE NOTES ON PAGE 5-415

Military 54LS645



AVAILABLE AS:

- 1) JAN: N/A
- 2) SMD: N/A
- 3) 883: 54LS645/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS
BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
DIR	1	1	1	VCC
A ₁	2	2	2	VCC
A ₂	3	3	3	VCC
A ₃	4	4	4	VCC
A ₄	5	5	5	VCC
A ₅	6	6	6	VCC
A ₆	7	7	7	VCC
A ₇	8	8	8	VCC
A ₈	9	9	9	VCC
GND	10	10	10	GND
B ₈	11	11	11	VCC
B ₇	12	12	12	VCC
B ₆	13	13	13	VCC
B ₅	14	14	14	VCC
B ₄	15	15	15	VCC
B ₃	16	16	16	VCC
B ₂	17	17	17	VCC
B ₁	18	18	18	VCC
$\bar{G}$	19	19	19	VCC
VCC	20	20	20	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

TRUTH TABLE

Control Inputs		Operation
$\bar{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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Symbol	SW1	SW2
tpZH	Open	Closed
tpZL	Closed	Open
tpLZ	Closed	Closed
tpHZ	Closed	Closed

OUTPUT CONTROL (HIGH-LEVEL ENABLING)

OUTPUT CONTROL (LOW-LEVEL ENABLING)

WAVEFORM 1

WAVEFORM 2

1.3 V

3.0 V

0.0 V

1.3 V

3.0 V

0.0 V

t_{pZL}

t_{pLZ}

t_{pZH}

t_{pHZ}

≈ 1.45 V

0.7 V

1.9 V

≈ 1.45 V

$V_{OL} + 0.5$ V

V_{OL}

V_{OH}

$V_{OH} - 0.5$ V

≈ 1.45 V

1. The pulse generator has the following characteristics:
 $V_{GEN} = 3.0\text{ V}$, $PRR = 1.0\text{ MHz}$, $t_r = 15\text{ ns}$, $t_f \leq 6.0\text{ ns}$, $Z_{OUT} = 50\ \Omega$.
2. $C_L = 50\text{ pF} \pm 10\%$, including scope probe, wiring and stray capacitance.
3. Voltage measurements are to be made with respect to network ground terminal.
4. $R_L = 110\ \Omega \pm 5.0\%$.
5. Clock pulse characteristics: $t_p(\text{CLK}) = 20\text{ ns}$, $t_{\text{setup}} = 20\text{ ns}$.
6. The diode and resistor shown within the dotted area are optional.
 When the diode and resistor are used, V_{BIAS} shall be 5.5 V for all tests except for TPH_2 ; for TPH_2 test, V_{BIAS} shall be -0.6 V .
7. All diodes are 1N3064 or equivalent.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = – 3.0 mA, V _{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\bar{G}$ = 0.7 V.
V _{OH1}	Logical "1" Output Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V, I _{OH} = – 12 mA, V _{IH} = 2.0 V (other inputs are open), DIR = 2.0 V or 0.5 V, $\bar{G}$ = 0.5 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 12 mA, V _{IL} = 0.7 V (other inputs are open), DIR = 2.0 V or 0.7 V, $\bar{G}$ = 0.7 V.
V _{IC}	Input Clamping Voltage		– 1.5					V	V _{CC} = 4.5 V, I _{IN} = – 18 mA, all other inputs are open, $\bar{G}$ = open, 5.5 V or (– 18 mA).
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open, $\bar{G}$ = open, 5.5 V or (2.7 V).
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open, $\bar{G}$ = open or 5.5 V.
I _{IL}	Logical "0" Input Current	– 5.0	– 240	– 5.0	– 240	– 5.0	– 240	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open, DIR = (0.4 V), 4.5 V or GND, $\bar{G}$ = open, 5.5 V or (0.4 V).
I _{OS}	Output Short Circuit Current	– 40	– 225	– 40	– 225	– 40	– 225	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (other inputs are open), V _{OUT} = GND, DIR = 5.5 V or GND, $\bar{G}$ = GND.
I _{OZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{OZL}	Output Off Current Low		– 200		– 200		– 200	μA	V _{CC} = 5.5 V, V _{IL} = 0.4 V, other inputs are open.
I _{CCH}	Power Supply Current		70		70		70	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V (all inputs), $\bar{G}$ & DIR = GND.
I _{CCL}	Power Supply Current		90		90		90	mA	V _{CC} = 5.5 V, V _{IN} = GND (all inputs).
I _{CCZ}	Power Supply Current Off		95		95		95	mA	V _{CC} = 5.5 V, all inputs are open, $\bar{G}$ = 5.5 V.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{INH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		– 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL} t _{PHL}	Propagation Delay /Data-Output A to B	2.0 —	17 15	2.0 —	22 19	2.0 —	22 19	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω
t _{PLH} t _{PLH}	Propagation Delay /Data-Output A to B	2.0 —	17 15	2.0 —	22 19	2.0 —	22 19	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω
t _{PLZ} t _{PLZ}	Propagation Delay Output Disable Time, $\bar{G}$, DIR to A	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 5.0 pF.
t _{PHZ} t _{PHZ}	Propagation Delay Output Disable Time, $\bar{G}$, DIR to A	2.0 —	30 25	2.0 —	39 34	2.0 —	39 34	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 5.0 pF.
t _{PZL} t _{PZL}	Propagation Delay Output Enable Time $\bar{G}$, DIR to A	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω
t _{PZH} t _{PZH}	Propagation Delay Output Enable Time $\bar{G}$, DIR to A	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 110 Ω V _{CC} = 5.0 V, C _L = 45 pF, R _L = 667 Ω