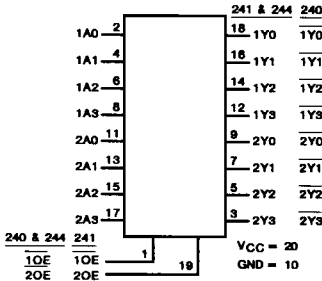


CD54/74FCT240, CD54/74FCT240AT
CD54/74FCT241, CD54/74FCT241AT
CD54/74FCT244, CD54/74FCT244AT

July 1990



FUNCTIONAL DIAGRAM

Octal Buffers/Line Drivers, 3-State

CD54/74FCT240, CD54/74FCT240AT - Inverting
 CD54/74FCT241, CD54/74FCT241AT - Non-Inverting
 CD54/74FCT244, CD54/74FCT244AT - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
 4.1ns @ $V_{CC} = 5V$, $T_A = +25^\circ C$, $C_L = 50pF$ (FCT240AT, FCT244AT)

Family Features:

- SCR-latchup-resistant BiCMOS process and circuit design
- FCTXXX Types - Speed of bipolar FAST*/AS/S;
 FCTXXXAT Types - 30% faster than FAST/AS/S with
 significantly reduced power consumption
- 64/48-mA output sink current (commercial/extended
 industrial)
- Output voltage swing limited to 3.7V @ $V_{CC} = 5V$
- Controlled output-edge rates
- Input/output isolation to V_{CC}
- BiCMOS technology with low quiescent power

* FAST is a registered trademark of Fairchild Semiconductor Corp.

The CD54/74FCT240, 240AT, 241, 241AT, 244 and 244AT 3-state octal buffers/line drivers use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below V_{CC} . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 to 64 milliamperes.

The CD54/74FCT240, 240AT, 244 and 244AT have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74FCT241 and CD54/74FCT241AT have one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

The CD54/74FCT240, 240AT, 241, 241AT, 244 and 244AT are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial ($0^\circ C$ to $+70^\circ C$) and Extended Industrial ($-55^\circ C$ to $+125^\circ C$).

The CD54FCT240, 241 and 244 are also available in chip form (H suffix). These unpackaged devices are operable over the $-55^\circ C$ to $+125^\circ C$ temperature range.

TRUTH TABLES

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

(FCT240, FCT240AT)

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

(FCT244, FCT244AT)

INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{1OE}$	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

(FCT241, FCT241AT)

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance

File No. 2227 — CD54/74FCT240, CD54/74FCT240AT, CD54/74FCT241, CD54/74FCT241AT, CD54/74FCT244, CD54/74FCT244AT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5V to 6V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5V$)	-20mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5V$)	-50mA
DC OUTPUT SINK CURRENT per Output Pin, I_O	+70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I_O	-30mA
DC V_{CC} CURRENT (I_{CC})	140mA
DC GROUND CURRENT (I_{GND})	528mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ (PACKAGE TYPE E)	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8mW/ $^\circ\text{C}$ to 300mW
For $T_A = -55^\circ\text{C}$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400mW
For $T_A = +70^\circ\text{C}$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6mW/ $^\circ\text{C}$ to 70mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE E, M	-55 $^\circ\text{C}$ to +125 $^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 in. $\pm$ 1/32 in. (1.59mm $\pm$ 0.79mm) from case for 10s maximum	+265 $^\circ\text{C}$
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only	+300 $^\circ\text{C}$

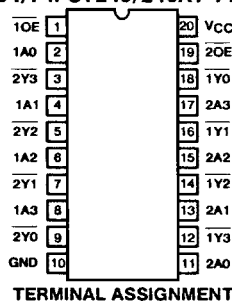
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

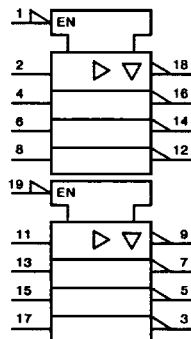
CHARACTERISTIC		LIMITS		UNITS
		MIN	MAX	
Supply-Voltage Range, V_{CC}^* :	CD74 Series, $T_A = 0^{\circ}\text{C}$ to 70°C	4.75	5.25	V
	CD54 Series, $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	4.5	5.5	V
DC Input Voltage, V_I		0	V_{CC}	V
DC Output Voltage, V_O		0	$\leq V_{CC}$	V
Operating Temperature, T_A		-55	+125	$^{\circ}\text{C}$
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT240/240AT TYPES

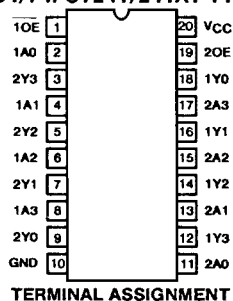


TERMINAL ASSIGNMENT

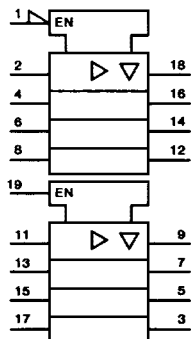


IEC LOGIC SYMBOL

CD54/74FCT241/241AT TYPES

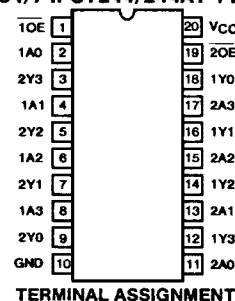


TERMINAL ASSIGNMENT

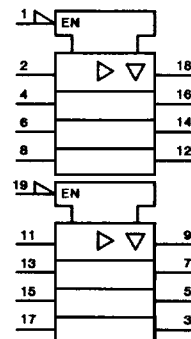


IEC LOGIC SYMBOL

CD54/74FCT244/244AT TYPES



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; V_{CC} max = 5.25V, V_{CC} min = 4.75V54FCT Extended Industrial Temperature Range, -55°C to +125°C; V_{CC} max = 5.5V, V_{CC} min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	V _{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	V _{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-15	MIN	2.4	-	2.4	-	-	-	V
			-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	64	MIN	-	0.55	-	0.55	-	-	V
			48	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I _{IH}	V _{CC}		MAX	-	0.1	-	1	-	1	μA
Low-Level Input Current	I _{IL}	GND		MAX	-	-0.1	-	-1	-	-1	μA
3-State Leakage Current	I _{OZH}	V _{CC}		MAX	-	0.5	-	10	-	10	μA
	I _{OZL}	GND		MAX	-	-0.5	-	-10	-	-10	μA
Short-Circuit Output Current *	I _{OS}	V _{CC} or GND V _O = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	MAX	-	8	-	80	-	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI _{CC}	3.4V†		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

† Inputs that are not measured are at V_{CC} or GND.FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

SWITCHING CHARACTERISTICS

FCT Series: $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L - See Figure 2

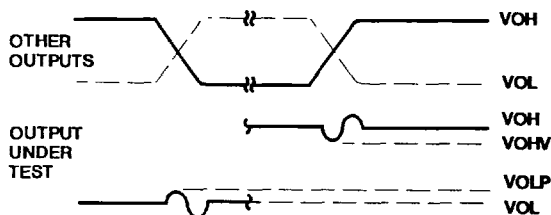
CHARACTERISTICS		SYMBOL	V _{CC} (V)	CD54/74FCT240, 241, 244						CD54/74FCT240AT, 241AT*, 244AT						UNITS
				AMBIENT TEMPERATURE (T _A)												
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C				
					TYP	MIN	MAX	MIN		MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays: Data to Outputs	FCT240/AT	t _{PLH} , t _{PHL}	5†	5	1.5	8	1.5	9	4.4	1.5	5.6	1.5	6.7	ns		
	FCT241/AT	t _{PLH} , t _{PHL}	5	4	1.5	6.5	1.5	7						ns		
	FCT244/AT	t _{PLH} , t _{PHL}	5	4.5	1.5	6.5	1.5	7	3.8	1.5	5.3	1.5	6.2	ns		
Output Enable Times	FCT240/AT	t _{PZL} , t _{PZH}	5	7	1.5	10	1.5	10.5	4.7	1.5	6.2	1.5	7.7	ns		
	FCT241/AT	t _{PZL} , t _{PZH}	5	5.5	1.5	8	1.5	8.5						ns		
	FCT244/AT	t _{PZL} , t _{PZH}	5	6	1.5	8	1.5	8.5	4.8	1.5	6.5	1.5	7.8	ns		
Output Disable Times	FCT240/AT	t _{PLZ} , t _{PHZ}	5	6	1.5	9.5	1.5	10	4	1.5	5.6	1.5	6.5	ns		
	FCT241/AT	t _{PLZ} , t _{PHZ}	5	4.5	1.5	7	1.5	7.5						ns		
	FCT244/AT	t _{PLZ} , t _{PHZ}	5	5	1.5	7	1.5	7.5	4.5	1.5	5.8	1.5	6.8	ns		
Power Dissipation Capacitance	FCT240/AT,	C _{PD} §		38 Typical						38 Typical						pF
	FCT241/AT,	C _{PD} §		33 Typical						33 Typical						pF
	FCT244/AT	C _{PD} §		35 Typical						35 Typical						pF
Min. (Valley) V _{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V _{OHV} See Figure 1	5	0.5 Typical @ +25°C										V		
Max. (Peak) V _{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V _{OLP} See Figure 1	5	1 Typical @ +25°C										V		
Input Capacitance		C _I	-	-	-	10	-	10	-	-	10	-	10	pF		
3-State Output Capacitance		C _O	-	-	-	15	-	15	-	-	15	-	15	pF		

†5V: min. is @ 5.5V
max. is @ 4.5V5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

* Contact local Sales Office for availability

§ C_{PD} , measured per function, is used to determine the dynamic power consumption.
 P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_o C_L + V_{CC} \Delta I_{CCD})$ where:
 V_{CC} = supply voltage
 ΔI_{CC} = flow through current x unit load
 C_L = output load capacitance
 D = duty cycle of input high
 f_o = output frequency
 f_i = input frequency

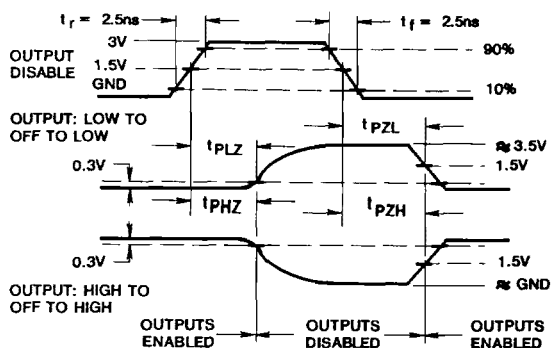
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics:
PRR $\leq$ 1MHz, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1 μF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.



TEST	SWITCH POSITION
t_{PLZ} , t_{PZL} , OPEN DRAIN	CLOSED
t_{PHZ} , t_{PZH} , t_{PLH} , t_{PHL}	OPEN

Figure 2 - Three-state propagation delay times and test circuit.

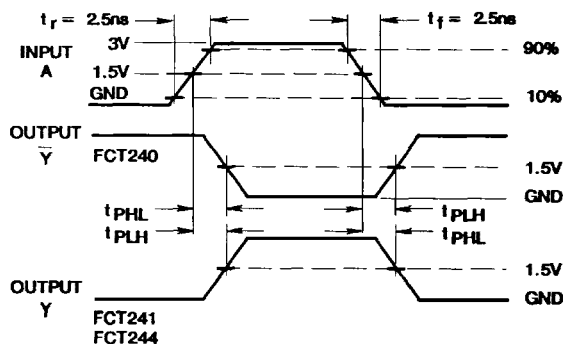


Figure 3 - Propagation delay times.