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NTE74LS377

Integrated Circuit

TTL – Octal D-Type Flip-Flop with Enable

Description:

The NTE74LS377 is a hex monolithic, positive-edge-triggered flip-flop in a 20-Lead plastic DIP type package that utilizes TTL circuitry to implement D-type flip-flop logic with an enable input. The NTE74LS377 is similar to the NTE74LS173 but features a common enable instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input $\overline{G}$ is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect on the output. The circuit is designed to prevent false clocking by transitions at the $\overline{G}$ input.

The flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30Mhz while maximum clock frequency is typically 40Mhz. Typical power dissipation is 10mW per flip-flop.

Features:

- Contains Eight Flip-Flops with Single Rail Outputs
- Individual Data Input to Each Flip-Flop

Applications:

- Buffer/Storage Registers
- Shift Registers
- Pattern Generators

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC}	7V
DC Input Voltage, V_{IN}	7V
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_{stg}	-65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High-Level Output Current	I_{OH}	–	–	–400	μA
Low-Level Output Current	I_{OL}	–	–	8	mA
Clock Frequency	f_{clock}	0	–	30	MHz
Width of Clock Pulse	t_w	20	–	–	ns
Setup Time Data Input	t_{su}	20 $\uparrow$	–	–	ns
Enable Active-State		25 $\uparrow$	–	–	ns
Enable Inactive-State		10 $\uparrow$	–	–	ns
Hold Time	t_h	5 $\uparrow$	–	–	ns
Operating Temperature Range	T_A	0	–	+70	$^{\circ}C$

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2	–	–	V
Low Level Input Voltage	V_{IL}		–	–	0.8	V
Input Clamp Voltage	V_{IK}	$V_{CC} = \text{MIN}, I_I = -18\text{mA}$	–	–	–1.5	V
High Level Output Voltage	V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = \text{MAX}, I_{OH} = -400\mu A$	2.7	3.5		V
Low Level Output Voltage	V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2V, V_{IL} = \text{MAX}$ $I_{OL} = 4\text{mA}$	–	0.25	0.4	V
			–	0.35	0.5	V
Input Current	I_I	$V_{CC} = \text{MAX}, V_I = 7V$	–	–	0.1	mA
High Level Input Current	I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.7V$	–	–	20	μA
Low Level Input Current	I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4V$	–	–	–0.4	mA
Short-Circuit Output Current	I_{OS}	$V_{CC} = \text{MAX}, \text{Note 4}$	–20	–	–100	mA
Supply Current	I_{CC}	$V_{CC} = \text{MAX}, \text{Note 5}$	–	17	28	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at $V_{CC} = 5V, T_A = +25^{\circ}C$.

Note 4. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Note 4. With all outputs open and ground applied to all data inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Switching Characteristics: ($V_{CC} = 5V, T_A = +25^{\circ}C$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	f_{max}	$R_L = 2k\Omega, C_L = 15pF$	30	40	–	MHz
Propagation Delay Time, from Clock	t_{PLH}		–	17	27	ns
	t_{PHL}		–	18	27	ns

Function Table (Each Flip-Flop):

Inputs			Outputs	
$\overline{G}$	Clock	Data	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	$\uparrow$	H	H	L
L	$\uparrow$	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

Pin Connection Diagram

