

## DS90CR563/DS90CR564

### LVDS 18-Bit Color Flat Panel Display (FPD) Link—65 MHz

#### General Description

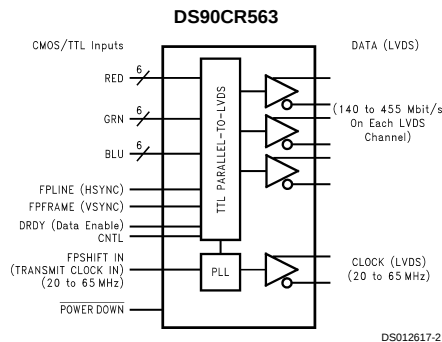
The DS90CR563 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR564 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 171 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

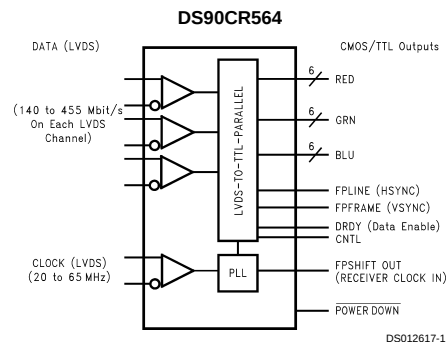
#### Features

- 20 to 65 MHz shift clk support
- Up to 171 Mbytes/s bandwidth
- Cable size is reduced to save cost
- 290 mV swing LVDS devices for low EMI
- Low power CMOS design (< 550 mW typ)
- Power-down mode saves power (< 0.25 mW)
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Single pixel per clock XGA (1024 x 768)
- Supports VGA, SVGA, XGA and higher
- 1.3 Gbps throughput

#### Block Diagrams

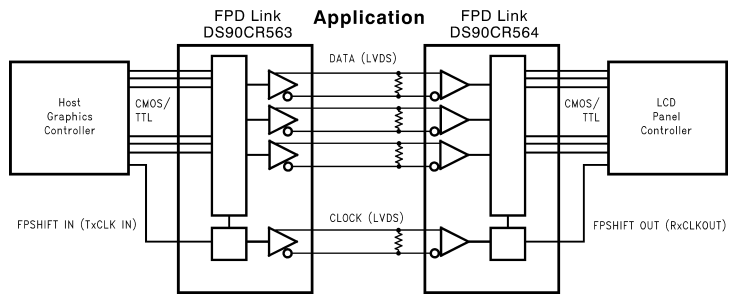


Order Number DS90CR563MTD  
See NS Package Number MTD48



Order Number DS90CR564MTD  
See NS Package Number MTD48

## Block Diagrams (Continued)



DS012617-3

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

|                                           |                              |
|-------------------------------------------|------------------------------|
| Supply Voltage ( $V_{CC}$ )               | –0.3V to +6V                 |
| CMOS/TTL Input Voltage                    | –0.3V to ( $V_{CC} + 0.3V$ ) |
| CMOS/TTL Output Voltage                   | –0.3V to ( $V_{CC} + 0.3V$ ) |
| LVDS Receiver Input Voltage               | –0.3V to ( $V_{CC} + 0.3V$ ) |
| LVDS Driver Output Voltage                | –0.3V to ( $V_{CC} + 0.3V$ ) |
| LVDS Output Short Circuit Duration        | Continuous                   |
| Junction Temperature                      | +150°C                       |
| Storage Temperature                       | –65°C to +150°C              |
| Lead Temperature (Soldering, 4 sec)       | +260°C                       |
| Maximum Package Power Dissipation @ +25°C |                              |
| MTD48 (TSSOP) Package:                    |                              |

|                                                      |                      |
|------------------------------------------------------|----------------------|
| DS90CR563                                            | 1.98W                |
| DS90CR564                                            | 1.89W                |
| Package Derating:                                    |                      |
| DS90CR563                                            | 16 mW/°C above +25°C |
| DS90CR564                                            | 15 mW/°C above +25°C |
| This device does not meet 2000V ESD rating (Note 4). |                      |

## Recommended Operating Conditions

|                                          | Min  | Nom | Max  | Units             |
|------------------------------------------|------|-----|------|-------------------|
| Supply Voltage ( $V_{CC}$ )              | 4.75 | 5.0 | 5.25 | V                 |
| Operating Free Air Temperature ( $T_A$ ) | –10  | +25 | +70  | °C                |
| Receiver Input Range                     | 0    |     | 2.4  | V                 |
| Supply Noise Voltage ( $V_{CC}$ )        |      |     | 100  | mV <sub>P-P</sub> |

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol                          | Parameter                                                     | Conditions                                                                        | Min                    | Typ   | Max             | Units |    |
|---------------------------------|---------------------------------------------------------------|-----------------------------------------------------------------------------------|------------------------|-------|-----------------|-------|----|
| CMOS/TTL DC SPECIFICATIONS      |                                                               |                                                                                   |                        |       |                 |       |    |
| V <sub>IH</sub>                 | High Level Input Voltage                                      |                                                                                   | 2.0                    |       | V <sub>CC</sub> | V     |    |
| V <sub>IL</sub>                 | Low Level Input Voltage                                       |                                                                                   | GND                    |       | 0.8             | V     |    |
| V <sub>OH</sub>                 | High Level Output Voltage                                     | I <sub>OH</sub> = -0.4 mA                                                         | 3.8                    | 4.9   |                 | V     |    |
| V <sub>OL</sub>                 | Low Level Output Voltage                                      | I <sub>OL</sub> = 2 mA                                                            |                        | 0.1   | 0.3             | V     |    |
| V <sub>CL</sub>                 | Input Clamp Voltage                                           | I <sub>CL</sub> = -18 mA                                                          |                        | -0.79 | -1.5            | V     |    |
| I <sub>IN</sub>                 | Input Current                                                 | V <sub>IN</sub> = V <sub>CC</sub> , GND, 2.5V or 0.4V                             |                        | ±5.1  | ±10             | µA    |    |
| I <sub>OS</sub>                 | Output Short Circuit Current                                  | V <sub>OUT</sub> = 0V                                                             |                        |       | -120            | mA    |    |
| LVDS DRIVER DC SPECIFICATIONS   |                                                               |                                                                                   |                        |       |                 |       |    |
| V <sub>OD</sub>                 | Differential Output Voltage                                   | R <sub>L</sub> = 100Ω                                                             | 250                    | 290   | 450             | mV    |    |
| ΔV <sub>OD</sub>                | Change in V <sub>OD</sub> between Complementary Output States |                                                                                   |                        |       | 35              | mV    |    |
| V <sub>CM</sub>                 | Common Mode Voltage                                           |                                                                                   | 1.1                    | 1.25  | 1.375           | V     |    |
| ΔV <sub>CM</sub>                | Change in V <sub>CM</sub> between Complementary Output States |                                                                                   |                        |       | 35              | mV    |    |
| V <sub>OH</sub>                 | High Level Output Voltage                                     |                                                                                   |                        | 1.3   | 1.6             | V     |    |
| V <sub>OL</sub>                 | Low Level Output Voltage                                      |                                                                                   | 0.9                    | 1.01  |                 | V     |    |
| I <sub>OS</sub>                 | Output Short Circuit Current                                  | V <sub>OUT</sub> = 0V, R <sub>L</sub> = 100Ω                                      |                        |       | -2.9            | -5    | mA |
| I <sub>OZ</sub>                 | Output TRI-STATE® Current                                     | Power Down = 0V, V <sub>OUT</sub> = 0V or V <sub>CC</sub>                         |                        |       | ±1              | ±10   | µA |
| LVDS RECEIVER DC SPECIFICATIONS |                                                               |                                                                                   |                        |       |                 |       |    |
| V <sub>TH</sub>                 | Differential Input High Threshold                             | V <sub>CM</sub> = +1.2V                                                           |                        |       |                 | +100  | mV |
| V <sub>TL</sub>                 | Differential Input Low Threshold                              |                                                                                   |                        | -100  |                 |       | mV |
| I <sub>IN</sub>                 | Input Current                                                 | V <sub>IN</sub> = +2.4V                                                           | V <sub>CC</sub> = 5.5V |       |                 | ±10   | µA |
|                                 |                                                               | V <sub>IN</sub> = 0V                                                              |                        |       |                 | ±10   | µA |
| TRANSMITTER SUPPLY CURRENT      |                                                               |                                                                                   |                        |       |                 |       |    |
| I <sub>CCTW</sub>               | Transmitter Supply Current, Worst Case                        | R <sub>L</sub> = 100Ω, C <sub>L</sub> = 5 pF, Worst Case Pattern (Figures 1, 3)   | f = 32.5 MHz           |       | 49              | 63    | mA |
|                                 |                                                               |                                                                                   | f = 37.5 MHz           |       | 51              | 64    | mA |
|                                 |                                                               |                                                                                   | f = 65 MHz             |       | 70              | 84    | mA |
| I <sub>CCTG</sub>               | Transmitter Supply Current, 16 Grayscale                      | R <sub>L</sub> = 100Ω, C <sub>L</sub> = 5 pF, 16 Grayscale Pattern (Figures 2, 3) | f = 32.5 MHz           |       | 40              | 55    | mA |
|                                 |                                                               |                                                                                   | f = 37.5 MHz           |       | 41              | 55    | mA |
|                                 |                                                               |                                                                                   | f = 65 MHz             |       | 55              | 67    | mA |

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol                            | Parameter                              | Conditions                                        | Min            | Typ | Max | Units   |
|-----------------------------------|----------------------------------------|---------------------------------------------------|----------------|-----|-----|---------|
| <b>TRANSMITTER SUPPLY CURRENT</b> |                                        |                                                   |                |     |     |         |
| $I_{CCTZ}$                        | Transmitter Supply Current, Power Down | Power Down = Low                                  |                | 1   | 25  | $\mu A$ |
| <b>RECEIVER SUPPLY CURRENT</b>    |                                        |                                                   |                |     |     |         |
| $I_{CCRW}$                        | Receiver Supply Current, Worst Case    | $C_L = 8$ pF, Worst Case Pattern (Figures 1, 4)   | $f = 32.5$ MHz |     | 64  | 77 mA   |
|                                   |                                        |                                                   | $f = 37.5$ MHz |     | 70  | 85 mA   |
|                                   |                                        |                                                   | $f = 65$ MHz   |     | 110 | 140 mA  |
| $I_{CCRG}$                        | Receiver Supply Current, 16 Grayscale  | $C_L = 8$ pF, 16 Grayscale Pattern (Figures 2, 4) | $f = 32.5$ MHz |     | 35  | 55 mA   |
|                                   |                                        |                                                   | $f = 37.5$ MHz |     | 37  | 55 mA   |
|                                   |                                        |                                                   | $f = 65$ MHz   |     | 55  | 67 mA   |
| $I_{CCRZ}$                        | Receiver Supply Current, Power Down    | Power Down = Low                                  |                | 1   | 10  | $\mu A$ |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

**Note 2:** Typical values are given for  $V_{CC} = 5.0V$  and  $T_A = +25^\circ C$ .

**Note 3:** Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except  $V_{OD}$  and  $\Delta V_{OD}$ ).

**Note 4:** ESD Rating: HBM (1.5 k $\Omega$ , 100 pF)

PLL  $V_{CC} \geq 1000V$

All other pins  $\geq 2000V$

EIAJ (0 $\Omega$ , 200 pF)  $\geq 150V$

## Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter                                                               | Min          | Typ   | Max           | Units |
|--------|-------------------------------------------------------------------------|--------------|-------|---------------|-------|
| LLHT   | LVDS Low-to-High Transition Time (Figure 3)                             |              | 0.75  | 1.5           | ns    |
| LHLT   | LVDS High-to-Low Transition Time (Figure 3)                             |              | 0.75  | 1.5           | ns    |
| TCIT   | TxCLK IN Transition Time (Figure 5)                                     |              |       | 8             | ns    |
| TCCS   | TxOUT Channel-to-Channel Skew (Note 5) (Figure 6)                       |              |       | 350           | ps    |
| TCCD   | TxCLK IN to TxCLK OUT Delay @ $25^\circ C$ , $V_{CC} = 5.0V$ (Figure 9) | 3.5          |       | 8.5           | ns    |
| TCIP   | TxCLK IN Period (Figure 7)                                              | 15           | T     | 50            | ns    |
| TCIH   | TxCLK IN High Time (Figure 7)                                           | 0.35T        | 0.5T  | 0.65T         | ns    |
| TCIL   | TxCLK IN Low Time (Figure 7)                                            | 0.35T        | 0.5T  | 0.65T         | ns    |
| TSTC   | TxIN Setup to TxCLK IN (Figure 7)                                       | $f = 65$ MHz | 5     | 3.5           | ns    |
| THTC   | TxIN Hold to TxCLK IN (Figure 7)                                        |              | 2.5   | 1.5           | ns    |
| TPDD   | Transmitter Powerdown Delay (Figure 18)                                 |              |       | 100           | ns    |
| TPLLS  | Transmitter Phase Lock Loop Set (Figure 11)                             |              |       | 10            | ms    |
| TPPos0 | Transmitter Output Pulse Position 0 (Figure 13)                         |              | -0.30 | 0             | ns    |
| TPPos1 | Transmitter Output Pulse Position 1                                     |              | 1.70  | $1/7 T_{clk}$ | ns    |
| TPPos2 | Transmitter Output Pulse Position 2                                     |              | 3.60  | $2/7 T_{clk}$ | ns    |
| TPPos3 | Transmitter Output Pulse Position 3                                     |              | 5.90  | $3/7 T_{clk}$ | ns    |
| TPPos4 | Transmitter Output Pulse Position 4                                     |              | 8.30  | $4/7 T_{clk}$ | ns    |
| TPPos5 | Transmitter Output Pulse Position 5                                     |              | 10.40 | $5/7 T_{clk}$ | ns    |
| TPPos6 | Transmitter Output Pulse Position 6                                     |              | 12.70 | $6/7 T_{clk}$ | ns    |

**Note 5:** This limit based on bench characterization.

## Receiver Switching Characteristics

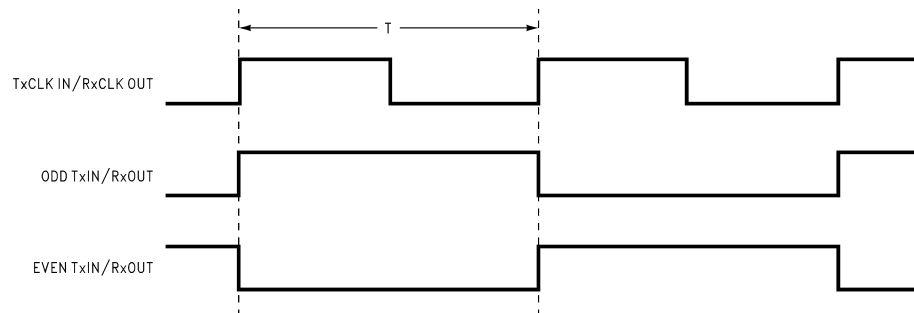
Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol | Parameter                                                              | Min                                         | Typ | Max  | Units |
|--------|------------------------------------------------------------------------|---------------------------------------------|-----|------|-------|
| CLHT   | CMOS/TTL Low-to-High Transition Time (Figure 4)                        |                                             | 2.5 | 4.0  | ns    |
| CHLT   | CMOS/TTL High-to-Low Transition Time (Figure 4)                        |                                             | 2.0 | 3.5  | ns    |
| RCOP   | RxCLK OUT Period                                                       | 15                                          | T   | 50   | ns    |
| RCOH   | RxCLK OUT High Time                                                    | f = 65 MHz                                  | 3.8 | 5    | ns    |
| RCOL   | RxCLK OUT Low Time                                                     | f = 65 MHz                                  | 7.8 | 9    | ns    |
| RSRC   | RxOUT Setup to RxCLK OUT                                               | f = 65 MHz                                  | 2.5 | 4.2  | ns    |
| RHRC   | RxOUT Hold to RxCLK OUT                                                | f = 65 MHz                                  | 4.0 | 5.2  | ns    |
| RCCD   | RxCLK IN to RxCLK OUT Delay @ 25°C, V <sub>CC</sub> = 5.0V (Figure 10) | 6.4                                         |     | 10.7 | ns    |
| RPLLS  | Receiver Phase Lock Loop Set (Figure 12)                               |                                             |     | 10   | ms    |
| RSKM   | RxIN Skew Margin (Note 6) (Figure 14)                                  | V <sub>CC</sub> = 5V, T <sub>A</sub> = 25°C | 600 |      | ps    |
| RPDD   | Receiver Powerdown (Figure 17)                                         |                                             |     | 1    | μs    |

**Note 6:** Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account transmitter output skew (TCCS) and the setup and hold time (internal data sampling window), allowing for LVDS cable skew dependent on type/length and source clock (TxCLK IN) jitter.

$RSKM \geq \text{cable skew (type, length)} + \text{source clock jitter (cycle to cycle)}$

## AC Timing Diagrams



DS012617-4

FIGURE 1. "Worst Case" Test Pattern

## AC Timing Diagrams (Continued)

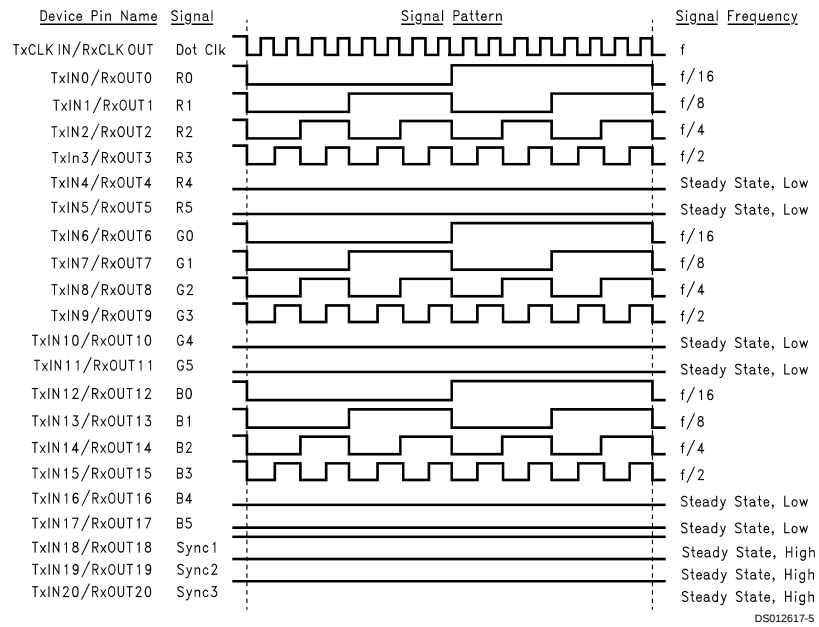


FIGURE 2. "16 Grayscale" Test Pattern

**Note 7:** The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

**Note 8:** The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

**Note 9:** Figure 1 and Figure 2 show a falling edge data strobe (TxCLK IN/RxCLOCK OUT).

**Note 10:** Recommended pin to signal mapping. Customer may choose to define differently.

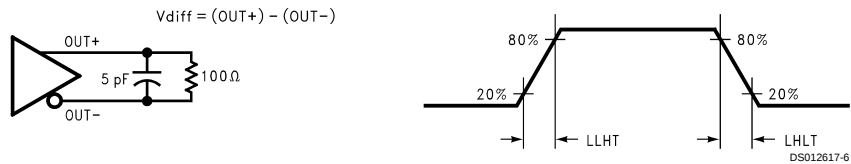


FIGURE 3. DS90CR563 (Transmitter) LVDS Output Load and Transition Times

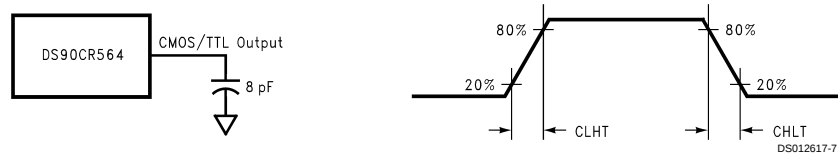


FIGURE 4. DS90CR564 (Receiver) CMOS/TTL Output Load and Transition Times

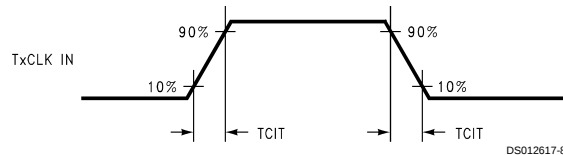
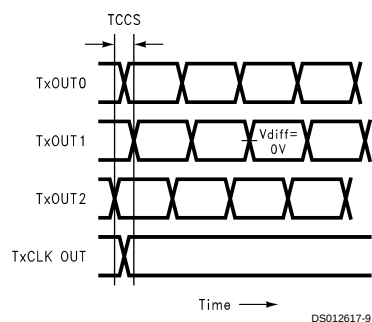


FIGURE 5. DS90CR563 (Transmitter) Input Clock Transition Time

## AC Timing Diagrams (Continued)

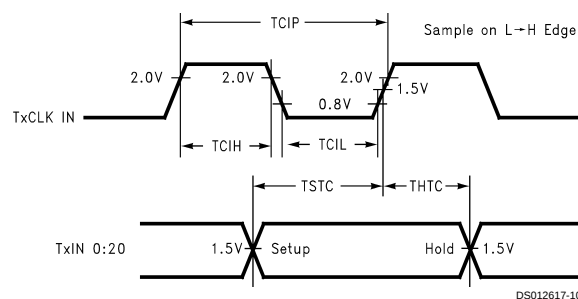


**Note:** Measurements at  $V_{diff} = 0V$

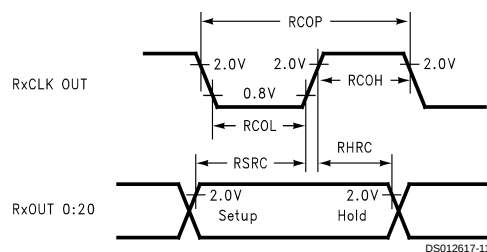
**Note:** TCSS measured between earliest and latest LVDS edges.

**Note:** TxCLK Differential High→Low Edge

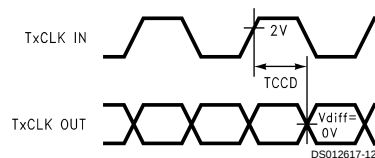
**FIGURE 6. DS90CR563 (Transmitter) Channel-to-Channel Skew and Pulse Width**



**FIGURE 7. DS90CR563 Setup/Hold and High/Low Times**



**FIGURE 8. DS90CR564 Setup/Hold and High/Low Times**



**FIGURE 9. DS90CR563 (Transmitter) Clock In to Clock Out Delay**

## AC Timing Diagrams (Continued)

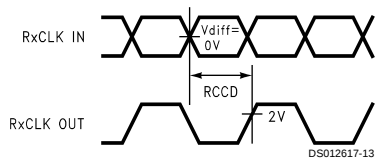


FIGURE 10. DS90CR564 (Receiver) Clock In to Clock Out Delay

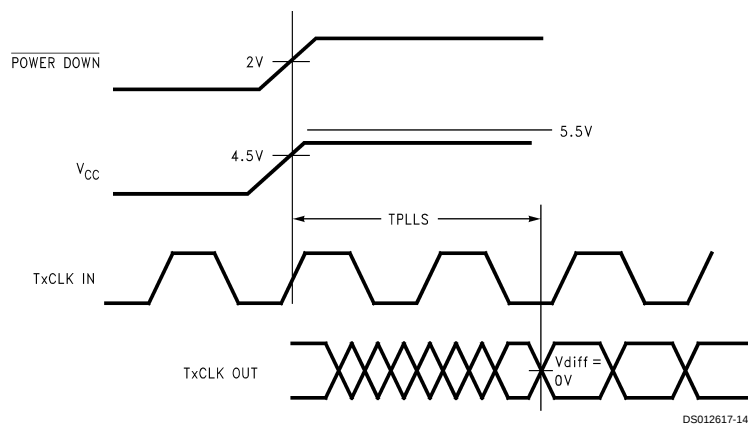


FIGURE 11. DS90CR563 (Transmitter) Phase Lock Loop Set Time

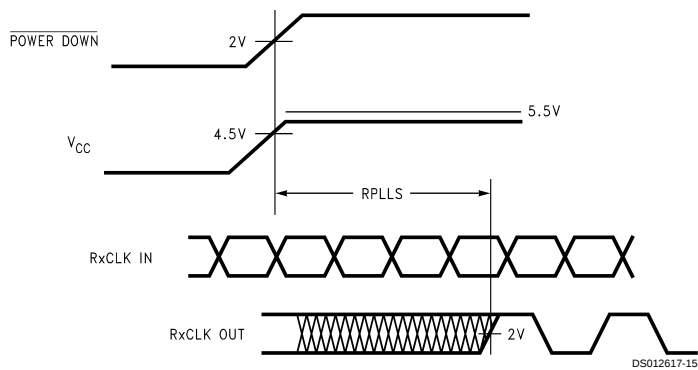
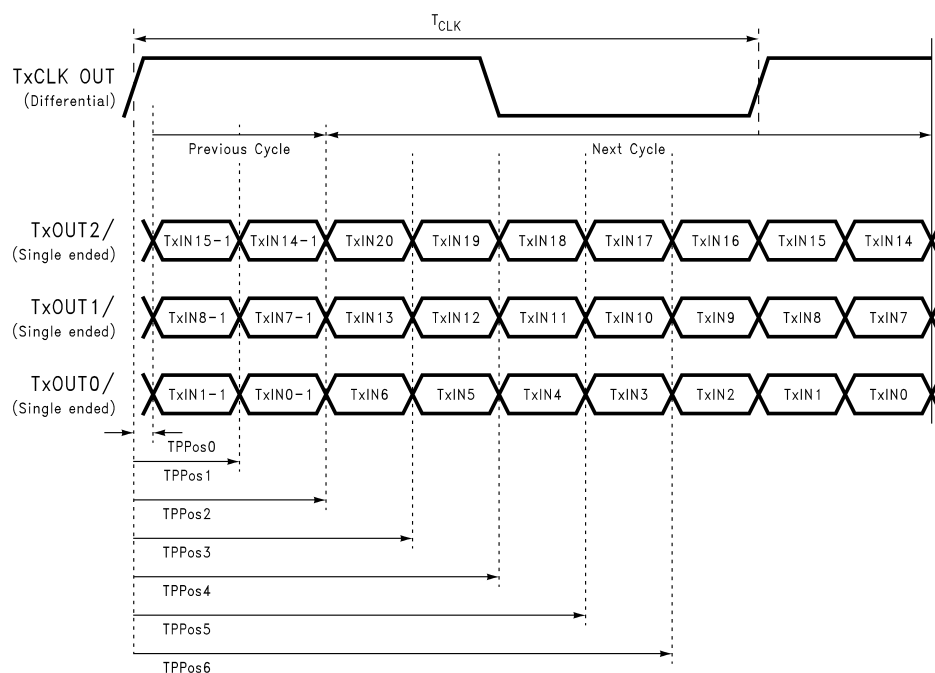


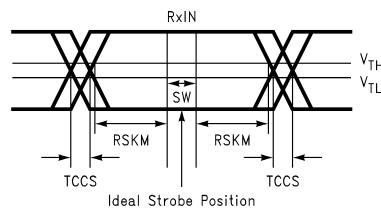
FIGURE 12. DS90CR564 (Receiver) Phase Lock Loop Set Time

## AC Timing Diagrams (Continued)



DS012617-16

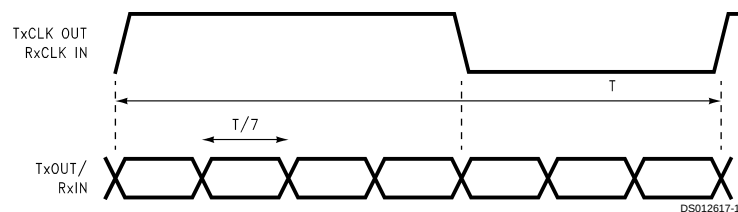
FIGURE 13. Transmitter LVDS Output Pulse Position Measurement



DS012617-17

SW — Setup and Hold Time (Internal Data Sampling Window)  
TCCS — Transmitter Output Skew  
 $RSKM \geq \text{Cable Skew (type, length)} + \text{Source Clock Jitter (cycle to cycle)}$   
Cable Skew — typically 10 ps–40 ps per foot

FIGURE 14. Receiver LVDS Input Skew Margin



DS012617-18

FIGURE 15. Seven Bits of LVDS in One Clock Cycle

## AC Timing Diagrams (Continued)

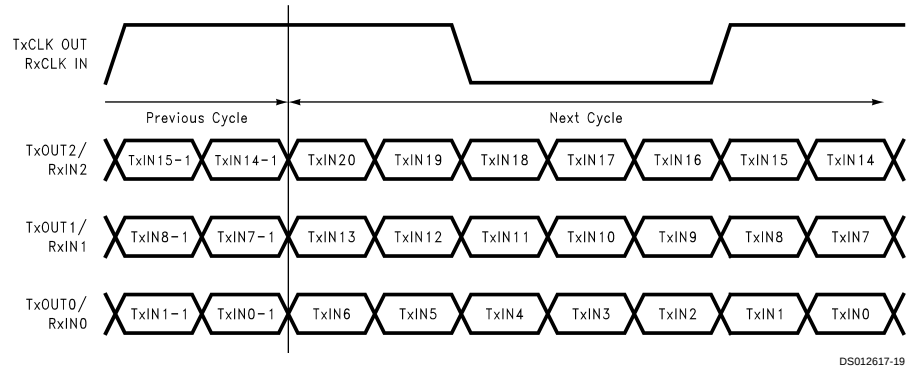


FIGURE 16. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR563)

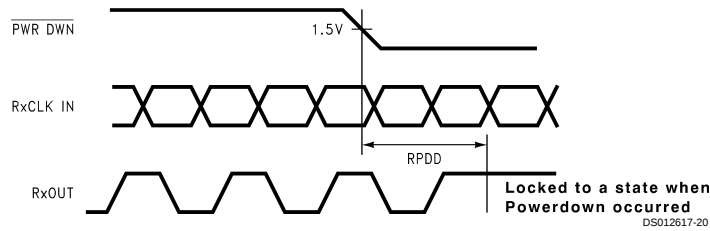


FIGURE 17. Receiver Powerdown Delay

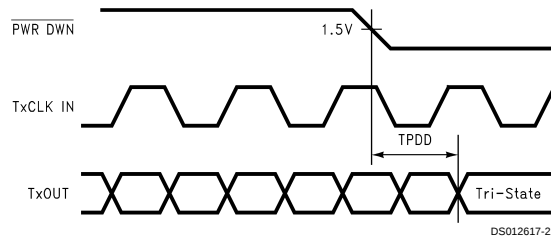


FIGURE 18. Transmitter Powerdown Delay

## DS90CR563 Pin Descriptions—FPD Link Transmitter

| Pin Name            | I/O | No. | Description                                                                                                                                      |
|---------------------|-----|-----|--------------------------------------------------------------------------------------------------------------------------------------------------|
| TxIN                | I   | 21  | TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines— FPLINE, FPFAME, DRDY(also referred to as HSYNC, VSYNC, Data Enable) |
| TxOUT+              | O   | 3   | Positive LVDS differential data output                                                                                                           |
| TxOUT-              | O   | 3   | Negative LVDS differential data output                                                                                                           |
| FPSHIFT IN          | I   | 1   | TTL level clock input. The falling edge acts as data strobe                                                                                      |
| TxCLK OUT+          | O   | 1   | Positive LVDS differential clock output                                                                                                          |
| TxCLK OUT-          | O   | 1   | Negative LVDS differential clock output                                                                                                          |
| PWR DOWN            | I   | 1   | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down                                                |
| V <sub>CC</sub>     | I   | 4   | Power supply pins for TTL inputs                                                                                                                 |
| GND                 | I   | 5   | Ground pins for TTL inputs                                                                                                                       |
| PLL V <sub>CC</sub> | I   | 1   | Power supply pin for PLL                                                                                                                         |

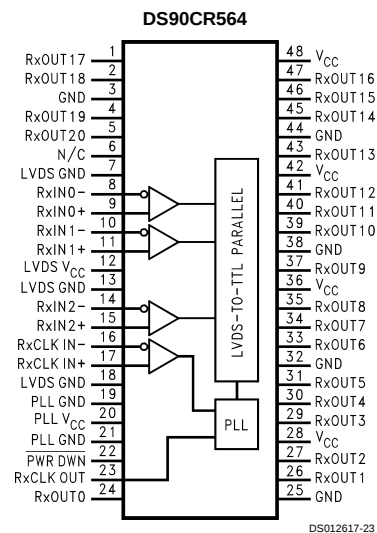
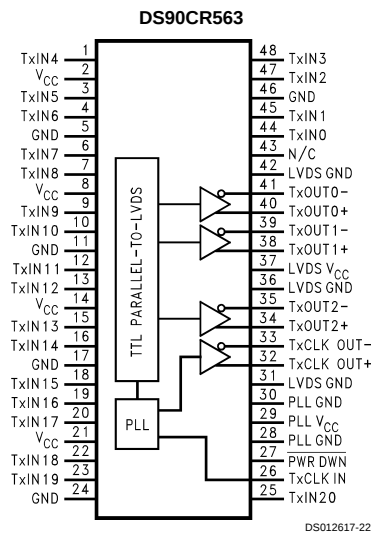
## DS90CR563 Pin Descriptions—FPD Link Transmitter (Continued)

| Pin Name             | I/O | No. | Description                       |
|----------------------|-----|-----|-----------------------------------|
| PLL GND              | I   | 2   | Ground pins for PLL               |
| LVDS V <sub>CC</sub> | I   | 1   | Power supply pin for LVDS outputs |
| LVDS GND             | I   | 3   | Ground pins for LVDS outputs      |

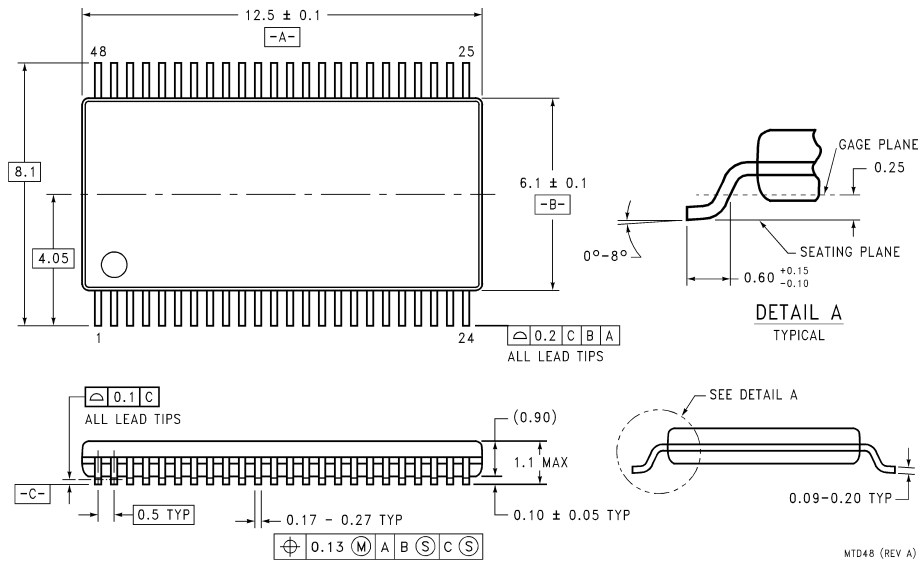
## DS90CR564 Pin Descriptions—FPD Link Receiver

| Pin Name             | I/O | No. | Description                                                                                                                                              |
|----------------------|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| RxIN+                | I   | 3   | Positive LVDS differential data inputs                                                                                                                   |
| RxIN-                | I   | 3   | Negative LVDS differential data inputs                                                                                                                   |
| RxOUT                | O   | 21  | TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable) |
| RxCLK IN+            | I   | 1   | Positive LVDS differential clock input                                                                                                                   |
| RxCLK IN-            | I   | 1   | Negative LVDS differential clock input                                                                                                                   |
| FPSHIFT OUT          | O   | 1   | TTL level clock output. The falling edge acts as data strobe                                                                                             |
| PWR DOWN             | I   | 1   | TTL level input. Assertion (low input) maintains the receiver outputs in the previous state                                                              |
| V <sub>CC</sub>      | I   | 4   | Power supply pins for TTL outputs                                                                                                                        |
| GND                  | I   | 5   | Ground pins for TTL outputs                                                                                                                              |
| PLL V <sub>CC</sub>  | I   | 1   | Power supply for PLL                                                                                                                                     |
| PLL GND              | I   | 2   | Ground pin for PLL                                                                                                                                       |
| LVDS V <sub>CC</sub> | I   | 1   | Power supply pin for LVDS inputs                                                                                                                         |
| LVDS GND             | I   | 3   | Ground pins for LVDS inputs                                                                                                                              |

## Connection Diagrams



## Physical Dimensions inches (millimeters) unless otherwise noted



### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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