

SSTUP32866

1.8 V 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer with parity and programmable output for DDR2-800 RDIMMs

Rev. 02 — 14 September 2006

Product data sheet

1. General description

The SSTUP32866 is a 1.8 V configurable register specifically designed for use on DDR2 memory modules requiring a parity checking function. It is defined in accordance with the JEDEC standard for the SSTUA32866 and SSTUB32866 registered buffers. The register is configurable (using configuration pins C0 and C1) to two topologies: 25-bit 1 : 1 or 14-bit 1 : 2, and in the latter configuration can be designated as Register A or Register B on the DIMM. It offers added features over the JEDEC standard register in that it can be configured for high or normal output drive strength, as well as for operation to 667 MT/s or 800 MT/s, simply by tying two input pins HIGH or LOW as needed.

The SSTUP32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{QERR}$ pin (active LOW). The convention is even parity, that is, valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

The SSTUP32866 is packaged in a 96-ball, 6×16 grid, 0.8 mm ball pitch LFBGA package (13.5 mm $\times$ 5.5 mm).

2. Features

- Configurable register supporting DDR2 up to 667 MT/s or 800 MT/s Registered DIMM applications
- Configurable to 25-bit 1 : 1 mode or 14-bit 1 : 2 mode
- Programmable for normal or high output drive
- Controlled multi-impedance output drivers enable optimal signal integrity and speed
- Programmable for 667 MT/s or 800 MT/s speed
- Excellent propagation delay performance
- Supports up to 450 MHz clock frequency of operation
- Optimized pinout for high-density DDR2 module design
- Chip-selects minimize power consumption by gating data outputs from changing state
- Supports SSTL_18 data inputs
- Checks parity on the DIMM-independent data inputs
- Partial parity output and input allows cascading of two SSTUP32866s for correct parity error processing
- Differential clock (CK and $\overline{CK}$) inputs
- Supports LVCMOS switching levels on the control and $\overline{RESET}$ inputs
- Single 1.8 V supply operation (1.7 V to 2.0 V)

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- Available in 96-ball, 13.5 mm × 5.5 mm, 0.8 mm ball pitch LFBGA package

3. Applications

- 667 MT/s to 800 MT/s DDR2 registered DIMMs desiring parity checking functionality

4. Ordering information

Table 1. Ordering information

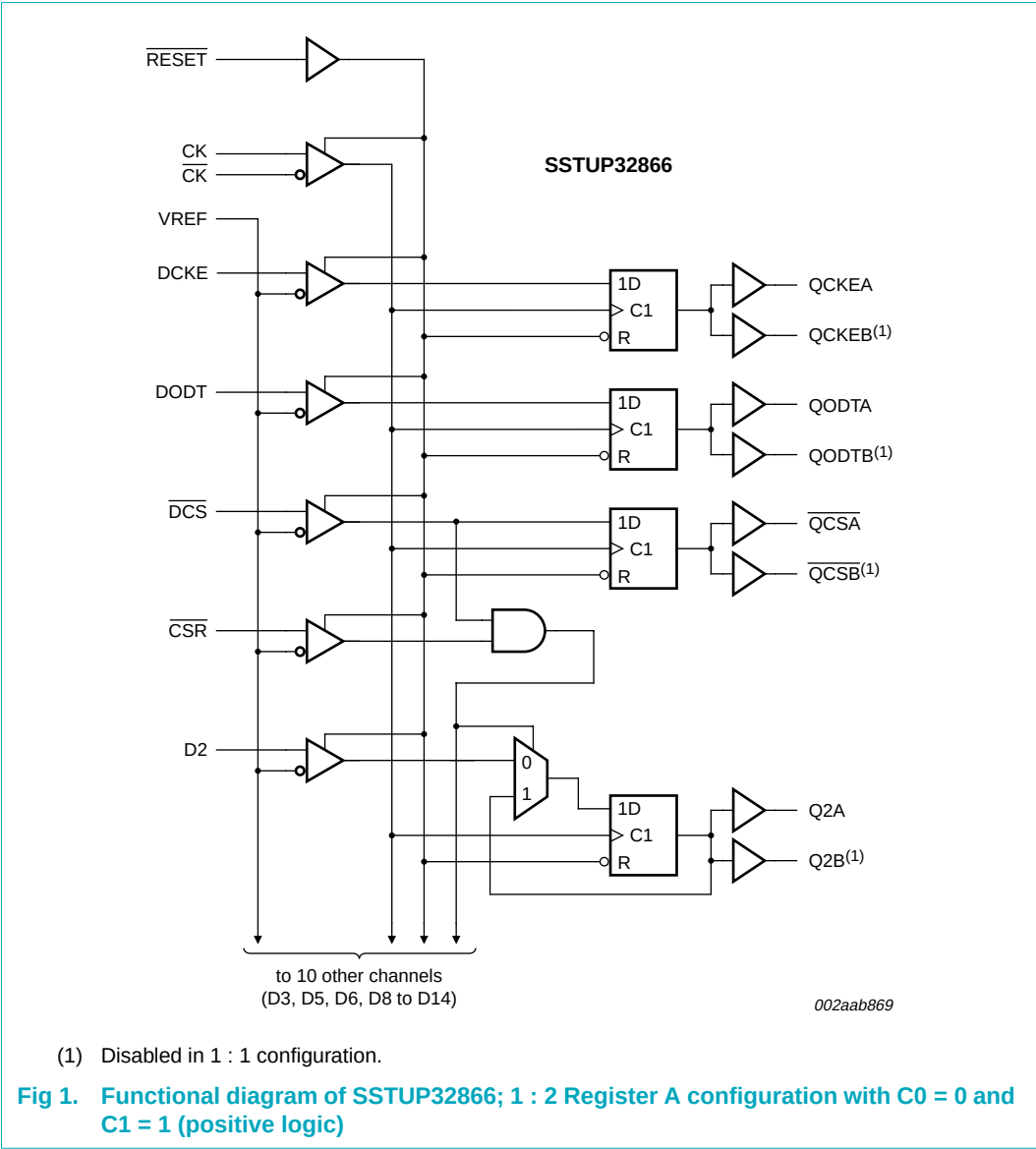
Type number	Solder process	Package		
		Name	Description	Version
SSTUP32866EC/G	Pb-free (SnAgCu solder ball compound)	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1
SSTUP32866EC/S	Pb-free (SnAgCu solder ball compound)	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4.1 Ordering options

Table 2. Ordering options

Type number	Temperature range
SSTUP32866EC/G	T _{amb} = 0 °C to +70 °C
SSTUP32866EC/S	T _{amb} = 0 °C to +85 °C

5. Functional diagram



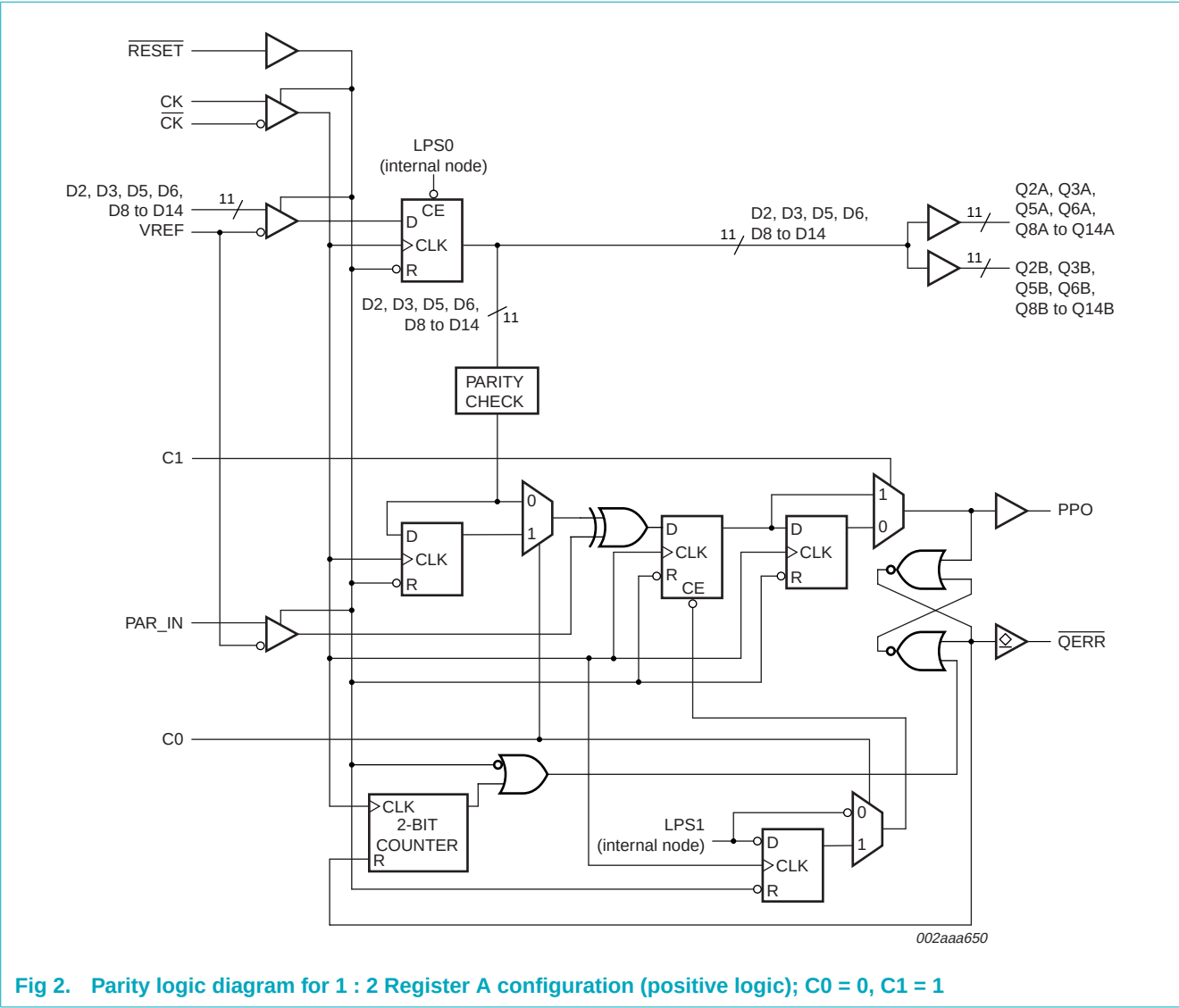


Fig 2. Parity logic diagram for 1 : 2 Register A configuration (positive logic); C0 = 0, C1 = 1

SSTUP32866EC/G
SSTUP32866EC/S

ball A1
index area

1 2 3 4 5 6

A
B
C
D
E
F
G
H
J
K
L
M
N
P
R
T

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Transparent top view

	1	2	3	4	5	6
A	○	○	○	○	○	○
B	○	○	○	○	○	○
C	○	○	○	○	○	○
D	○	○	○	○	○	○
E	○	○	○	○	○	○
F	○	○	○	○	○	○
G	○	○	○	○	○	○
H	○	○	○	○	○	○
J	○	○	○	○	○	○
K	○	○	○	○	○	○
L	○	○	○	○	○	○
M	○	○	○	○	○	○
N	○	○	○	○	○	○
P	○	○	○	○	○	○
R	○	○	○	○	○	○
T	○	○	○	○	○	○

Fig 3. Pin configuration for LFBGA96

	1	2	3	4	5	6
A	DCKE	PPO	VREF	V _{DD}	QCKE	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	V _{DD}	V _{DD}	Q3	Q16
D	D0DT	$\overline{\text{QERR}}$	GND	GND	Q0DT	DNU
E	D5	D17	V _{DD}	V _{DD}	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{\text{RESET}}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{\text{DCS}}$	GND	GND	$\overline{\text{QCS}}$	DNU
J	$\overline{\text{CK}}$	$\overline{\text{CSR}}$	V _{DD}	V _{DD}	SELAB	SELDR
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	V _{DD}	V _{DD}	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	V _{DD}	V _{DD}	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	V _{DD}	V _{DD}	Q13	Q24
T	D14	D25	VREF	V _{DD}	Q14	Q25

Fig 4. Ball mapping, 1 : 1 register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	DCKE	PPO	VREF	V _{DD}	QCKEA	QCKEB
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	DODT	$\overline{QERR}$	GND	GND	QODTA	QODTB
E	D5	n.c.	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	n.c.	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V _{DD}	V _{DD}	SELAB	SELDLDR
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V _{DD}	V _{DD}	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	D14	DNU	VREF	V _{DD}	Q14A	Q14B

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Fig 5. Ball mapping, 1 : 2 Register A (C0 = 0, C1 = 1)

	1	2	3	4	5	6
A	D1	PPO	VREF	V _{DD}	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V _{DD}	V _{DD}	Q3A	Q3B
D	D4	$\overline{QERR}$	GND	GND	Q4A	Q4B
E	D5	DNU	V _{DD}	V _{DD}	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RESET}$	V _{DD}	V _{DD}	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	V _{DD}	V _{DD}	SELAB	SELDLDR
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V _{DD}	V _{DD}	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	DODT	DNU	V _{DD}	V _{DD}	QODTA	QODTB
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V _{DD}	V _{DD}	Q13A	Q13B
T	DCKE	DNU	VREF	V _{DD}	QCKEA	QCKEB

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Fig 6. Ball mapping, 1 : 2 Register B (C0 = 1, C1 = 1)

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
GND	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	ground input	ground
V _{DD}	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	1.8 V nominal	power supply voltage
VREF	A3, T3	0.9 V nominal	input reference voltage
CK	H1	differential input	positive master clock input
$\overline{\text{CK}}$	J1	differential input	negative master clock input
C0	G6	LVC MOS inputs	Configuration control inputs; Register A or Register B and 1 : 1 mode or 1 : 2 mode select.
C1	G5		
SELD _R	J6	LVC MOS input	Selects output drive strength: HIGH for normal drive, LOW for high drive. This pin will default HIGH if left open-circuit (built-in weak pull-up resistor).
SELAB	J5	LVC MOS input	Selects speed grade: HIGH for DDR2-667, LOW for DDR2-800. This pin will default HIGH if left open-circuit (built-in weak pull-up resistor).
$\overline{\text{RESET}}$	G2	LVC MOS input	Asynchronous reset input (active LOW). Resets registers and disables VREF data and clock.
CSR	J2	SSTL ₁₈ input	Chip select inputs (active LOW). Disables D1 to D25 ^[1] outputs switching when both inputs are HIGH.
$\overline{\text{DCS}}$	H2		
D1 to D25	^[2]	SSTL ₁₈ input	Data input. Clocked in on the crossing of the rising edge of CK and the falling edge of CK.
DODT	^[2]	SSTL ₁₈ input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
DCKE	^[2]	SSTL ₁₈ input	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
PAR _{IN}	G1	SSTL ₁₈ input	Parity input. Arrives one clock cycle after the corresponding data input.
Q1 to Q25, Q2A to Q14A, Q1B to Q14B	^[2]	1.8 V CMOS outputs	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control ^[3] .
PPO	A2	1.8 V CMOS output	Partial parity out. Indicates odd parity of inputs D1 to D25 ^[1] .
$\overline{\text{QCS}}$, $\overline{\text{QCSA}}$, $\overline{\text{QCSB}}$	^[2]	1.8 V CMOS output	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.
QODT, QODTA, QODTB	^[2]	1.8 V CMOS output	Data output that will not be suspended by the DCS and CSR control.

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
QCKE, QCKEA, QCKEB	[2]	1.8 V CMOS output	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control.
$\overline{QERR}$	D2	open-drain output	Output error bit (active LOW). Generated one clock cycle after the corresponding data output
DNU	[2]	-	Do not use. Inputs are in standby-equivalent mode and outputs are driven LOW.

- [1] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.
 Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.
 Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.
- [2] Depends on configuration. See [Figure 4](#), [Figure 5](#), and [Figure 6](#) for ball number.
- [3] Data outputs = Q2, Q3, Q5, Q6, Q8 to Q25 when C0 = 0 and C1 = 0.
 Data outputs = Q2, Q3, Q5, Q6, Q8 to Q14 when C0 = 0 and C1 = 1.
 Data outputs = Q1 to Q6, Q8 to Q10, Q12, Q13 when C0 = 1 and C1 = 1.

7. Functional description

The SSTUP32866 is a 25-bit 1 : 1 or 14-bit 1 : 2 configurable registered buffer with parity, designed for 1.7 V to 2.0 V V_{DD} operation. Additionally, the SSTUP32866 can be programmed to deliver either normal or high output drive, and either 600 MT/s or 800 MT/s speeds.

Two programming pins, SELAB and SELDR, allow the user to respectively select speed and drive strength options by tying these pins either LOW or HIGH on the DIMM. The truth table for these options is shown in [Table 6](#).

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control and reset ($\overline{RESET}$) inputs are LVCMOS. All data outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load, and meet SSTL_18 specifications. The error ($\overline{QERR}$) output is 1.8 V open-drain driver.

The SSTUP32866 operates from a differential clock (CK and $\overline{CK}$). Data are registered at the crossing of CK going HIGH, and CK going LOW.

The C0 input controls the pinout configuration for the 1 : 2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1 : 1 (when LOW) to 14-bit 1 : 2 (when HIGH).

The SSTUP32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain $\overline{QERR}$ pin (active LOW). The convention is even parity, that is, valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

When used as a single device, the C0 and C1 inputs are tied LOW. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. The Partial-Parity-Out (PPO) and $\overline{QERR}$ signals are produced three cycles after the corresponding data inputs.

When used in pairs, the C0 input of the first register is tied LOW and the C0 input of the second register is tied HIGH. The C1 input of both registers are tied HIGH. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. The PPO and $\overline{QERR}$ signals are produced on the second device three clock cycles after the corresponding data inputs. The PPO output of the first register is cascaded to the PAR_IN of the second register. The $\overline{QERR}$ output of the first register is left floating and the valid error information is latched on the $\overline{QERR}$ output of the second register.

If an error occurs and the $\overline{QERR}$ output is driven LOW, it stays latched LOW for two clock cycles or until $\overline{RESET}$ is driven LOW. The DIMM-dependent signals (DCKE, $\overline{DCS}$, DODT, and $\overline{CSR}$) are not included in the parity check computation.

The device supports low-power standby operation. When $\overline{RESET}$ is LOW, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when $\overline{RESET}$ is LOW all registers are reset, and all outputs are forced LOW. The LVCMOS $\overline{RESET}$ input must always be held at a valid logic HIGH or LOW level.

The device also supports low-power active operation by monitoring both system chip select ($\overline{DCS}$ and $\overline{CSR}$) inputs and will gate the Qn and PPO outputs from changing states when both $\overline{DCS}$ and $\overline{CSR}$ inputs are HIGH. If either $\overline{DCS}$ or $\overline{CSR}$ input is LOW, the Qn and PPO outputs will function normally. The $\overline{RESET}$ input has priority over the $\overline{DCS}$ and $\overline{CSR}$ control and when driven LOW will force the Qn and PPO outputs LOW, and the $\overline{QERR}$ output HIGH. If the $\overline{DCS}$ control functionality is not desired, then the $\overline{CSR}$ input can be hard-wired to ground, in which case, the setup time requirement for $\overline{DCS}$ would be the same as for the other Dn data inputs. To control the low-power mode with $\overline{DCS}$ only, then the $\overline{CSR}$ input should be pulled up to V_{DD} through a pull-up resistor.

To ensure defined outputs from the register before a stable clock has been supplied, $\overline{RESET}$ must be held in the LOW state during power-up.

In the DDR2 RDIMM application, $\overline{RESET}$ is specified to be completely asynchronous with respect to CK and $\overline{CK}$. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the Qn outputs will be driven LOW quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are LOW, and the clock is stable during the time from the LOW-to-HIGH transition of $\overline{RESET}$ until the input receivers are fully enabled, the design of the SSTUP32866 must ensure that the outputs will remain LOW, thus ensuring no glitches on the output.

7.1 Function table

Table 4. Function table (each flip-flop)

L = LOW voltage level; H = HIGH voltage level; X = don't care; $\uparrow$ = LOW-to-HIGH transition; $\downarrow$ = HIGH-to-LOW transition.

Inputs						Outputs ^[1]		
RESET	DCS	CSR	CK	$\overline{CK}$	Dn, DODTn, DCKEn	Qn	$\overline{QCS}$	QODT, QCKE
H	L	L	$\uparrow$	$\downarrow$	L	L	L	L
H	L	L	$\uparrow$	$\downarrow$	H	H	L	H
H	L	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	L	H	$\uparrow$	$\downarrow$	L	L	L	L
H	L	H	$\uparrow$	$\downarrow$	H	H	L	H
H	L	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	L	$\uparrow$	$\downarrow$	L	L	H	L
H	H	L	$\uparrow$	$\downarrow$	H	H	H	H
H	H	L	L or H	L or H	X	Q ₀	Q ₀	Q ₀
H	H	H	$\uparrow$	$\downarrow$	L	Q ₀	H	L
H	H	H	$\uparrow$	$\downarrow$	H	Q ₀	H	H
H	H	H	L or H	L or H	X	Q ₀	Q ₀	Q ₀
L	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

[1] Q₀ is the previous state of the associated output.

Table 5. Parity and standby function table

L = LOW voltage level; H = HIGH voltage level; X = don't care; $\uparrow$ = LOW-to-HIGH transition; $\downarrow$ = HIGH-to-LOW transition.

Inputs							Outputs ^[1]	
RESET	DCS	CSR	CK	$\overline{CK}$	Σ of inputs = H (D1 to D25)	PAR_IN ^[2]	PPO ^[3]	$\overline{QERR}$ ^[4]
H	L	X	$\uparrow$	$\downarrow$	even	L	L	H
H	L	X	$\uparrow$	$\downarrow$	odd	L	H	L
H	L	X	$\uparrow$	$\downarrow$	even	H	H	L
H	L	X	$\uparrow$	$\downarrow$	odd	H	L	H
H	H	L	$\uparrow$	$\downarrow$	even	L	L	H
H	H	L	$\uparrow$	$\downarrow$	odd	L	H	L
H	H	L	$\uparrow$	$\downarrow$	even	H	H	L
H	H	L	$\uparrow$	$\downarrow$	odd	H	L	H
H	H	H	$\uparrow$	$\downarrow$	X	X	PPO ₀	$\overline{QERR}_0$
H	X	X	L or H	L or H	X	X	PPO ₀	$\overline{QERR}_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	H

[1] PPO₀ is the previous state of output PPO; $\overline{QERR}_0$ is the previous state of output $\overline{QERR}$.

[2] Data inputs = D2, D3, D5, D6, D8 to D25 when C0 = 0 and C1 = 0.

Data inputs = D2, D3, D5, D6, D8 to D14 when C0 = 0 and C1 = 1.

Data inputs = D1 to D6, D8 to D10, D12, D13 when C0 = 1 and C1 = 1.

[3] PAR_IN arrives one clock cycle (C0 = 0), or two clock cycles (C0 = 1), after the data to which it applies.

[4] This condition assumes $\overline{QERR}$ is HIGH at the crossing of CK going HIGH and $\overline{CK}$ going LOW. If $\overline{QERR}$ is LOW, it stays latched LOW for two clock cycles or until RESET is driven LOW.

Table 6. Speed and drive programmability

Inputs		Mode
SELDL	SELAL	
L	L	DDR2-800; high output drive
L	H	DDR2-667; high output drive
H	L	DDR2-800; normal output drive
H	H	DDR2-667; normal output drive

8. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+2.5	V
V_I	input voltage	receiver	-0.5 ^[1]	+2.5 ^[2]	V
V_O	output voltage	driver	-0.5 ^[1]	$V_{DD} + 0.5$ ^[2]	V
I_{IK}	input clamping current	$V_I < 0\text{ V}$ or $V_I > V_{DD}$	-	-50	mA
I_{OK}	output clamping current	$V_O < 0\text{ V}$ or $V_O > V_{DD}$	-	±50	mA
I_O	output current	continuous; $0\text{ V} < V_O < V_{DD}$	-	±50	mA
I_{CCC}	continuous current through each V_{DD} or GND pin		-	±100	mA
T_{stg}	storage temperature		-65	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); 1.5 kΩ; 100 pF	2	-	kV
		Machine Model (MM); 0 Ω; 200 pF	200	-	V

[1] The input and output negative voltage ratings may be exceeded if the input and output clamping current ratings are observed.

[2] This value is limited to 2.5 V maximum.

9. Recommended operating conditions

Table 8. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		1.7	-	2.0	V
V_{ref}	reference voltage		$0.49 \times V_{DD}$	$0.50 \times V_{DD}$	$0.51 \times V_{DD}$	V
V_T	termination voltage		$V_{ref} - 0.040$	V_{ref}	$V_{ref} + 0.040$	V
V_I	input voltage		0	-	V_{DD}	V
$V_{IH(AC)}$	AC HIGH-level input voltage	data (Dn), $\overline{CSR}$, and PAR_IN inputs	$V_{ref} + 0.250$	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage	data (Dn), $\overline{CSR}$, and PAR_IN inputs	-	-	$V_{ref} - 0.250$	V
$V_{IH(DC)}$	DC HIGH-level input voltage	data (Dn), $\overline{CSR}$, and PAR_IN inputs	$V_{ref} + 0.125$	-	-	V
$V_{IL(DC)}$	DC LOW-level input voltage	data (Dn), $\overline{CSR}$, and PAR_IN inputs	-	-	$V_{ref} - 0.125$	V
V_{IH}	HIGH-level input voltage	$\overline{RESET}$, Cn, SELAB, SELDR	[1] $0.65 \times V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage	$\overline{RESET}$, Cn, SELAB, SELDR	[1] -	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	CK, $\overline{CK}$	[2] 0.675	-	1.125	V
V_{ID}	differential input voltage	CK, $\overline{CK}$	[2] 600	-	-	mV
I_{OH}	HIGH-level output current	SELDR either HIGH or LOW	-	-	-8	mA
I_{OL}	LOW-level output current	SELDR either HIGH or LOW	-	-	8	mA
T_{amb}	ambient temperature	operating in free air				
		SSTUP32866EC/G	0	-	70	°C
		SSTUP32866EC/S	0	-	85	°C

[1] The $\overline{RESET}$ and Cn inputs of the device must be held at valid levels (not floating) to ensure proper device operation.

[2] The differential inputs must not be floating, unless $\overline{RESET}$ is LOW.

10. Characteristics

Table 9. Characteristics

At recommended operating conditions (see Table 8); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$I_{OH} = -6 \text{ mA}$; $V_{DD} = 1.7 \text{ V}$	1.2	-	-	V
V_{OL}	LOW-level output voltage	$I_{OL} = 6 \text{ mA}$; $V_{DD} = 1.7 \text{ V}$	-	-	0.5	V
I_I	input current	all inputs; $V_I = V_{DD}$ or GND; $V_{DD} = 2.0 \text{ V}$	-	-	± 5	μA
I_{DD}	supply current	static Standby mode; $\overline{\text{RESET}} = \text{GND}$; $I_O = 0 \text{ mA}$; $V_{DD} = 2.0 \text{ V}$	-	-	100	μA
		static Operating mode; $\text{RESET} = V_{DD}$; $I_O = 0 \text{ mA}$; $V_{DD} = 2.0 \text{ V}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$	-	-	40	mA
I_{DDO}	dynamic operating current per MHz	clock only; $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle; $I_O = 0 \text{ mA}$; $V_{DD} = 1.8 \text{ V}$	-	16	-	μA
		per each data input, 1 : 1 mode; $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle; $I_O = 0 \text{ mA}$; $V_{DD} = 1.8 \text{ V}$	-	11	-	μA
		per each data input, 1 : 2 mode; $\overline{\text{RESET}} = V_{DD}$; $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$; CK and $\overline{\text{CK}}$ switching at 50 % duty cycle; one data input switching at half clock frequency, 50 % duty cycle; $I_O = 0 \text{ mA}$; $V_{DD} = 1.8 \text{ V}$	-	19	-	μA
C_i	input capacitance	data and $\overline{\text{CSR}}$ inputs; $V_I = V_{\text{ref}} \pm 250 \text{ mV}$; $V_{DD} = 1.8 \text{ V}$	2.5	-	3.5	pF
		CK and $\overline{\text{CK}}$ inputs; $V_{ICR} = 0.9 \text{ V}$; $V_{i(p-p)} = 600 \text{ mV}$; $V_{DD} = 1.8 \text{ V}$	2	-	3	pF
		$\overline{\text{RESET}}$ input; $V_I = V_{DD}$ or GND; $V_{DD} = 1.8 \text{ V}$	3	-	4	pF
Z_o	output impedance	normal drive; instantaneous	[1]	-	15	Ω
		normal drive; steady-state	-	53	-	Ω
		high drive; instantaneous	[1]	-	7	Ω
		high drive; steady-state	-	53	-	Ω

[1] Instantaneous is defined as within < 2 ns following the output data transition edge.

Table 10. Timing requirementsAt recommended operating conditions (see [Table 8](#)), unless otherwise specified. See [Section 11.1](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clock}	clock frequency		-	-	450	MHz
t_W	pulse width	CK, $\overline{\text{CK}}$ HIGH or LOW	1	-	-	ns
t_{ACT}	differential inputs active time		[1][2]	-	10	ns
t_{INACT}	differential inputs inactive time		[1][3]	-	15	ns
t_{SU}	setup time	$\overline{\text{DCS}}$ before CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$, $\overline{\text{CSR}}$ HIGH; $\overline{\text{CSR}}$ before CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$, $\overline{\text{DCS}}$ HIGH	0.6	-	-	ns
		$\overline{\text{DCS}}$ before CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$, $\overline{\text{CSR}}$ LOW	0.5	-	-	ns
		DODT, DCKE and data (Dn) before CK $\uparrow$, CK $\downarrow$	0.5	-	-	ns
		PAR_IN before CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$	0.5	-	-	ns
t_{H}	hold time	DCS, DODT, DCKE and data (Dn) after CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$	0.4	-	-	ns
		PAR_IN after CK $\uparrow$, $\overline{\text{CK}}$ $\downarrow$	0.4	-	-	ns

[1] This parameter is not necessarily production tested.

[2] VREF must be held at a valid input voltage level and data inputs must be held LOW for a minimum time of $t_{\text{ACT(max)}}$ after $\overline{\text{RESET}}$ is taken HIGH.[3] VREF, data and clock inputs must be held at valid levels (not floating) a minimum time of $t_{\text{INACT(max)}}$ after $\overline{\text{RESET}}$ is taken LOW.**Table 11. Switching characteristics (667 mode, SELAB = HIGH)**At recommended operating conditions (see [Table 8](#)), unless otherwise specified. See [Section 11.1](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum input clock frequency		450	-	-	MHz
t_{PDM}	peak propagation delay	single bit switching; from CK $\uparrow$ and $\overline{\text{CK}}$ $\downarrow$ to Qn	[1]	1.2	-	1.8 ns
t_{PD}	propagation delay	from CK $\uparrow$ and $\overline{\text{CK}}$ $\downarrow$ to PPO	0.5	-	1.8	ns
t_{LH}	LOW-to-HIGH delay	from CK $\uparrow$ and $\overline{\text{CK}}$ $\downarrow$ to $\overline{\text{QERR}}$	1.2	-	3	ns
t_{HL}	HIGH-to-LOW delay	from CK $\uparrow$ and $\overline{\text{CK}}$ $\downarrow$ to $\overline{\text{QERR}}$	1	-	2.4	ns
t_{PDMSS}	simultaneous switching peak propagation delay	from CK $\uparrow$ and $\overline{\text{CK}}$ $\downarrow$ to Qn	[1][2]	-	2.0	ns
t_{PHL}	HIGH-to-LOW propagation delay	from $\overline{\text{RESET}}$ $\downarrow$ to Qn $\downarrow$	-	-	3	ns
		from $\overline{\text{RESET}}$ $\downarrow$ to PPO $\downarrow$	-	-	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from $\overline{\text{RESET}}$ $\downarrow$ to $\overline{\text{QERR}}$ $\uparrow$	-	-	3	ns

[1] Includes 350 ps of test load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 12. Switching characteristics (800 mode, SELAB = LOW)At recommended operating conditions (see [Table 8](#)), unless otherwise specified. See [Section 11.1](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\max}$	maximum input clock frequency		450	-	-	MHz
t_{PDM}	peak propagation delay	single bit switching; from CK $\uparrow$ and CK $\downarrow$ to Qn	[1] 1.1	-	1.5	ns
t_{PD}	propagation delay	from CK $\uparrow$ and CK $\downarrow$ to PPO	0.5	-	1.7	ns
t_{LH}	LOW-to-HIGH delay	from CK $\uparrow$ and CK $\downarrow$ to QERR	1.2	-	3	ns
t_{HL}	HIGH-to-LOW delay	from CK $\uparrow$ and CK $\downarrow$ to QERR	1	-	2.4	ns
t_{PDMSS}	simultaneous switching peak propagation delay	from CK $\uparrow$ and CK $\downarrow$ to Qn	[1][2] -	-	1.6	ns
t_{PHL}	HIGH-to-LOW propagation delay	from RESET $\downarrow$ to Qn $\downarrow$	-	-	3	ns
		from RESET $\downarrow$ to PPO $\downarrow$	-	-	3	ns
t_{PLH}	LOW-to-HIGH propagation delay	from RESET $\downarrow$ to QERR $\uparrow$	-	-	3	ns

[1] Includes 350 ps of test load transmission line delay.

[2] This parameter is not necessarily production tested.

Table 13. Data output edge ratesAt recommended operating conditions (see [Table 8](#)), unless otherwise specified. See [Section 11.2](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
dV/dt_r	rising edge slew rate	from 20 % to 80 %	1	-	4	V/ns
dV/dt_f	falling edge slew rate	from 80 % to 20 %	1	-	4	V/ns
dV/dt_{Δ}	absolute difference between dV/dt_r and dV/dt_f	from 20 % or 80 % to 80 % or 20 %	-	-	1	V/ns

10.1 Timing diagrams

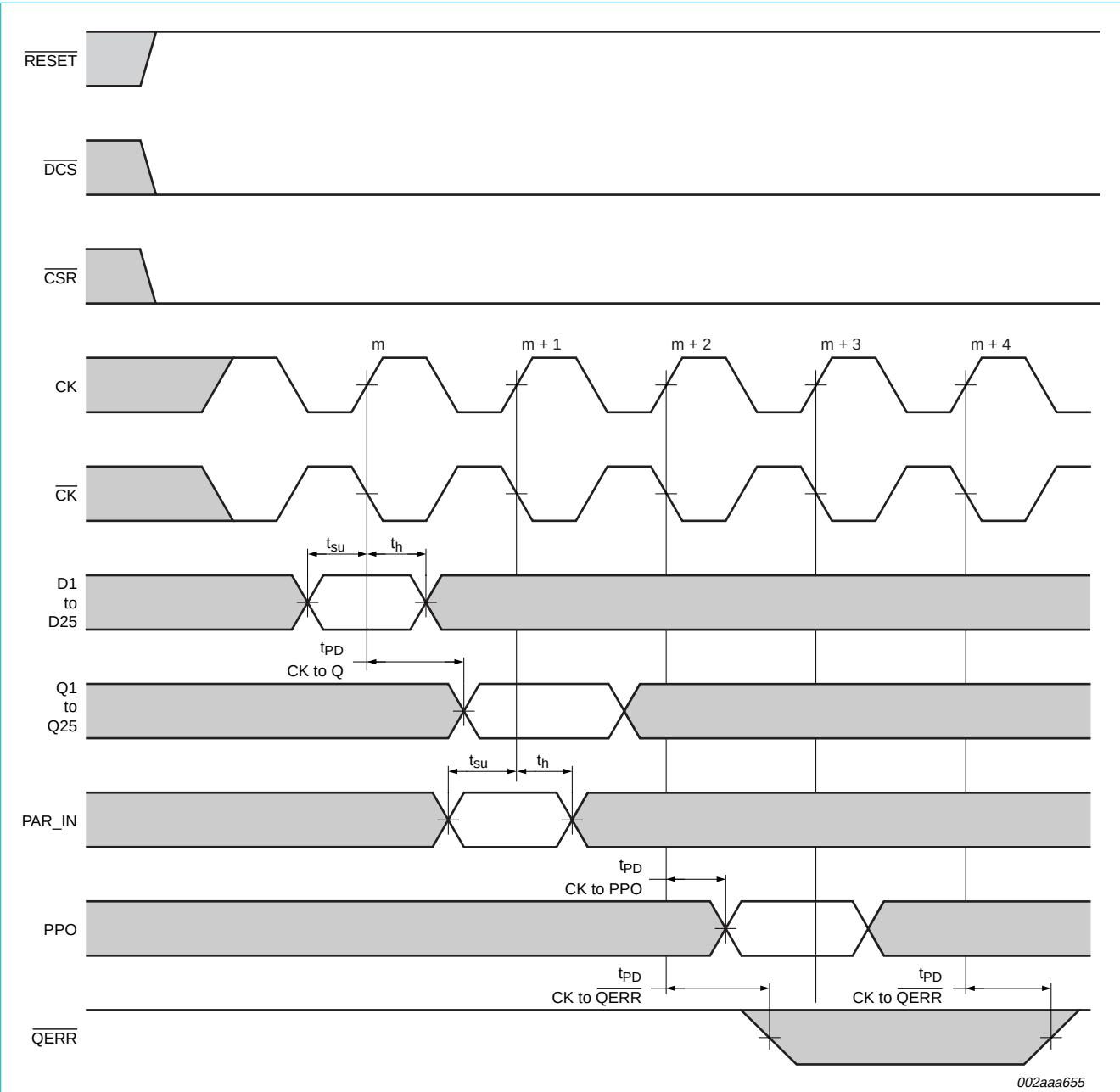
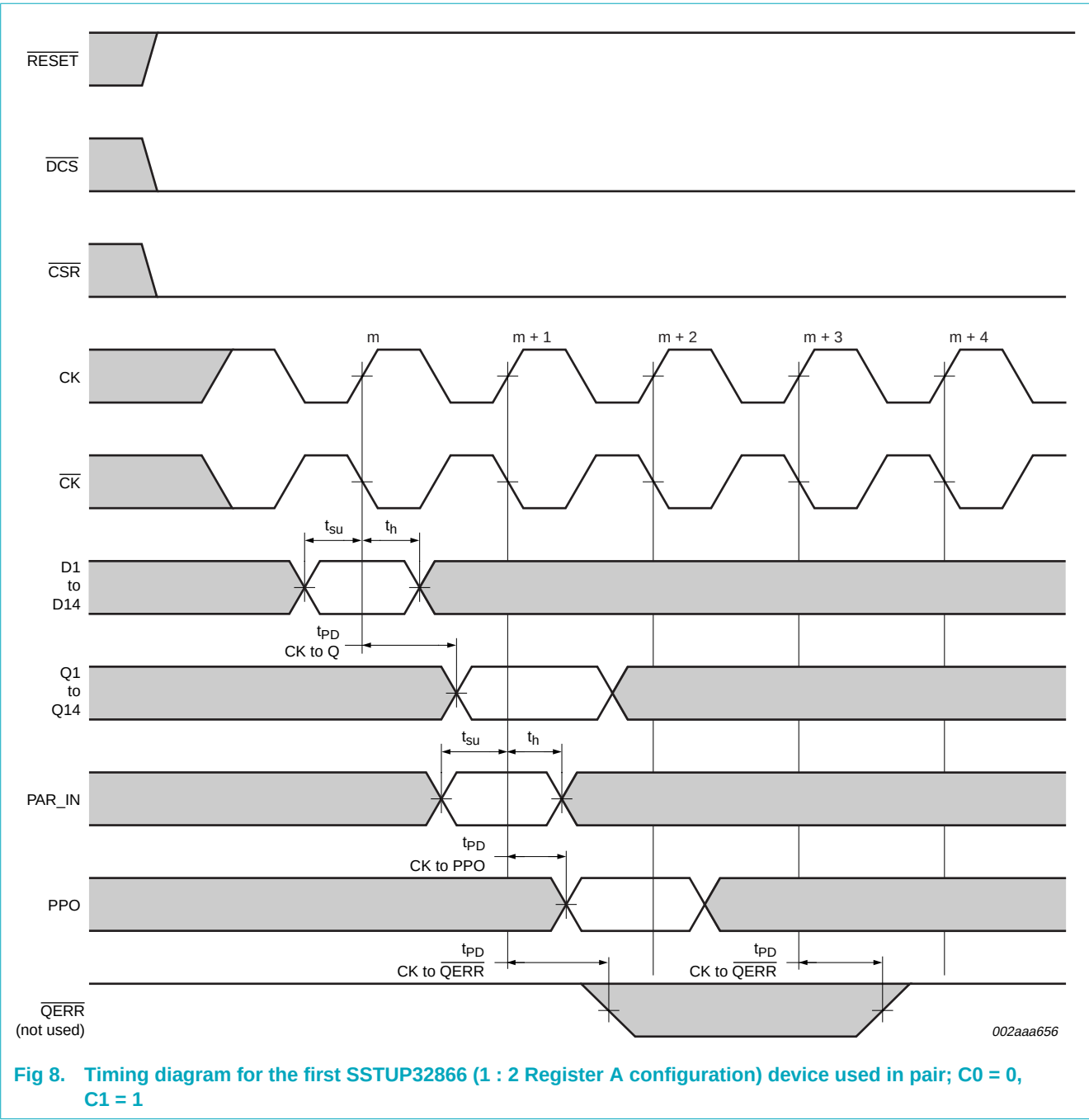
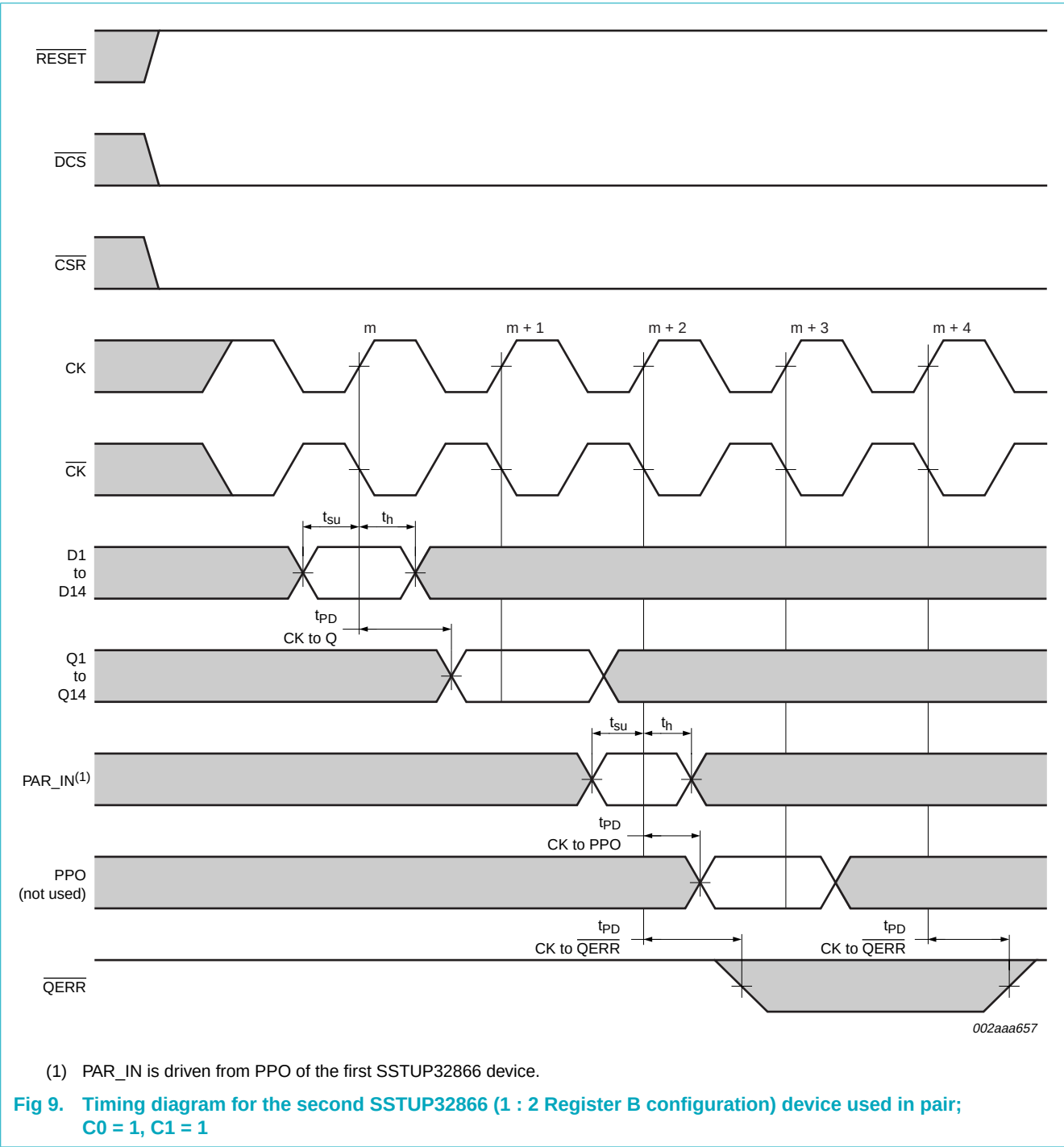


Fig 7. Timing diagram for SSTUP32866 used as a single device; C0 = 0, C1 = 0





11. Test information

11.1 Parameter measurement information for data output load circuit

$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V}$.

All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$; $Z_0 = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20 \%$, unless otherwise specified.

The outputs are measured one at a time with one transition per measurement.

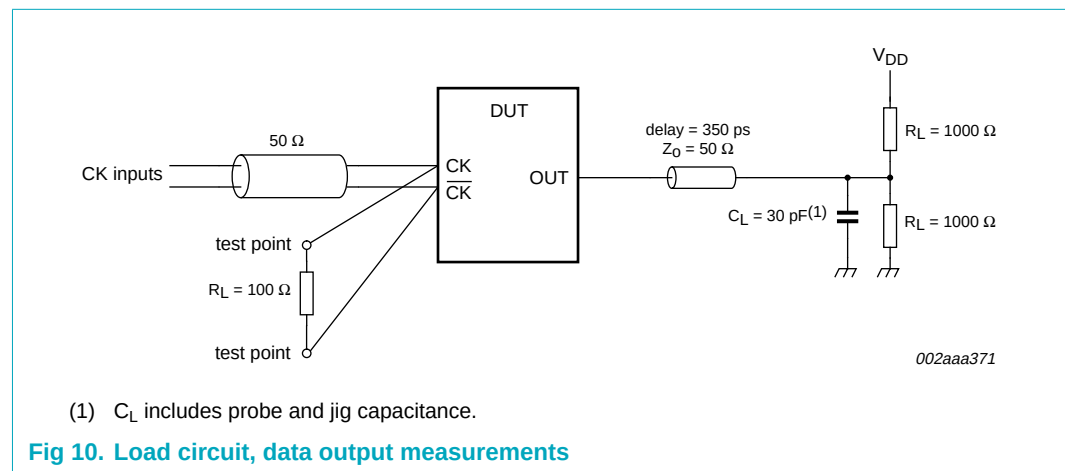


Fig 10. Load circuit, data output measurements

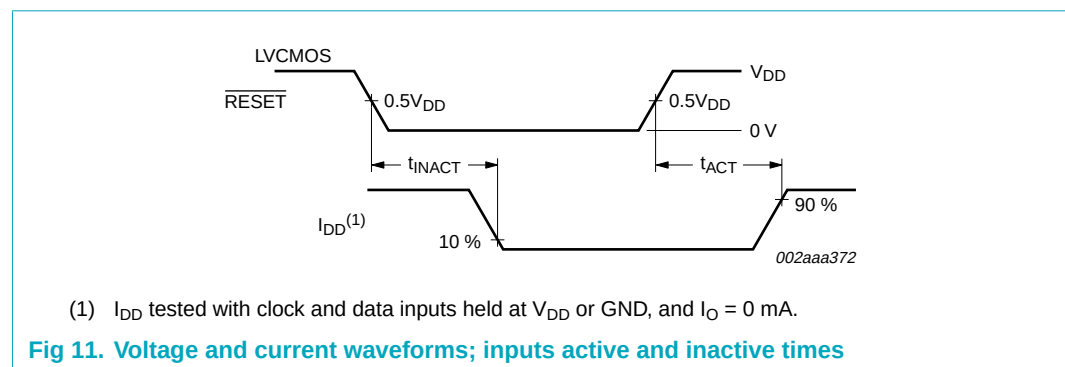


Fig 11. Voltage and current waveforms; inputs active and inactive times

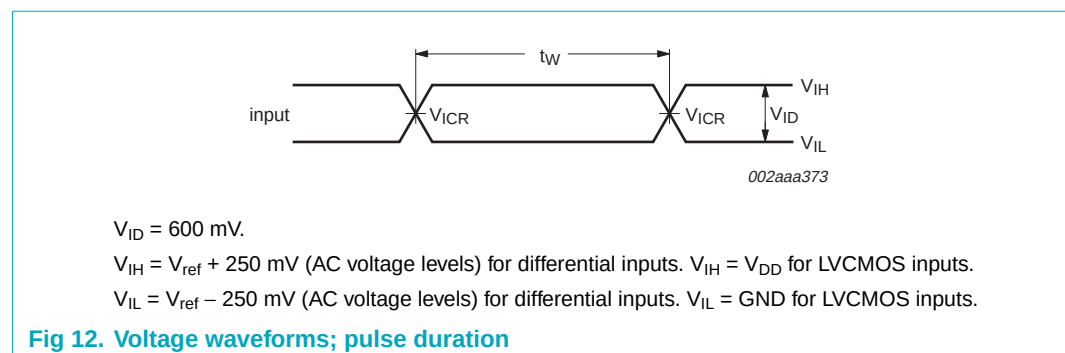
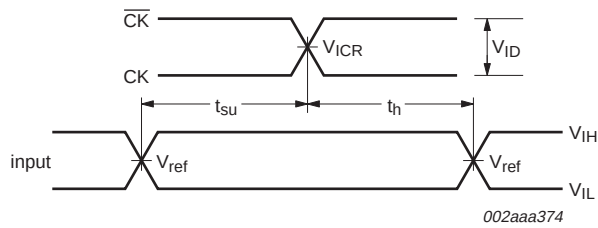


Fig 12. Voltage waveforms; pulse duration



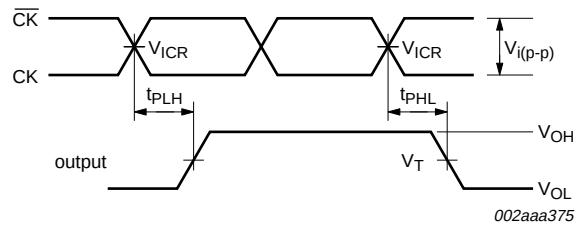
$V_{ID} = 600 \text{ mV}$.

$V_{ref} = 0.5V_{DD}$.

$V_{IH} = V_{ref} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

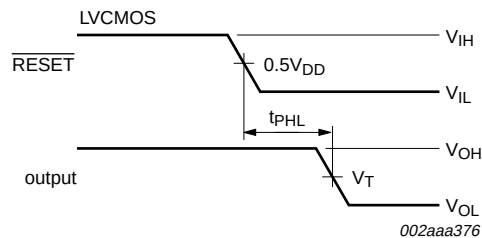
$V_{IL} = V_{ref} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS inputs.

Fig 13. Voltage waveforms; setup and hold times



t_{PLH} and t_{PHL} are the same as t_{PD} .

Fig 14. Voltage waveforms; propagation delay times (clock to output)



t_{PLH} and t_{PHL} are the same as t_{PD} .

$V_{IH} = V_{ref} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

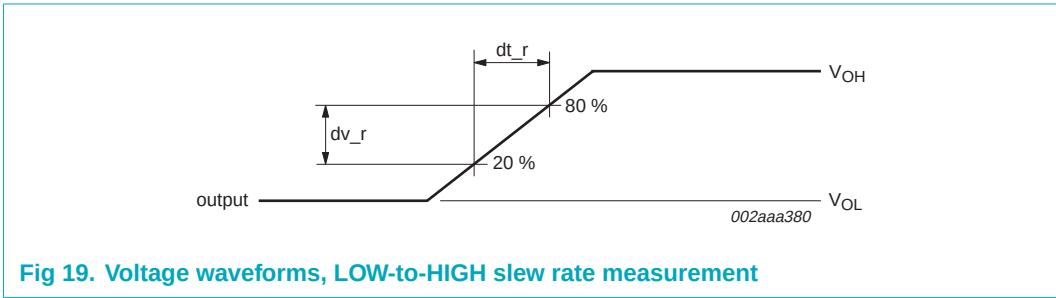
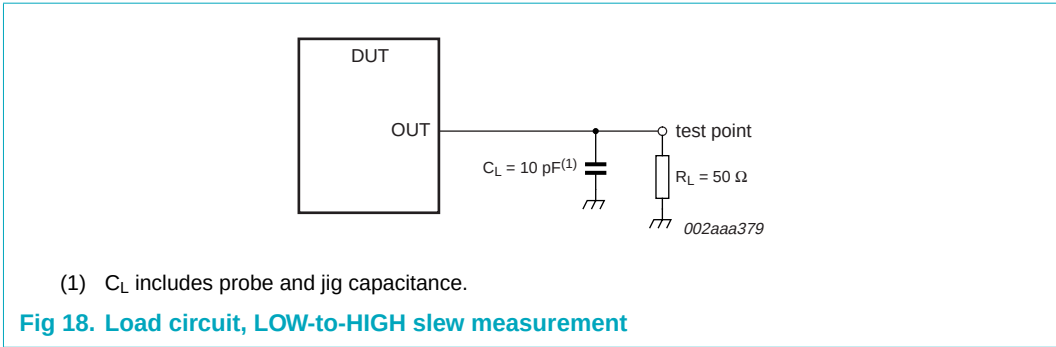
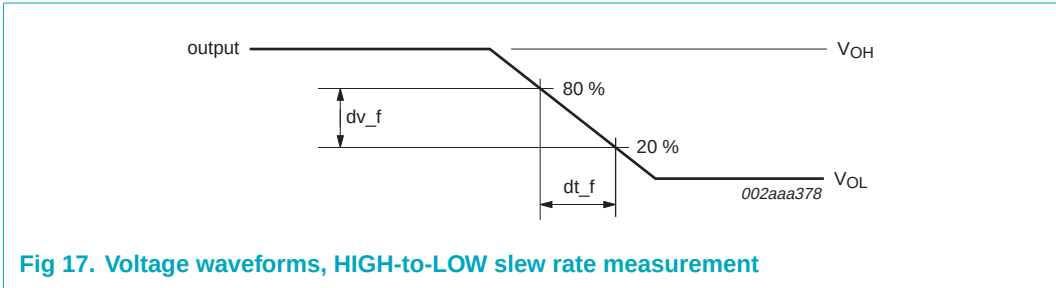
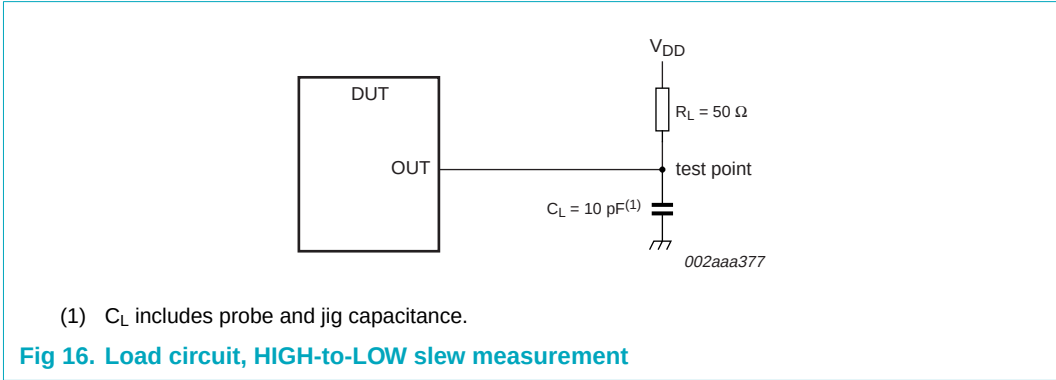
$V_{IL} = V_{ref} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS inputs.

Fig 15. Voltage waveforms; propagation delay times (reset to output)

11.2 Data output slew rate measurement information

$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}.$

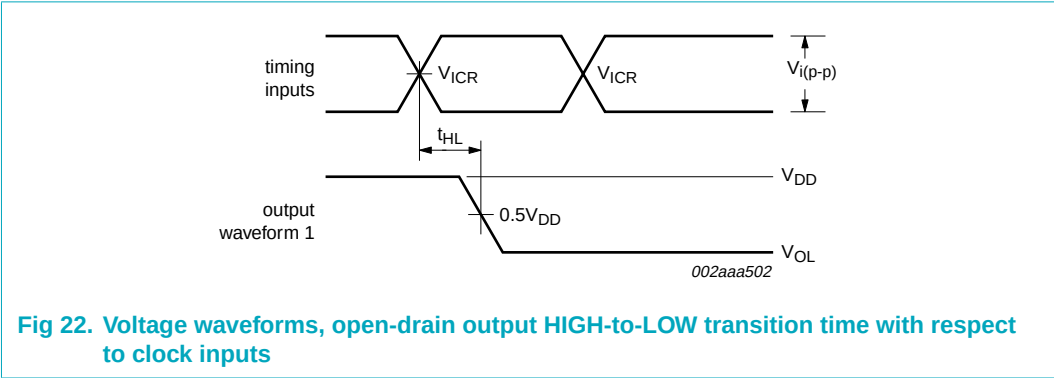
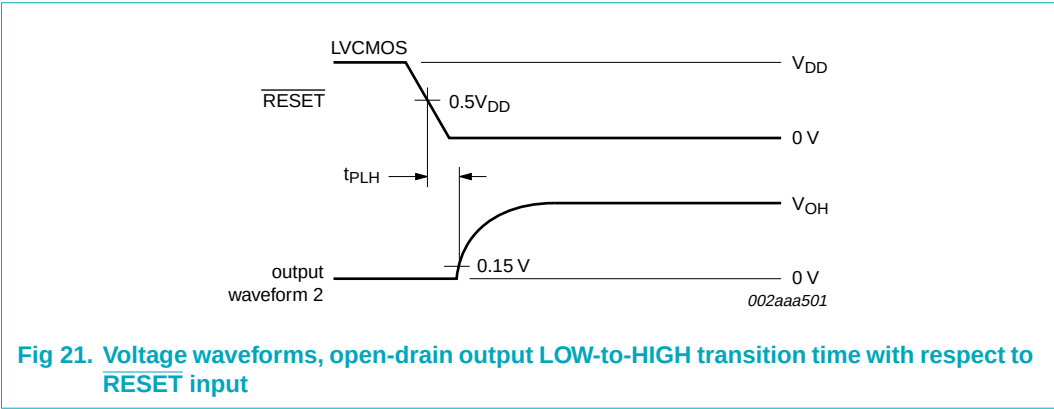
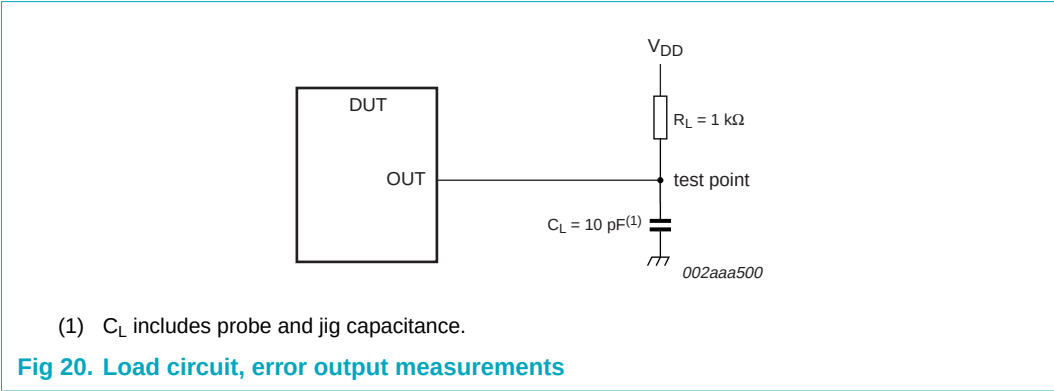
All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10\text{ MHz}$; $Z_0 = 50\text{ }\Omega$; input slew rate = $1\text{ V/ns} \pm 20\text{ }\%$, unless otherwise specified.



11.3 Error output load circuit and voltage measurement information

$V_{DD} = 1.8\text{ V} \pm 0.1\text{ V}.$

All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10\text{ MHz}$; $Z_0 = 50\text{ }\Omega$; input slew rate = $1\text{ V/ns} \pm 20\text{ }\%$, unless otherwise specified.



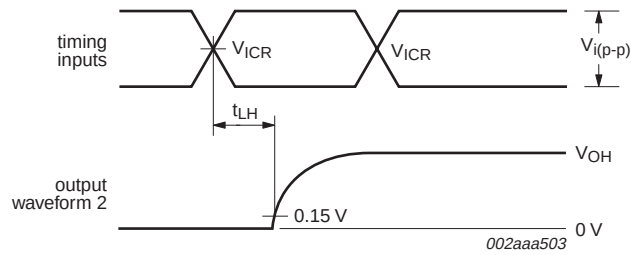
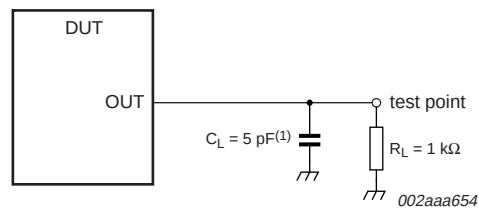


Fig 23. Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

11.4 Partial parity out load circuit and voltage measurement information

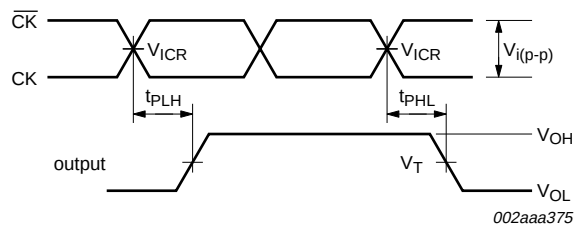
$$V_{DD} = 1.8 \text{ V} \pm 0.1 \text{ V.}$$

All input pulses are supplied by generators having the following characteristics:
 $PRR \leq 10 \text{ MHz}$; $Z_0 = 50 \Omega$; input slew rate = $1 \text{ V/ns} \pm 20 \%$, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Fig 24. Partial parity out load circuit

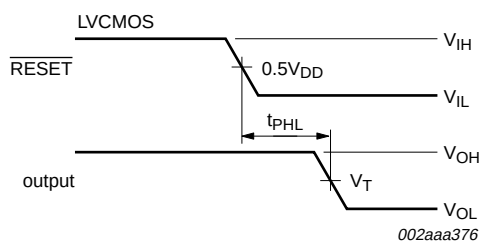


$$V_T = 0.5V_{DD}.$$

t_{PLH} and t_{PHL} are the same as t_{PD} .

$$V_{i(p-p)} = 600 \text{ mV.}$$

Fig 25. Partial parity out voltage waveforms; propagation delay times with respect to clock inputs



$V_T = 0.5V_{DD}$.

t_{PLH} and t_{PHL} are the same as t_{PD} .

$V_{IH} = V_{ref} + 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVC MOS inputs.

$V_{IL} = V_{ref} - 250 \text{ mV}$ (AC voltage levels) for differential inputs. $V_{IL} = \text{GND}$ for LVC MOS inputs.

Fig 26. Partial parity out voltage waveforms; propagation delay times with respect to RESET input

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

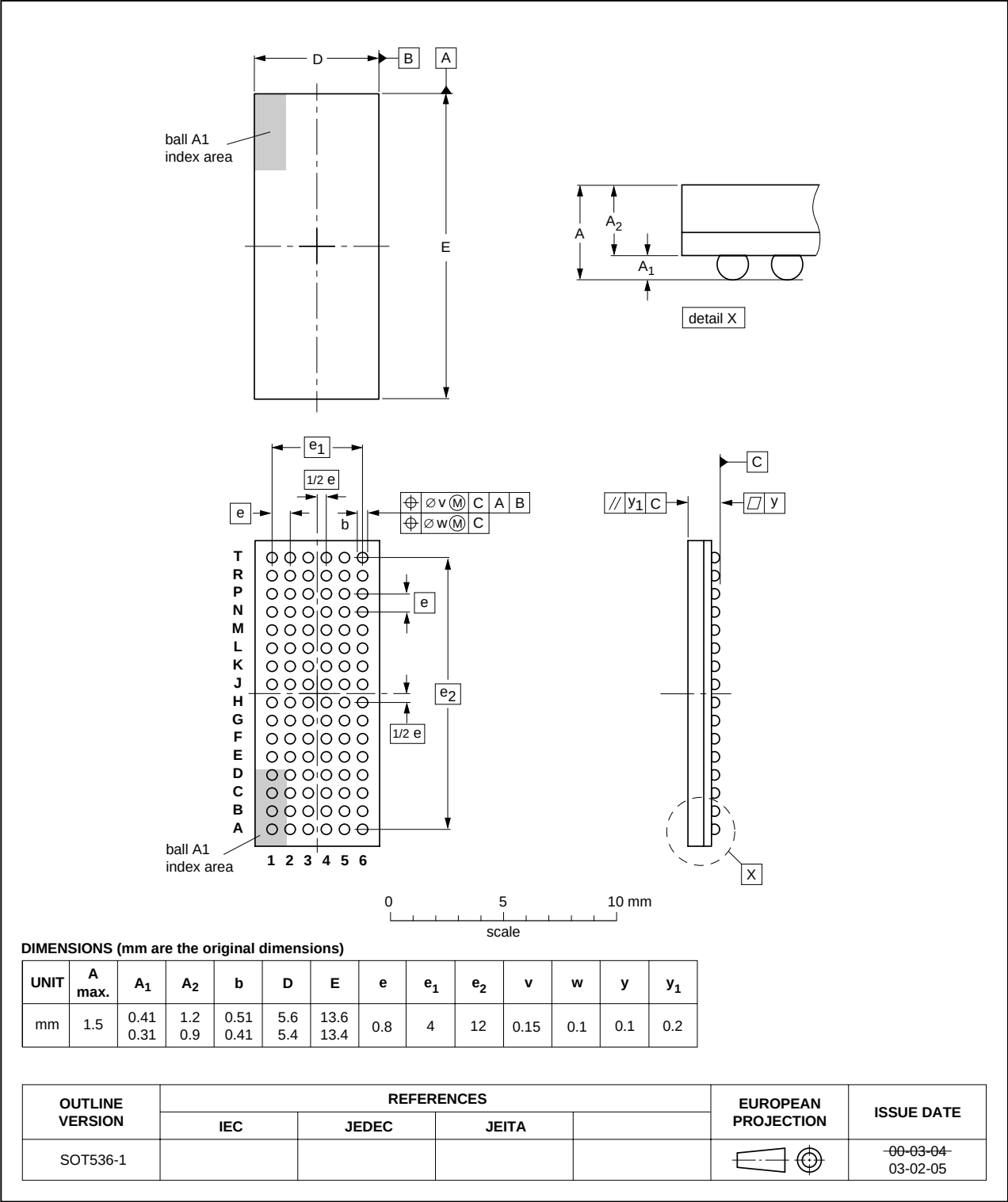


Fig 27. Package outline SOT536-1 (LFBGA96)

13. Soldering

13.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

13.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 14. SnPb eutectic process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ ≥ 350
< 2.5 mm	240 °C + 0/-5 °C	225 °C + 0/-5 °C
≥ 2.5 mm	225 °C + 0/-5 °C	225 °C + 0/-5 °C

Table 15. Pb-free process - package peak reflow temperatures (from J-STD-020C July 2004)

Package thickness	Volume mm ³ < 350	Volume mm ³ 350 to 2000	Volume mm ³ > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

13.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

- larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
- smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

13.5 Package related soldering information

Table 16. Suitability of surface mount IC packages for wave and reflow soldering methods

Package ^[1]	Soldering method	
	Wave	Reflow ^[2]
BGA, HTSSON..T ^[3] , LBGA, LFBGA, SQFP, SSOP..T ^[3] , TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable ^[4]	suitable
PLCC ^[5] , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ^{[5][6]}	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended ^[7]	suitable
CWQCCN..L ^[8] , PMFP ^[9] , WQCCN..L ^[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages*; Section: Packing Methods.

- [3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding $217\text{ }^{\circ}\text{C} \pm 10\text{ }^{\circ}\text{C}$ measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
- [4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- [5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- [6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- [7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
- [8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
- [9] Hot bar soldering or manual soldering is suitable for PMFP packages.

14. Abbreviations

Table 17. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
DIMM	Dual In-line Memory Module
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
PPO	Partial Parity Out
PRR	Pulse Repetition Rate
RDIMM	Registered Dual In-line Memory Module
SSTL	Stub Series Terminated Logic

15. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SSTUP32866_2	20060914	Product data sheet	-	SSTUP32866_1
Modifications:				
• Table 1 “Ordering information”: added Type number SSTUP32866EC/S • added Section 4.1 “Ordering options” • Figure 3 “Pin configuration for LFBGA96” modified (added Type number SSTUP32866EC/S) • Table 5 “Parity and standby function table”: added reference to Table note 4 at column heading “QERR” • Table 8 “Recommended operating conditions”, Symbol T_{amb}: added separate specifications for SSTUP32866EC/G and SSTUP32866EC/S • Table 10 “Timing requirements”, description below table title: changed “See Figure 2.” to “See Section 11.1.” • Table 11 “Switching characteristics (667 mode, SELAB = HIGH)” and Table 12 “Switching characteristics (800 mode, SELAB = LOW)”: – changed parameter description of t_{PDM} from “propagation delay, single bit switching” to “peak propagation delay” (moved “single bit switching” to Conditions column) – changed parameter description of t_{PDMSS} from “propagation delay, simultaneous switching” to “simultaneous switching peak propagation delay” • Figure 26 “Partial parity out voltage waveforms; propagation delay times with respect to RESET input”, 4th note: changed “$V_{IL} = V_{DD}$” to “$V_{IL} = GND$”				
SSTUP32866_1	20060406	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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