
Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip LAN8841. These checklist items should be followed when utilizing the LAN8841 in a new design. A summary of these items is provided in [Section 10.0, "Hardware Checklist Summary," on page 17](#). Detailed information on these subjects can be found in the corresponding section:

- [Section 2.0, "General Considerations"](#)
- [Section 3.0, "Power"](#)
- [Section 4.0, "Ethernet Signals"](#)
- [Section 5.0, "Clock Circuit"](#)
- [Section 6.0, "Digital Interfaces"](#)
- [Section 7.0, "1588 Support"](#)
- [Section 8.0, "Startup"](#)
- [Section 9.0, "Miscellaneous"](#)

2.0 GENERAL CONSIDERATIONS

2.1 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.2 Ground

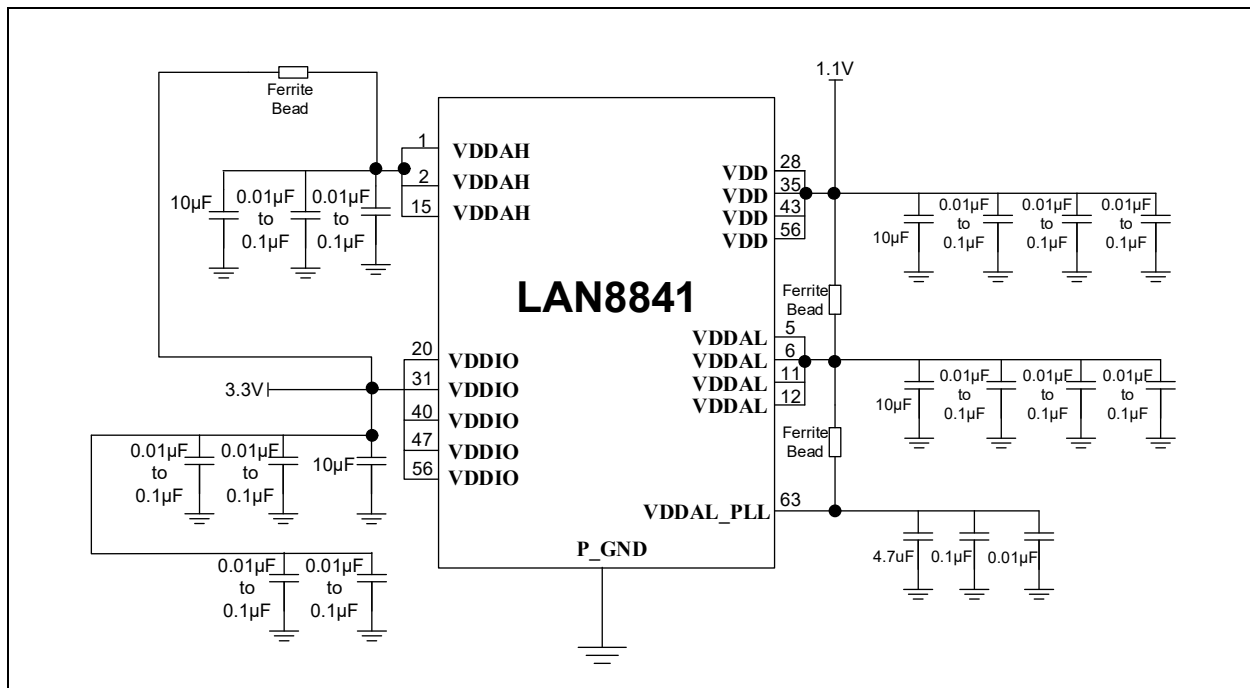
- The ground pins, **GND**, should be connected to the solid ground plane on the board.
- It is recommended that all ground connections be tied together to the same ground plane. Separate ground planes are not recommended.

LAN8841

3.0 POWER

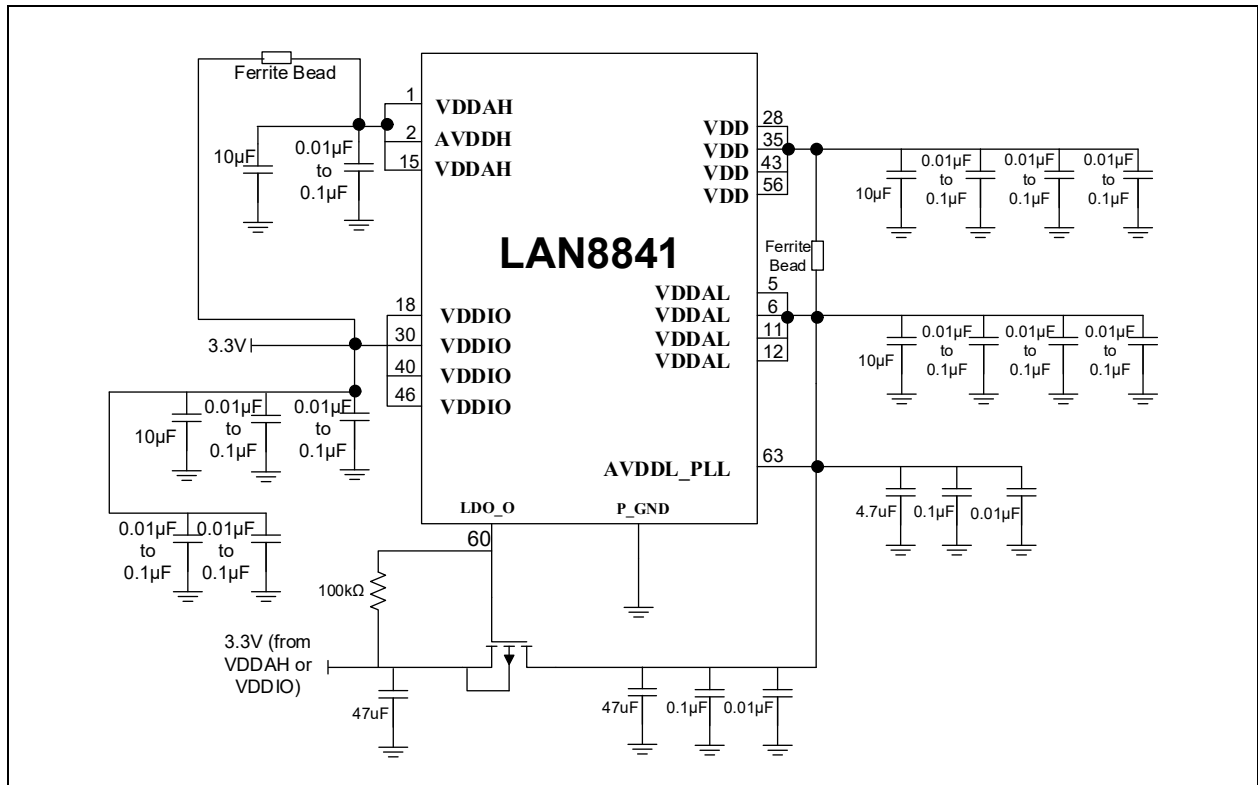
- The analog supply (**VDDAH**) is located on pins 1, 2, and 15, and requires a connection to **VDDIO** (created from +3.3V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220 Ω (at 100 MHz) ferrite bead is used. Each **VDDAH** pin should include 0.1 μ F and 10 μ F capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDDAL** (pins 5, 6, 11, and 12) is the analog core voltage supply. It should be connected to a +1.1V supply (created from +1.1V through a ferrite bead). Bulk capacitance should be placed on each side of the ferrite bead. Generally, a 100-220 Ω (at 100 MHz) ferrite bead is used. Each **VDD** pin should include 0.1 μ F and 22 μ F capacitors to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The **VDDIO** (pins 20, 31, 40, 47, and 56) is the variable supply voltage for the I/O pads. It should be connected to the +3.3V, 2.5V, or 1.8V supply. A bulk capacitor is needed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors must be placed as close as possible to the part to reduce high frequency noise being injected through EMI interference.
- The **VDD** (pins 28, 35, 43, and 56) is the digital core voltage supply. It should be connected to the +1.1V supply. A bulk capacitor is needed close to the source to prevent any droop in the supply when the part starts. Decoupling capacitors must be placed as close as possible to the part to reduce high frequency noise being injected through EMI interference.
- **VDDAL_PLL** (pin 63) supplies power to the LAN8841 PLL. Decouple with a 4.7-10 μ F capacitor, a 0.1 μ F capacitor, and a 0.01 μ F capacitor to ground, and join them to the +1.1V power trace or plane through a ferrite bead.
- The power and ground connections without using the LDO are shown in [Figure 3-1](#), and the power and ground connections with the LDO (using an external MOSFET) are shown in [Figure 3-2](#).

FIGURE 3-1: POWER AND GROUND CONNECTIONS WITHOUT LDO



Caution: This +1.2V supply is for internal logic only. Do *not* power other circuits or devices with this supply.

FIGURE 3-2: POWER AND GROUND CONNECTIONS WITH LDO



Caution: This +1.2V supply is for internal logic only. Do *not* power other circuits or devices with this supply.

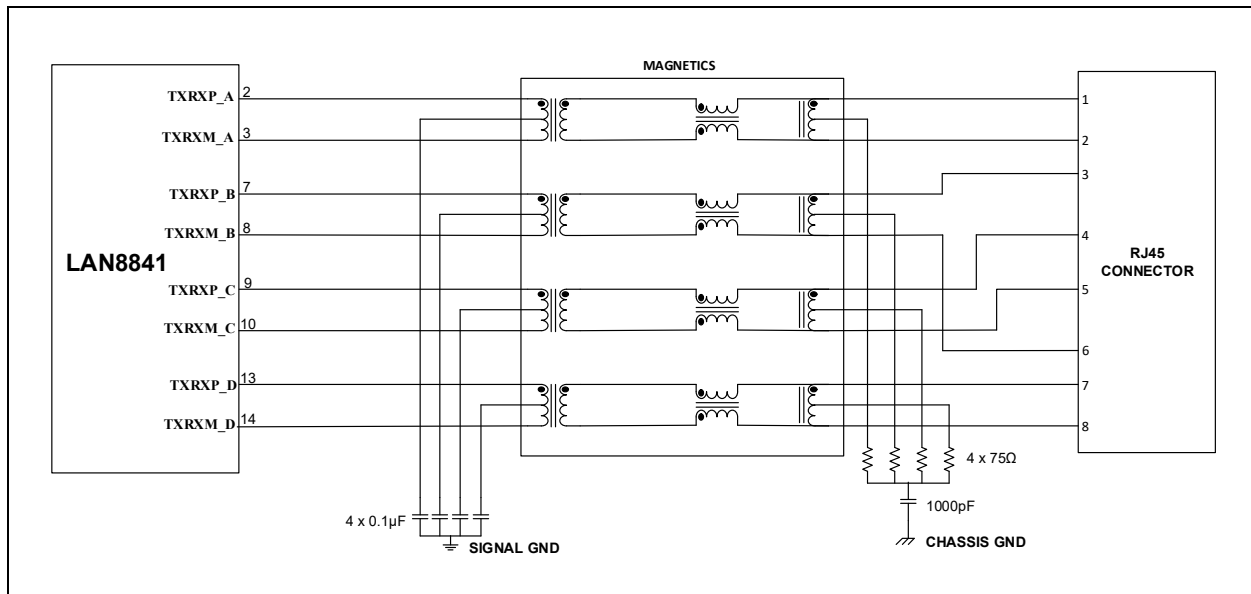
4.0 ETHERNET SIGNALS

4.1 10/100/1000 Mbps Interface Connection—Separate Center Tap

- **MAGJACK** (pin 17) must be pulled low for either separate center-tap magnetics or separate center-tap magnetic connectors.
- **TXRXP_A** (pin 3): This pin is the transmit (TX)/receive (RX) positive connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_A** (pin 4): This pin is the TX/RX negative connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_B** (pin 7): This pin is the TX/RX positive connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_B** (pin 8): This pin is the TX/RX negative connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_C** (pin 9): This pin is the TX/RX positive connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_C** (pin 10): This pin is the TX/RX negative connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_D** (pin 13): This pin is the TX/RX positive connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_D** (pin 14): This pin is the TX/RX negative connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

For 10/100/1000 Mbps channel connections details, refer to [Figure 4-1](#).

FIGURE 4-1: 10/100/1000 MBPS CHANNEL CONNECTIONS—SEPARATE CENTER TAP



4.2 10/100/1000 Magnetics Connection—Separate Center Tap

- The center tap connection on the LAN8841 side for pair A channel only connects a 0.1 μ F capacitor to GND, and no bias is needed.
- The center tap connection on the LAN8841 side for pair B channel only connects a 0.1 μ F capacitor to GND, and no bias is needed.
- The center tap connection on the LAN8841 side for pair C channel only connects a 0.1 μ F capacitor to GND, and no bias is needed.
- The center tap connection on the LAN8841 side for pair D channel only connects a 0.1 μ F capacitor to GND, and no bias is needed.
- The center taps of the magnetics of all pairs should not be connected together without this 0.1 μ F capacitor to ground. The reason is that the common-mode voltage can be different between pairs, especially for 10/100 operation (pairs A and B are active while pairs C and D are inactive).
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75 Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by pair A, pair B, pair C, and pair D center taps.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See [Section 9.2, "Other Considerations"](#) for guidance on how chassis ground should be created from digital or signal ground.

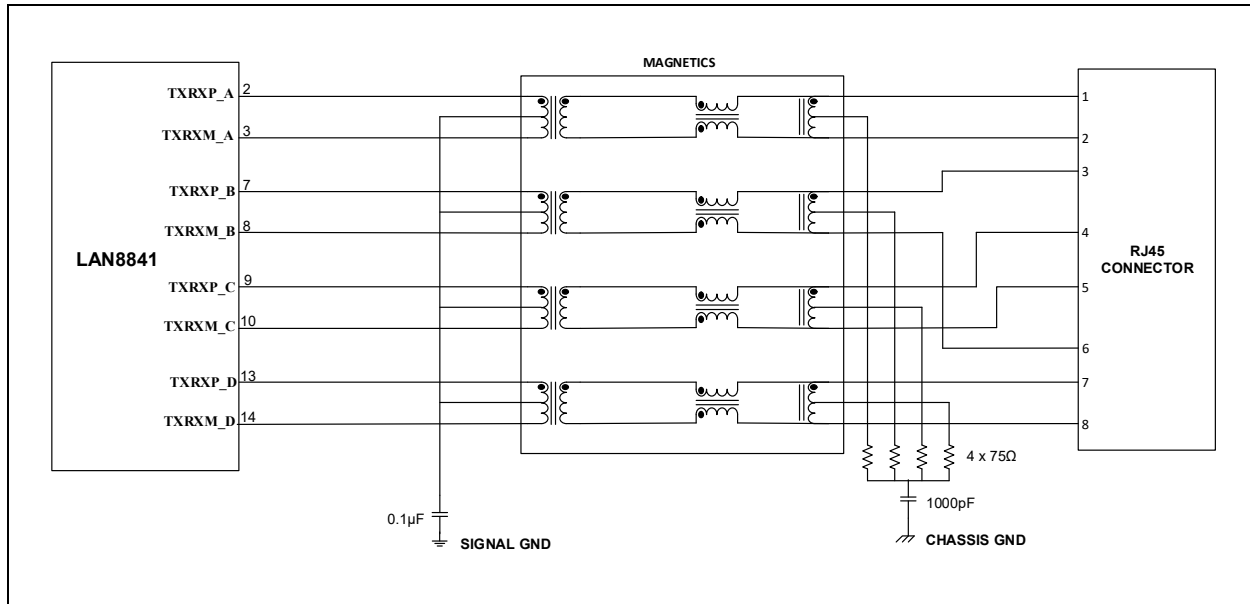
4.3 1000 Mbps Interface Connection—Shorted Center Tap

- **MAGJACK** (pin 17) must be pulled high for shorted center-tap magnetics and/or shorted center-tap magnetic connectors.
- **TXRXP_A** (pin 3): This pin is the TX/RX positive connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_A** (pin 4): This pin is the TX/RX negative connection from pair A of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_B** (pin 7): This pin is the TX/RX positive connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_B** (pin 8): This pin is the TX/RX negative connection from pair B of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_C** (pin 9): This pin is the TX/RX positive connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_C** (pin 10): This pin is the TX/RX negative connection from pair C of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXP_D** (pin 13): This pin is the TX/RX positive connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.
- **TXRXM_D** (pin 14): This pin is the TX/RX negative connection from pair D of the internal PHY. This pin connects to the 10/100/1000 magnetics. No external terminator and bias are needed.

LAN8841

For 10/100/1000 Mbps channel connections details, refer to [Figure 4-2](#).

FIGURE 4-2: 10/100/1000 MBPS CHANNEL CONNECTIONS—SHORTED CENTER TAP



4.4 10/100/1000 Magnetics Connection—Shorted Center Tap

- The center tap connection on the LAN8841 side for pairs A, B, C, and D connect to a 0.1 μ F capacitor to GND, and no bias is needed.
- The center tap connection for each pair (A, B, C, and D) on the cable side (RJ45 side) should be terminated with a 75 Ω resistor through a common 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by pair A, pair B, pair C, and pair D center taps.
- The RJ45 shield should connect to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See [Section 9.2, "Other Considerations"](#) for guidance on how chassis ground should be created from digital or signal ground.

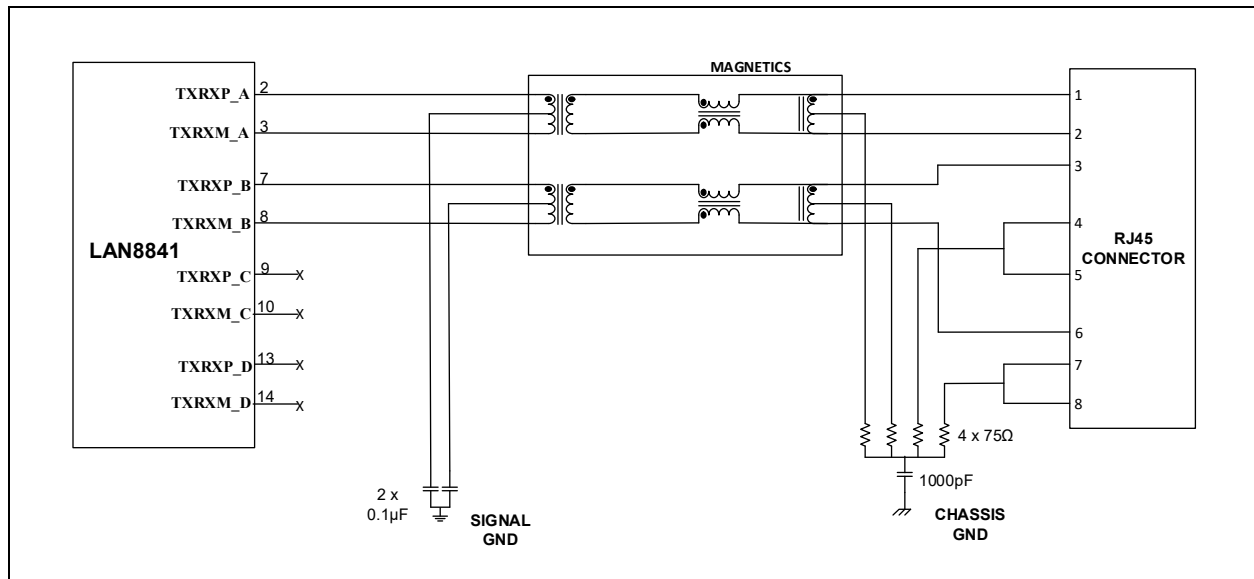
4.5 10/100 Mbps Interface Connection—RJ45 Connection

For designs needing only a 10/100 connection, the 1000 Mbps capability must be removed. The following removes the 1000 Mbps advertisement for auto-negotiation:

1. Set Port Register 0x00, Bit [6] = '0' to remove 1000 Mbps speed.
 2. Set Port Register 0x09, Bits [9:8] = '00' to remove auto-negotiation advertisements for 1000 Mbps.
 3. Write a '1' to Register 0x00, Bit [9], a self-clearing bit, to force a restart of auto-negotiation.
- **TXRXP_A** (pin 3): This pin is the TX/RX positive connection from pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
 - **TXRXM_A** (pin 4): This pin is the TX/RX negative connection from pair A of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
 - **TXRXP_B** (pin 7): This pin is the TX/RX positive connection from pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
 - **TXRXM_B** (pin 8): This pin is the TX/RX negative connection from pair B of the internal PHY. This pin connects to the 10/100 magnetics. No external terminator and bias are needed.
 - **TXRXP_C** (pin 10): This pin can be left as No Connect (NC).
 - **TXRXM_C** (pin 11): This pin can be left as NC.
 - **TXRXP_D** (pin 13): This pin can be left as NC.
 - **TXRXM_D** (pin 14): This pin can be left as NC.

For 10/100 Mbps channel connections details, refer to [Figure 4-3](#).

FIGURE 4-3: 10/100 MBPS CHANNEL CONNECTIONS—RJ45 CONNECTION



4.6 10/100 Magnetics Connection

- The center tap connection on the LAN8841 side for pair A (Transmit Channel) only connects a 0.1 μF capacitor to GND, and no bias is needed.
- The center tap connection on the LAN8841 side for pair B (Receive Channel) only connects a 0.1 μF capacitor to GND, and no bias is needed.
- The center taps of the magnetics of the TX and RX channels should not be connected together. The reason is the common-mode voltage can be different between pairs.
- The center tap connection on the LAN8841 side for the RX channel is connected to the TX channel center tap on the magnetics.
- The center tap connection on the cable side (RJ45 side) for pair A should be terminated with a 75 Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for pair B should be terminated with a 75 Ω resistor through a 1000 pF, 2 kV capacitor to chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both pair A and pair B center taps.
- MDI connections:
 - Pin 1 of the RJ45 is TX+ and should trace through the magnetics to TXRXP_A (pin 2) of the LAN8841.
 - Pin 2 of the RJ45 is TX- and should trace through the magnetics to TXRXM_A (pin 3) of the LAN8841.
 - Pin 3 of the RJ45 is RX+ and should trace through the magnetics to TXRXP_B (pin 7) of the LAN8841.
 - Pin 6 of the RJ45 is RX- and should trace through the magnetics to TXRXM_B (pin 8) of the LAN8841.
- MDIX Connections:
 - Pin 3 of the RJ45 is TX+ and should trace through the magnetics to TXRXP_B (pin 8) of the LAN8841.
 - Pin 6 of the RJ45 is TX- and should trace through the magnetics to TXRXM_B (pin 7) of the LAN8841.
 - Pin 1 of the RJ45 is RX+ and should trace through the magnetics to TXRXP_A (pin 2) of the LAN8841.
 - Pin 2 of the RJ45 is RX- and should trace through the magnetics to TXRXM_A (pin 3) of the LAN8841.
- When using the LAN8841 device in the Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module (that is, the one where the two channels are identical) is required.

4.7 10/100 Mbps RJ45 Connection

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of doing this:
 - Pins 4 and 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
 - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of doing this:
 - Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
 - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. So, by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground, an equivalent circuit is created.
- The RJ45 shield should be attached directly to chassis ground. This includes RJ45 connectors with or without integrated magnetics. See [Section 9.2, "Other Considerations"](#) for guidance on how chassis ground should be created from digital or signal ground.

5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections

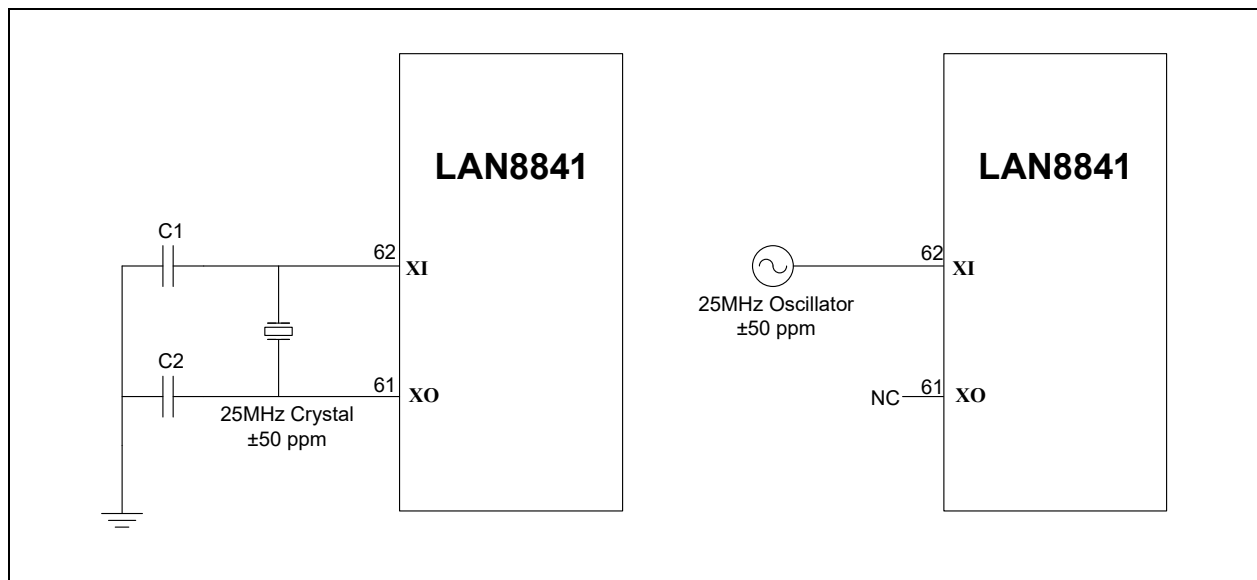
A 25.000 MHz (± 50 ppm) crystal should be used to provide the clock source. For exact specifications and tolerances, refer to the latest revision of the *LAN8841 Data Sheet*.

- **XI** (pin 62) is the clock circuit input for the LAN8841 device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.
- **XO** (pin 61) is the clock circuit output for the LAN8841 device. This pin requires a capacitor to ground. One side of the crystal connects to this pin.

Since every system design is unique, the capacitor values are system-dependent, based on the C_L spec of the crystal and the stray capacitance value. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.

Alternatively, a 25.000 MHz, 3.3V clock oscillator may be used to provide the clock source for the LAN8841. When using a single-ended clock source, **XO** should be left floating as a No Connect (NC).

FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS

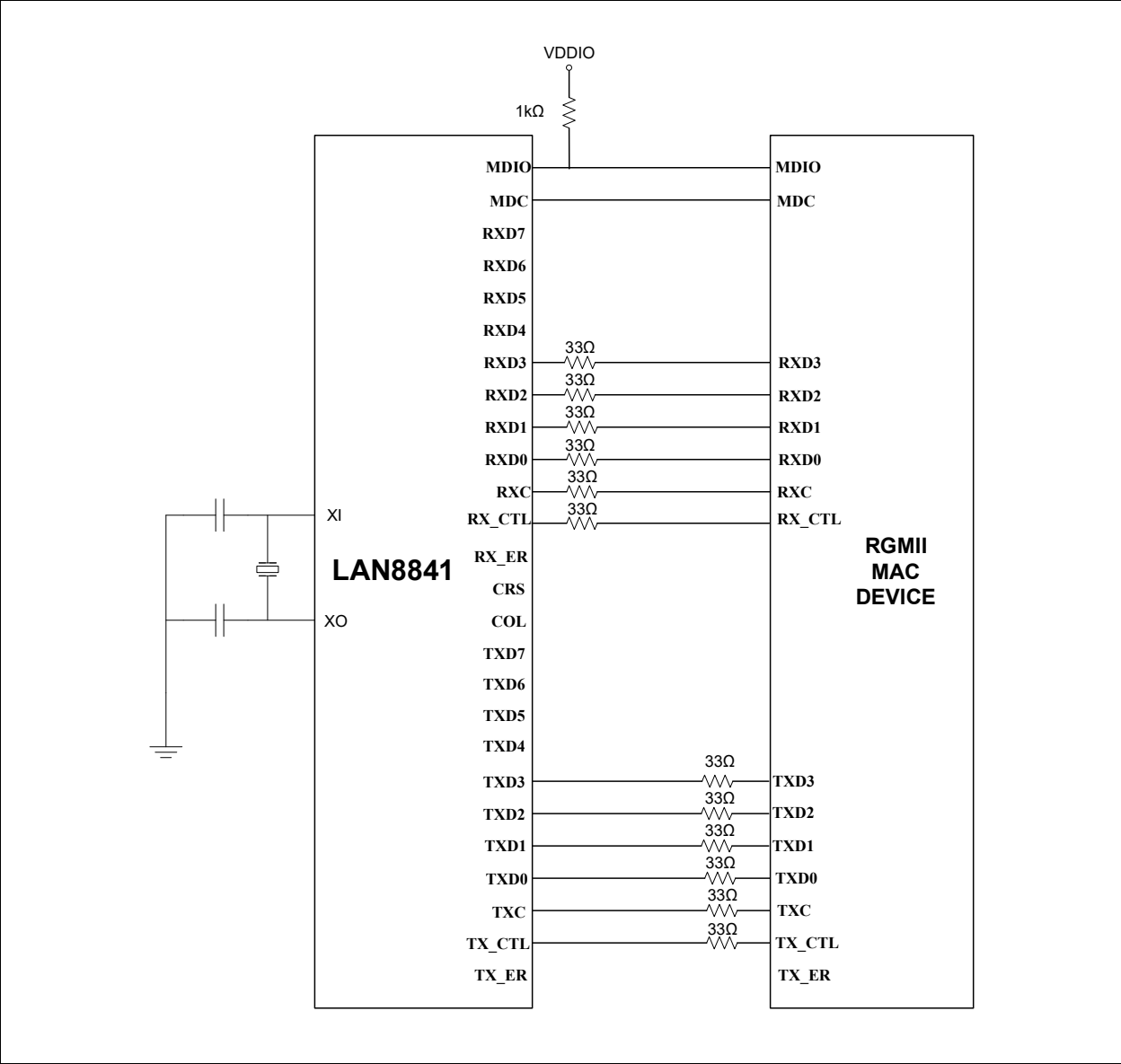


6.0 DIGITAL INTERFACES

6.1 RGMII Interface

- When utilizing either an external RGMII MAC interface, [Figure 6-1](#) indicates the proper connections for the 14 signals, including two management pins (MDC and MDIO).
- Provisions should be made for series terminations for all outputs on the RGMII interface. Series resistors enable the designer to closely match the output driver impedance of the LAN8841 and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

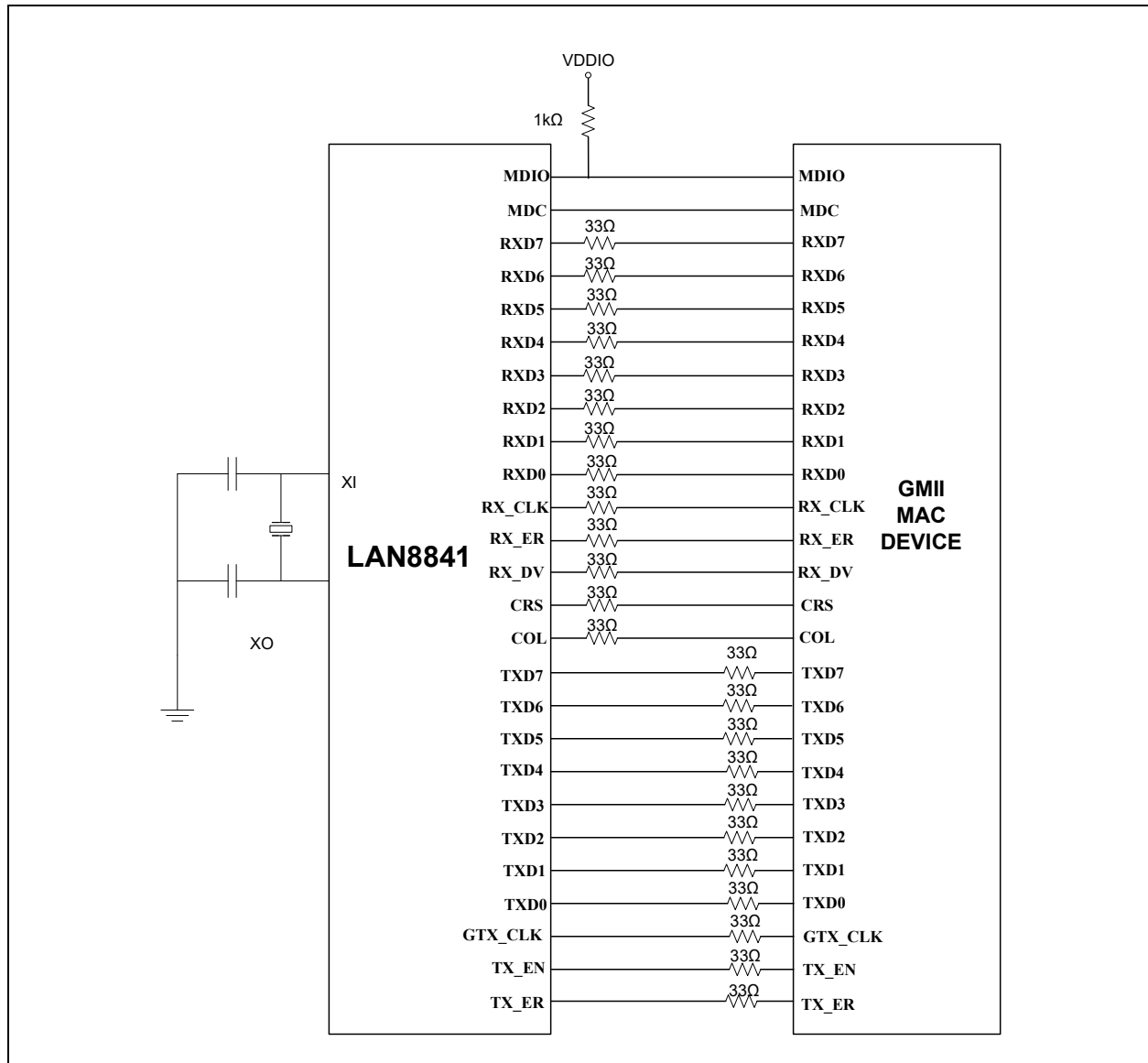
FIGURE 6-1: RGMII INTERFACE CONNECTIONS



6.2 GMII Interface

- When utilizing either an external GMII MAC interface, [Figure 6-2](#) indicates the proper connections for the 22 signals, including two management pins (MDC and MDIO).
- Provisions should be made for series terminations for all outputs on the GMII interface. Series resistors enable the designer to closely match the output driver impedance of the LAN8841 and the PCB trace impedance to minimize ringing on the signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors is 33Ω.

FIGURE 6-2: GMII INTERFACE CONNECTIONS



6.3 Required External Pull-ups

- When using the LAN8841 MDC/MDIO management pins, a pull-up resistor of 1 kΩ on the **MDIO** signal (pin 52) is required.
- If used, the **INT_N** pin (pin 54) requires a 4.7 kΩ external pull-up resistor since this output is an open drain. If the **INT_N** pin is not used, then this pin can float.

7.0 1588 SUPPORT

7.1 IEEE 1588 Pin Connections

The LAN8841 supports IEEE-1588 Timestamping functionality.

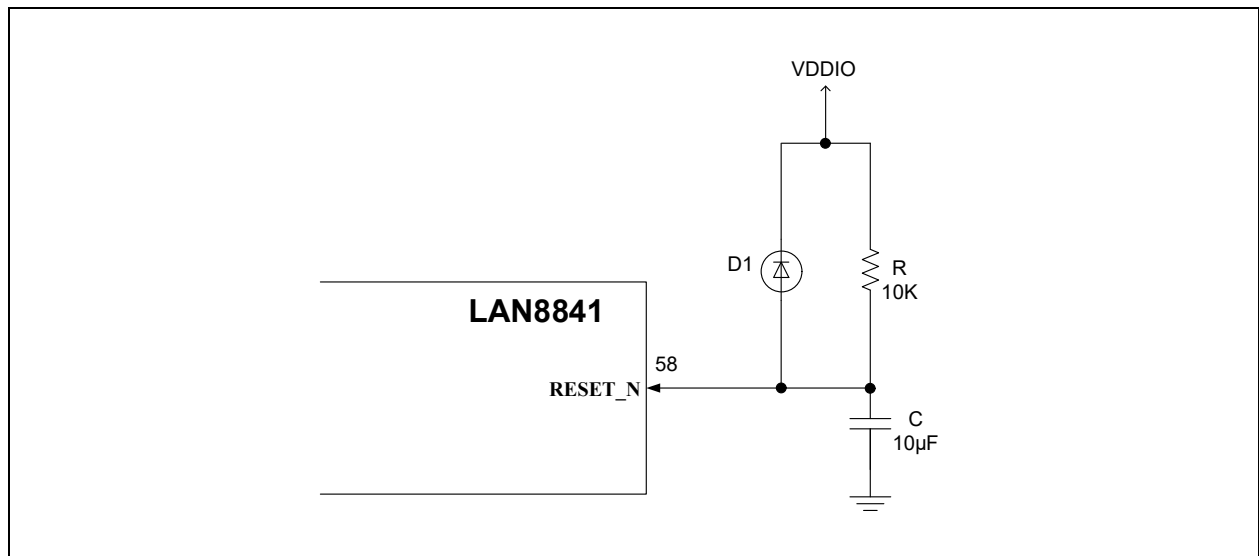
- **CLK125_NDO** (pin 57): **CLK125_EN** must be pulled up to enable. Default is 125 MHz clock output for either SyncE applications or a 125 MHz reference output. This pin can be configured to accept a reference clock if MMD Address 2, Register 258, bits 12:10 = 100. Acceptable clock input frequencies are 66.67 MHz, 71.43 MHz, 76.92 MHz, 83.33 MHz, 90.90 MHz, 100 MHz, 111.1 MHz, or 125.0 MHz.
- **1588_EVENT_A**: 1588 LTC Event A. When asserted, this pin signals that 1588 LTC Event A has occurred. This pin can also be configured to provide a PPS Output signal. This can be brought out on any of GPIO0 through GPIO9; however, GPIO selected for event trigger should not be used on LED lines used for Ethernet link/activity. Also, GPIO6 should not be used for this event trigger if CLK_NDO is used as a 1588 reference clock input.
- **1588_EVENT_B**: 1588 LTC Event B. When asserted, this pin signals that 1588 LTC Event B has occurred. This pin can also be configured to provide a PPS Output signal. This can be brought out on any of GPIO0 through GPIO9; however, GPIO selected for event trigger should not be used on LED lines used for Ethernet link/activity. Also, GPIO6 should not be used for this event trigger if CLK_NDO is used as a 1588 reference clock input.
- The default configuration of the **CLK125_NDO** pin sets the device to use an internal clock for the Local Time Counter (LTC). Refer to MMD Address 2, Register 258, bits 15:13 which control the reference clock source. The default value of MMD Address 2, Register 258 bits 15:13 is 000 (125 MHz clock from internal System PLL). To enable an external clock source, MMD Address 2, Register 258 bits 15:13 would need to be changed and set to 011 = External 1588_REF_CLK (can be 66.67 MHz, 71.43 MHz, 76.92 MHz, 83.33 MHz, 90.90 MHz, 100 MHz, 111.1 MHz, or 125.0 MHz).
- The local time counter keeps the local time for the device and the time is monitored and synchronized to an external reference by the CPU. The source clock for the counter is selected externally to be 66.67 MHz, 71.43 MHz, 76.92 MHz, 83.33 MHz, 90.90 MHz, 100 MHz, 111.1 MHz, or 125.0 MHz. The clock may also be a line clock or the dedicated **CLK125_NDO** pin. This clock source is selected in register. MMD Address 2, Register 258, bits 15:13 have the following options for Reference Clock Source:
 - 000 = 125 MHz clock (internal)
 - 001 = 200 MHz clock (internal)
 - 010 = 250 MHz clock (internal)
 - 011 = Receive clock (2.5 MHz, 25 MHz, or 125 MHz)
 - 100 = External input (can be 66.67 MHz, 71.43 MHz, 76.92 MHz, 83.33 MHz, 90.90 MHz, 100 MHz, 111.1 MHz, or 125.0 MHz)
 - 101 = RESERVED
 - 110 = RESERVED
 - 111 = RESERVED
- Please be aware that when the link drops while using the Recovered Clock Options, it will result in NO 1588 Ref Clock that causes undesired behavior.

8.0 STARTUP

8.1 Reset Circuit

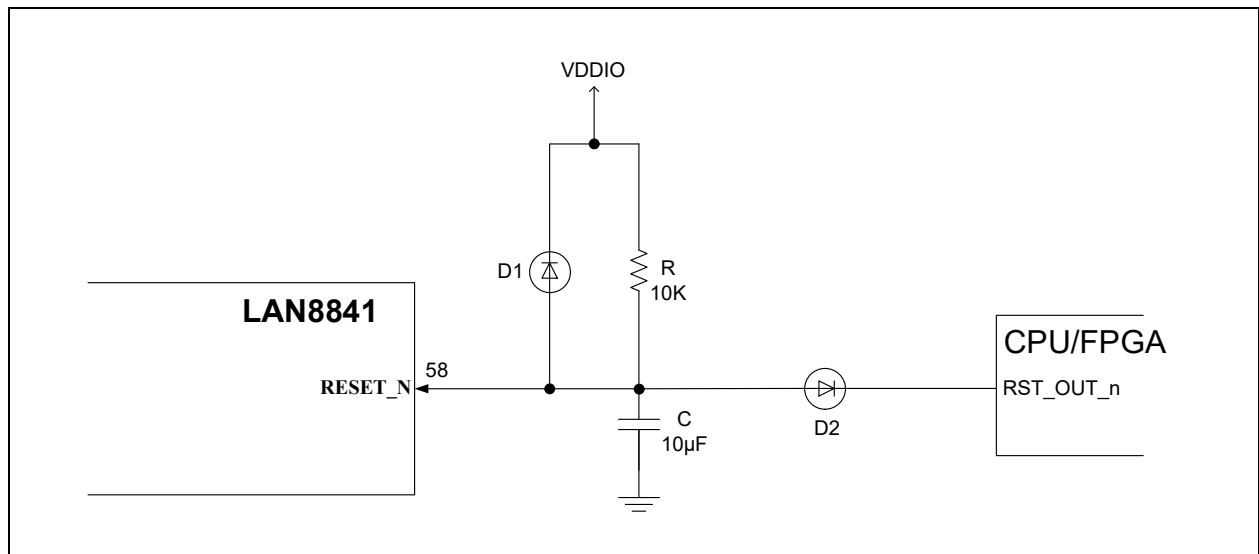
RESET_N (pin 58) is an active-low reset input. This signal resets all logic and registers within the LAN8841. A hardware reset (**RESET_N** assertion) is required following power-up. Refer to the latest copy of the *LAN8841 Data Sheet* for reset timing requirements. [Figure 8-1](#) shows a recommended reset circuit for powering up the LAN8841 when reset is triggered by the power supply.

FIGURE 8-1: RESET TRIGGERED BY POWER SUPPLY



[Figure 8-2](#) details the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset out pin (**RST_OUT_n**) from the CPU/FPGA provides the warm reset after power-up. If the Ethernet device and CPU/FPGA use the same **VDDIO** voltage, **D2** can be removed and both reset pins can be directly connected.

FIGURE 8-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



8.2 Configuration Mode Pins (Strapping Options)

The configuration mode pins of the LAN8841 (**MODE[4:0]**) control the default configuration of the LAN8841. Speed, duplex, auto-negotiation, and power-down functionality can be configured through these pins. The values of these strap pins are latched upon power-up and reset. In some systems, the MAC receive input pins may drive high during power-up or reset and consequently cause the PHY strap-in pins on the RGMII/GMII signals to be latched high. In this case, it is recommended to add 1 k Ω pull-downs on these PHY strap-in pins to ensure that the PHY does not strap in to an incorrect MODE configuration or is not configured with an incorrect PHY address. Refer to the *LAN8841 Data Sheet* for complete details for the operation of these pins.

8.3 LED Pins

The LAN8841 provides five LED signals. These indicators display speed, link, and activity information about the current state of the PHY. The LED pins drive low to light up the LED indicators, which should have their anode ends tied to 3.3V and their cathode ends tied through a series resistor (typically 220 Ω -470 Ω). Refer to the *LAN8841 Data Sheet* for further details on how to connect each pin for correct operation.

The LED functionality signal pins are shared with the following pin strapping functions:

- **LED1** is shared with **PHYAD0** and **LEDPOL1** on pin 21 for LAN8841.
- **LED2** is shared with **PHYAD1** and **LEDPOL2** on pin 19 for LAN8841.
- **LED3** is shared with **PHYAD2** and **LEDPOL3** on pin 18 for LAN8841.
- **LED4** is shared with **PHYAD3** and **LEDPOL4** on pin 17 for LAN8841.
- **LED5** is shared with **ALLPHYAD** and **LEDPOL5** on pin 16 for LAN8841.

Note 1: For 1.8V VDDIO, LED indication support is not recommended due to the low voltage. Without the LED indicator, the **PHYAD3**, **PHYAD2**, **PHYAD1**, and **PHYAD0/PME_N1** strapping pins are functional with a 4.7 k Ω pull-up to 1.8V VDDIO (or be floated) for a value of '1', and with a 1.0 k Ω pull-down to ground for a value of '0'.

2: If using RJ45 jacks with integrated LEDs and 1.8V VDDIO, a level shifting is recommended from 1.8V to 3.3V. In this case, a bipolar transistor or a level shifting device can be used.

8.4 GPIO Pins

- The LAN8841 provides ten signals for IEEE 1588 Precision Timing Protocol (PTP) support. The GPIO pins are shared with the following signals:
 - **GPIO0** is shared with **LED1** on pin 21 for LAN8841.
 - **GPIO1** is shared with **LED2** on pin 19 for LAN8841.
 - **GPIO2** is shared with **LED3** on pin 18 for LAN8841.
 - **GPIO3** is shared with **LED4** on pin 17 for LAN8841.
 - **GPIO4** is shared with **LED5** on pin 16 for LAN8841.
 - **GPIO5** is shared with **INT_N** on pin 54 for LAN8841.
 - **GPIO6** is shared with **CLK125_NDO** on pin 57 for LAN8841.
 - **GPIO7** is shared with **TX_ER** on pin 32 for LAN8841.
 - **GPIO8** is shared with **CRS** on pin 50 for LAN8841.
 - **GPIO9** is shared with **COL** on pin 53 for LAN8841.
- For GPIO pins, the recommendation is to use unused LED pins IEEE 1588 functions as a traditional RJ45 will have two or three LEDs for operation. Alternatively, if there is no 125 MHz clock reference needed, the **CLK125_NDO/GPIO6** can be used.
- For LAN8841 in RGMII mode, **GPIO7**, **GPIO8**, and/or **GPIO9** can be used since the **TX_ER**, **CRS**, and **COL** are unused in RGMII mode.

9.0 MISCELLANEOUS

9.1 ISET Resistor

The ISET pin on the LAN8841 must connect to ground through a 6.04 k Ω resistor with a tolerance of 1.0%. This is used to set up critical bias currents for the embedded 10/100/1000 Ethernet physical device.

9.2 Other Considerations

- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the digital ground. This allows some flexibility at EMI testing for different grounding options. Leaving the footprint open allows the two grounds to remain separate. Shorting them together with a zero ohm resistor connects them. For best performance, short them together with a cap or a ferrite bead.
- Be sure to incorporate enough bulk capacitors (4.7-22 μ F) for each power plane.

LAN8841

NOTES:

10.0 HARDWARE CHECKLIST SUMMARY

TABLE 10-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Pin Check"	Verify that the pins match the data sheet.		
	Section 2.2, "Ground"	Verify that the grounds are tied together.		
Section 3.0, "Power"	Section 3.0, "Power"	• Ensure that VDDAH is in the range 3.135V to 3.465V and a 10 μF or 22 μF capacitor is on each pin bulk capacitor and there are at least two 0.1 μF capacitors. • Ensure that VDDIO is in the range 3.135V to 3.465V and a 10 μF or 22 μF capacitor bulk capacitor and there are at least four 0.1 μF capacitors. • VDDL requires a 10 μF or 22 μF capacitor bulk capacitor and at least three 0.1 μF capacitors. • VDDAL requires a 10 μF or 22 μF capacitor bulk capacitor and at least three 0.1 μF capacitors. • For LDO designs, check the capacitance on both the drain and source of FET have at least 47 μF. • For LDO designs, make sure that the 100 kΩ resistor is in place (see Figure 3-2) to prevent in-rush current.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 4.0, "Ethernet Signals"	Section 4.1, "10/100/1000 Mbps Interface Connection—Separate Center Tap"	Verify each pair's positive and negative connections go to the following: • Pair A - Pair 1 of the magnetics • Pair B - Pair 2 of the magnetics • Pair C - Pair 3 of the magnetics • Pair D - Pair 4 of the magnetics		
	Section 4.2, "10/100/1000 Magnetics Connection—Separate Center Tap"	Verify each of pair A, pair B, pair C, and pair D center taps go from a 0.1 μ F capacitor to digital/signal GND. There cannot be a shorting of the connections to a common point before these capacitors.		
		Each cable side center tap go through a 75 Ω resistor.		
		All center taps go through a 1000 pF, 2 kV capacitor to chassis GND.		
	Section 4.3, "1000 Mbps Interface Connection—Shorted Center Tap"	Verify each pair's positive and negative connections go to the following: • Pair A - Pair 1 of the magnetics • Pair B - Pair 2 of the magnetics • Pair C - Pair 3 of the magnetics • Pair D - Pair 4 of the magnetics		
	Section 4.4, "10/100/1000 Magnetics Connection—Shorted Center Tap"	Verify pair A, pair B, pair C, and pair D are tied together and then go to a 0.1 μ F capacitor to digital/signal GND.		
		Each cable side center tap go through a 75 Ω resistor.		
		All center taps go through a 1000 pF, 2 kV cap. to chassis GND.		
	Section 4.5, "10/100 Mbps Interface Connection—RJ45 Connection" (10/100 only)	Verify each pair's positive and negative connections go to the following: • Pair A - Pair 1 of the magnetics • Pair B - Pair 2 of the magnetics • Pair C - No Connect (NC) • Pair D - No Connect (NC)		
		Verify each of pair A and pair B center taps go from a 0.1 μ F capacitor to digital/signal GND.		
	Section 4.6, "10/100 Magnetics Connection"	Verify the magnetics on each cable side center tap goes through a 75 Ω resistor terminated with RJ45 pins 4/5 and RJ45 pins 7/8 through a 1000 pF, 2 kV capacitor.		
	Section 4.7, "10/100 Mbps RJ45 Connection"	Verify that pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2-kV capacitor.		

TABLE 10-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	✓	Notes
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections"	Verify usage of 25 MHz $\pm$ 50 ppm crystal or 25 MHz $\pm$ 50 ppm clock source.		
Section 6.0, "Digital Interfaces"	Section 6.1, "RGMII Interface"	Confirm proper RGMII signals between MAC and PHY interface based on Figure 6-1 (RGMII).		
	Section 6.2, "GMII Interface"	Confirm proper GMII signals between MAC and PHY interface based on Figure 6-2 (GMII).		
Section 7.0, "1588 Support"	Section 7.1, "IEEE 1588 Pin Connections"	Confirm correct IEEE 1588 pin connections.		
Section 8.0, "Startup"	Section 8.1, "Reset Circuit"	Confirm proper reset circuit design: standalone reset or external CPU/FPGA reset.		
	Section 8.2, "Configuration Mode Pins (Strapping Options)"	Confirm mode settings and PHYAD (PHY Address) settings. In systems where the MAC receive input pins are driven high after reset, it is recommended to add 1 k Ω pull-downs on the PHY strap pins.		
	Section 8.3, "LED Pins"	If used, confirm proper connections, taking into consideration shared functionality on select LED pins.		
	Section 8.4, "GPIO Pins"	If used, confirm proper connections, taking into consideration shared functionality on select GPIO pins.		
Section 9.0, "Miscellaneous"	Section 9.1, "ISET Resistor"	Confirm proper ISET resistor (6.04 k Ω , 1.0%).		
	Section 9.2, "Other Considerations"	- Incorporate a large SMD footprint (SMD_1210) to connect the chassis ground to the chip ground instead of the digital ground. - Incorporate sufficient power plane bulk capacitors (4.7-22 μF).		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00004681B (10-07-22)	Section 3.0, "Power"	Updated Figure 3-2 and removed a note underneath it.
DS00004681A (07-22-22)	Initial release	

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