Three-Phase Sensorless Pump Driver IC

FEATURES AND BENEFITS

- AEC-Q100 qualified
- I²C serial port control
- Fast startup features
- Trapezoidal drive
- Sensorless (no Hall sensors required)
- Low $R_{DS(ON)}$ power MOSFETs
- FG speed output
- Lock detection
- Soft start
- Overcurrent protection
- Overvoltage protection
- Diagnostic outputs
- Small form factor automotive pump

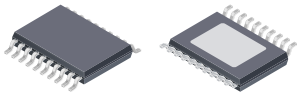
DESCRIPTION

The A89303 three-phase motor driver incorporates sensorless drive intended to drive low power automotive BLDC motors. A trapezoidal drive algorithm is implemented to minimize time to ramp up to maximum speed.

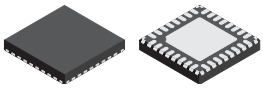
The device can be operated by PWM duty or I²C interface. The I²C serial port can be used to customize the startup and running operation via EEPROM.

The A89303 is available in a 20-lead TSSOP with exposed power pad (suffix LP) and a 32-contact 5 mm × 5 mm QFN with exposed thermal pad and wettable flank (suffix ET).

PACKAGES:



20-lead TSSOP with exposed thermal pad (LP package)



32-contact QFN with exposed thermal pad and wettable flank 5 mm × 5 mm × 0.90 mm (ET package)

Not to scale

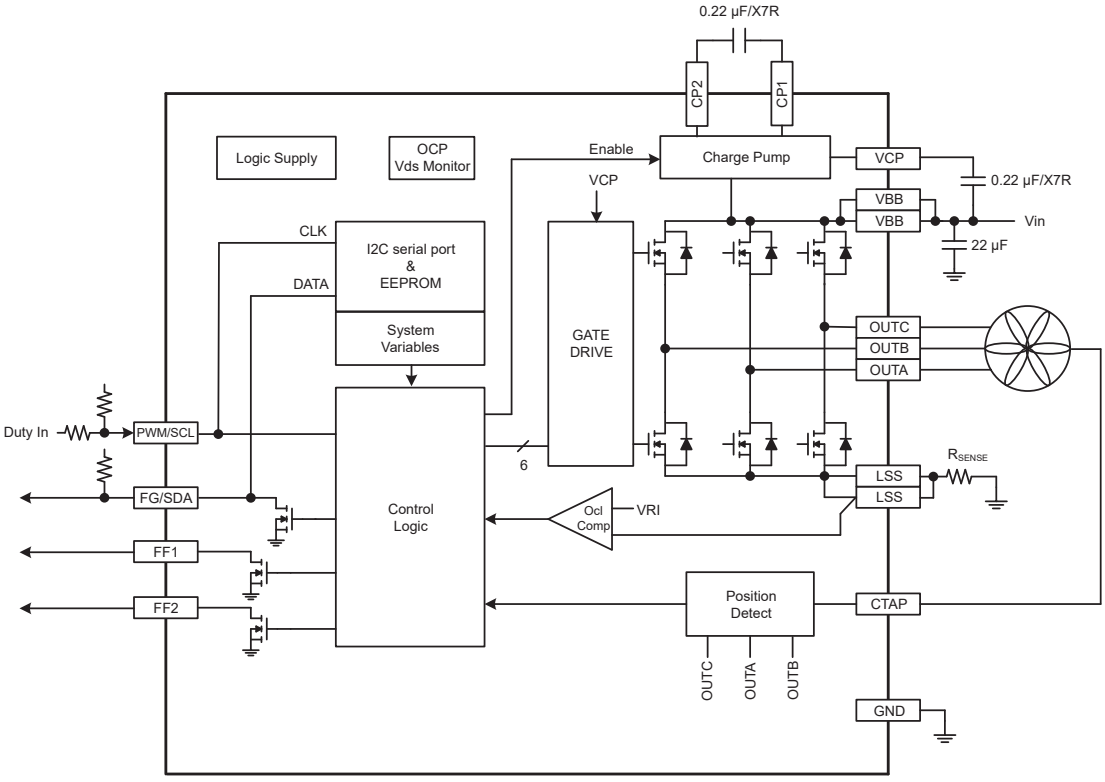


Figure 1: Typical Application

SPECIFICATIONS

SELECTION GUIDE

Part Number	Operating Temperature Range (T_A) (°C)	Packaging	Packing
A89303KLPTR-T	–40 to 125	20-lead TSSOP with exposed thermal pad	4000 pieces per 13-inch reel
A89303KETSR-J	–40 to 125	32-contact QFN with exposed thermal pad and wettable flank	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		–0.3 to 40	V
Logic Input Voltage Range	V_{IN}	PWM	–0.3 to 6	V
Logic Output	V_O	FG, FF1, FF2	–0.3 to 6	V
Output Current	I_{OUT}		3.6	A
LSS	V_{LSS}	DC	±0.36	V
		t < 200 ns	±2.5	V
Output Voltage	V_{OUT}	OUTA, OUTB, OUTC	–1.5 to V_{BB} + 1	V
CTAP			–0.6 to V_{BB} + 0.6	V
VCP			V_{BB} – 0.3 to V_{BB} + 8	V
CP1			–0.3 to V_{BB} + 0.3	V
CP2			V_{BB} – 0.3 to V_{CP} + 0.3	V
Maximum EEPROM write cycles	$EEPROM_{W(MAX)}$		1000	cycles
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A		–40 to 125	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	20-lead TSSOP (package LP), on 2-sided PCB 1-in.^{2} copper	35	°C/W
		32-contact QFN (package ET), on 2-sided PCB 1-in.^{2} copper	40	°C/W

*Additional thermal information available on the Allegro website.

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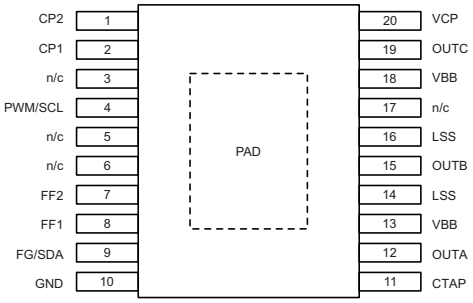
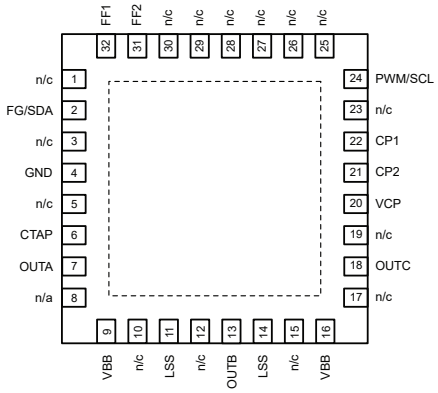
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



LP Package Pinout



ET Package Pinout

Terminal List Table

Name	Number		Description
	LP	ET	
CP2	1	21	Charge pump capacitor
CP1	2	22	Charge pump capacitor
n/c	3	23	
PWM/SCL	4	24	Logic input – PWM duty or I2C clock
n/c	5	25, 26, 27	
n/c	6	28, 29, 30	
FF2	7	31	Logic output signal
FF1	8	32	Logic output signal
n/c	–	1	
FG/SDA	9	2	I/O – Speed output signal or I2C data
n/c	–	3	
GND	10	4	Ground
n/c	–	5	
CTAP	11	6	Motor common
OUTA	12	7	Motor terminal
n/c	–	8	
VBB	13	9	Input supply
n/c	–	10	
LSS	14	11	Low-side source connection
n/c	–	12	
OUTB	15	13	Motor terminal
LSS	16	14	Low-side source connection
n/c	17	15	
VBB	18	16	Input supply
n/c	–	17	
OUTC	19	18	Motor terminal
n/c	–	19	
VCP	20	20	Charge pump capacitor
PAD	–	–	Exposed pad for enhanced thermal dissipation; connect to GND pin

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ELECTRICAL CHARACTERISTICS: Valid for T_J = –40°C to 125°C and V_{BB} = 5.5 to 40 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Load Supply Operating Range	V_{BB}	Driving	5.5	–	V_{BBOV}	V
		Operating	5.5	–	40	V
VBB Supply Current	I_{BB}	Active mode (PWM duty < DC_ON)	–	8.5	12	mA
Charge Pump	V_{CP}	Relative to V_{BB}, V_{BB} = 8 V	6.5	7	7.7	V
		Relative to V_{BB}, V_{BB} = 5.5 V	4	5	–	V
POWER DRIVER						
Total Driver On-Resistance (Sink + Source)	$R_{DS(ON)}$	I_{OUT} = 1.5 A, T_J = 25°C, V_{BB} = 12 V	–	300	–	mΩ
		I_{OUT} = 1.5 A, T_J = 125°C, V_{BB} = 12 V	–	450	520	mΩ
		Source Driver, T_J = 25°C, V_{BB} = 12 V	–	150	–	mΩ
		Sink Driver, T_J = 25°C, V_{BB} = 12 V	–	150	–	mΩ
Motor PWM Frequency	f_{PWM}		23.3	24.5	25.7	kHz
MOTOR CONTROL LOGIC						
PWM Input Frequency Range	f_{PWMIN}		2.1	–	45	kHz
Duty Cycle On Threshold	DC_{ON}		9.5	10	10.5	%
Duty Cycle Off Threshold	DC_{OFF}		7	7.4	8	%
External PWM Delay ON	t_{PWM_ON}		494	520	546	µs
External PWM Delay OFF	t_{PWM_OFF}		494	520	546	µs
PROTECTION CIRCUITS						
VBB Undervoltage Threshold	V_{BBUVLO}	V_{BB} rising	4.7	4.85	5	V
VBB Undervoltage Hysteresis	V_{BBHYS}		400	500	600	mV
VBB Overvoltage	V_{BBOV}	V_{BB} rising	29	–	31.5	V
VBB Overvoltage Hysteresis	$V_{BBOVHYS}$		1.5	2	2.5	V
VCP UVLO	V_{CPUVLO}	V_{CP} rising	3.6	3.85	4.1	V
VCP UVLO Hysteresis	$V_{CPUVHYS}$		200	–	400	mV
Charge Pump Power Up Time [2]	t_{VCPUV}		–	80	400	µs
POR Delay Time [2]	t_{POR_DELAY}		–	80	90	µs
Overcurrent Threshold	V_{OCL}	V_{RI} = 160 mV	–5	0	5	%
Overcurrent Protection	I_{OCP}		5	–	–	A
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	165	175	185	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C

[1] Specified limits are tested at a single temperature and assured over temperature range by design and characterization.

[2] Ensured by design and characterization, not production tested

Continued on next page...

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ELECTRICAL CHARACTERISTICS (continued): Valid for T_J = –40°C to 125°C and V_{BB} = 5.5 to 40 V, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC/INPUT OUTPUT/I²C						
Input Current (PWM, FG)	I_{IN}	V_{IN} = 0 to 5.5 V	–5	<1	5	µA
Logic Input Low Level	V_{IL}		0	–	0.8	V
Logic Input High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage	V_{SAT}	I = 5 mA	–	–	0.3	V
Logic Output Leakage (FG, FF1, FF2)	I_{FG}	V = 5.5 V, switch OFF	–	–	5	µA
I²C TIMING						
SCL Clock Frequency	f_{CLK}		8	–	400	kHz
Bus Free-Time Between Stop/Start	t_{BUF}		1.3	–	–	µs
Hold Time Start Condition	$t_{HD:STA}$		0.6	–	–	µs
Setup Time for Start Condition	$t_{SU:STA}$		0.6	–	–	µs
SCL Low Time	t_{LOW}		1.3	–	–	µs
SCL High Time	t_{HIGH}		0.6	–	–	µs
Data Setup Time	$t_{SU:DAT}$		100	–	–	ns
Data Hold Time	$t_{HD:DAT}$		0	–	900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		0.6	–	–	µs

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FUNCTIONAL DESCRIPTION

Basic Operation

The A89303 targets automotive pump BLDC applications to meet the objectives of fast startup, high efficiency, and robust protection features.

The speed of the fan is typically controlled by variable duty cycle PWM input. The duty cycle is measured and converted to a 9-bit number. This 9-bit "demand" is translated to a PWM duty cycle applied to the motor windings, effectively a percentage of the power supply voltage.

Protection features include lock detection with restart, overcurrent limit, overvoltage protection, motor output short-circuit protection (OCP), thermal shutdown, and undervoltage monitors (VBB, VCP).

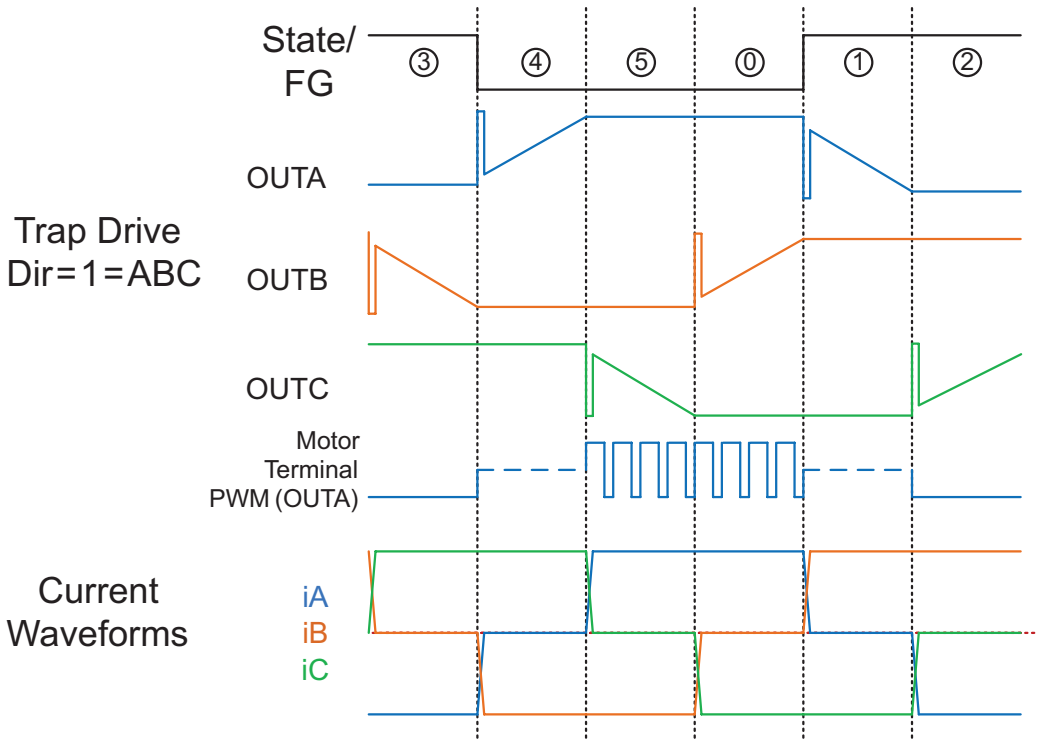

Figure 2: Trapezoidal Drive Sequence

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FG. Open-drain output. Represents electrical frequency of the motor. Additionally, the FG pin serves as the data line (SDA) for I^2C communication.

PWM. Speed demand input. The demand can be in the form of duty cycle, or direct I^2C command. The PWM pin also is the I^2C clock input (SCL). The allowable frequency range for duty input is 2.1 to 45 kHz. There is a 520 µs delay after PWM changes for logic to detect a valid ON or OFF command.

LOCK DETECT. During motor operation, the core logic will check to see if motor is synchronized based on comparison of expected back-EMF zero crossing to the actual back-EMF zero crossing. If it is determined the rotor has lost synchronization, the A89303 will disable the outputs before attempting a motor restart.

CTAP. Connection for the motor common. This pin must be left open if not connected.

CHARGE PUMP (VCP, CP1, CP2). A charge pump is used to generate a gate supply 7 V greater than V_{BB} in order to drive the source side DMOS gates. Two 0.22 µF ceramic capacitors are required for this function, connected as shown in application diagram. The charge pump is disabled when the PWM input is less than duty cycle thresholds. The charge pump circuit also integrates an undervoltage monitor to protect against turning on DMOS outputs when VCP is too low.

OVP. The outputs can be disabled if power supply voltage exceeds threshold V_{BBOV}.

Motor Lead Fault (OCP). Overcurrent Protection, V_{DS} monitor. To protect from short to ground, shorted load, or short to battery conditions for the motor lines, the voltage across the power outputs are always monitored when the MOSFET is turned ON. There will be a short blank time before the motor outputs are disabled if the overcurrent protection limit I_{OCP} is exceeded. The fault is latched off and can only be reset by power cycle or PWM on/off cycle.

Note: During the shorted event, the absolute maximum ratings may be exceeded for the blank time.

OCL. Overcurrent Limit. The voltage on LSS pin is monitored to limit current in the motor outputs. The overcurrent threshold voltage VRI can be programmed via EEPROM.

$$I_{OCL} = V_{RI} / R_{SENSE}$$

where V_{RI} = (Code + 1) × 10 mV ; Code = [15..31]

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Fault Flags. Two open drain fault pins indicate status as follows.

FF2	FF1	Fault Condition
0	0	No Fault – Normal operation
0	1	Temperature Fault [1]
1	0	Motor Lead Fault – Short to Ground, Short to Battery, Shorted load, Rotor Lock
1	1	Voltage Fault – VBB UVLO, VBB OVP, VCP UVLO [2]

[1] TSD with PWM = high results in rotor lock fault. Rotor lock fault has priority. To check TSD when motor running, drive PWM low to observe FF change from 10 to 01.
[2] If PWM is below DCON/DCOFF threshold, VCP UVLO fault will be masked.

Fault	Fault Action	Latched	Reset Method
VBB Undervoltage	Disable Outputs [1]	N	Restart attempted when VBB in valid range
TSD	Disable Outputs, start TLOCK timer	N	Motor restart after TLOCK Timeout
VCP Undervoltage	Disable Outputs	N	Restart attempted when VCP in valid range
VBB Overvoltage	Disable Outputs	N	Restart attempted when VBB in valid range
VDS Fault (OCP)	Disable Outputs	Y	Latch reset by PWM OFF→ON transition
Loss of Sync	Disable Outputs, start TLOCK timer	N	Motor Restart after TLOCK Timeout

[1] Output disable based on VBB UVLO can be masked by EEPROM bit UVMASK. In this case, the outputs will be protected by the charge pump UVLO function.

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TSD/Fault Flag with PWM High Timing

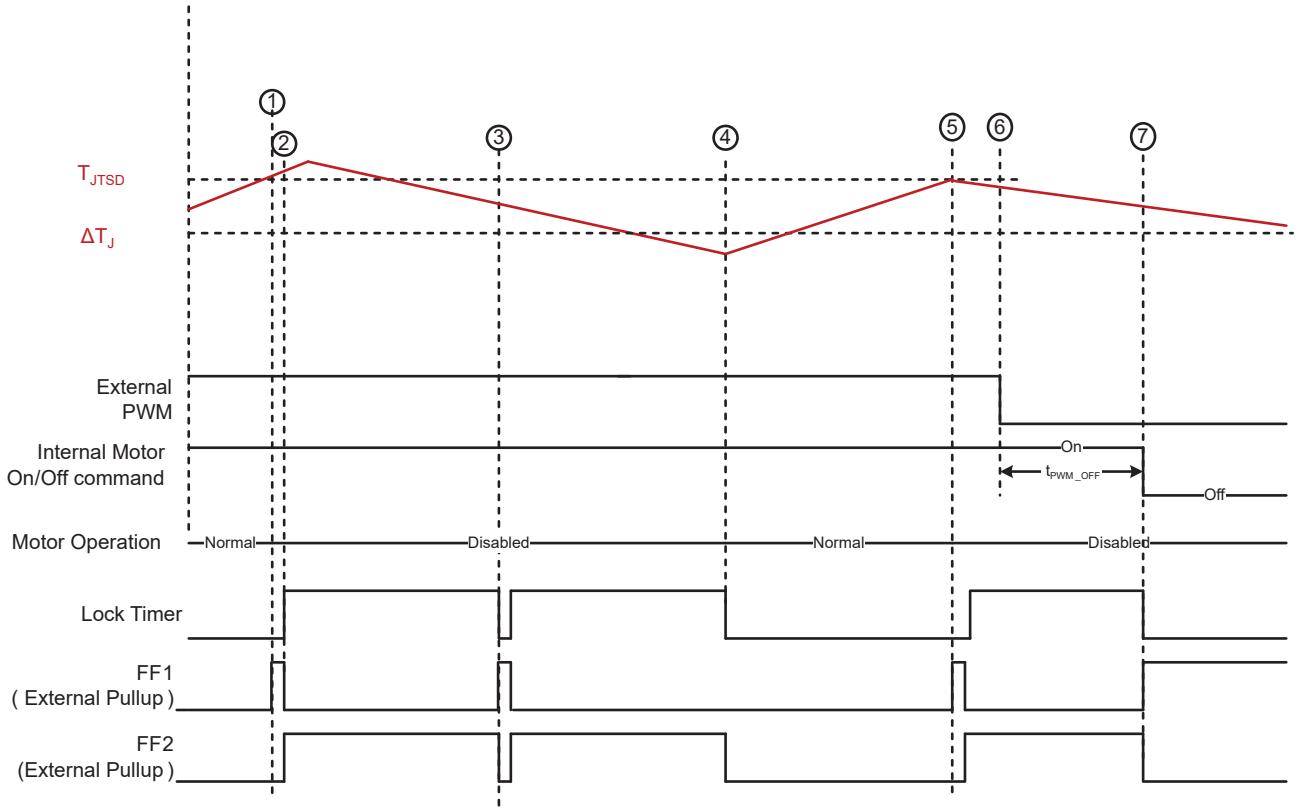

Figure 3: TSD/ Fault Flag with PWM High Timing

Description of events:

1. TSD threshold exceeded, short pulse on FF1, FF = 01
2. TSD triggers lock detect timer, FF = 10.
3. At end of lock timer. Since TSD condition still exists, Lock timer triggered again, FF = 10.
4. At end of lock timer, TSD is OK, normal motor operation can resume, FF = 00.
5. TSD threshold exceeded, short pulse on FF1, FF = 01, shortly followed by FF = 10.
6. Upon detection of FF = 10, controller wants to determine fault caused by motor lead fault or TSD. Method is to drive PWM low
7. Short delay (t_{PWM_OFF}) – before internal on/off signal changes state. This signal resets lock timer (will not reset OCP fault). FF changes to 01.

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Power On / Power Off Timing

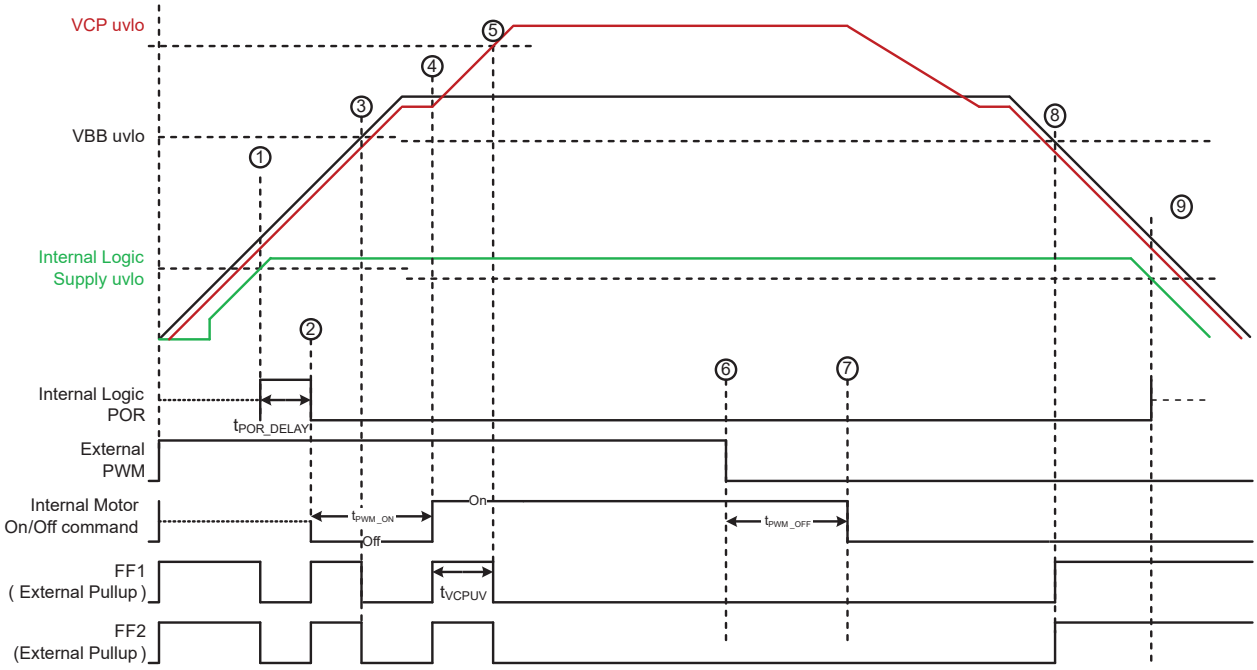

Figure 4: Power On / Power Off Timing, PWM high on power up, low on power down

Conditions: PWM high on power up, low on power down.

Description of events:

1. POR delay signal (t_{POR_DELAY}) triggered by UV signal on internal 3p3 power supply. Fault signals driven low during this delay.
2. At end of delay, logic is valid. FF = 11, voltage fault due to V_{BB} below undervoltage level. At this point, logic circuit is running PWM signal is checked.
3. FF = 00 voltage fault is released as V_{BB} rises over V_{BBUVLO}.
4. PWM logic high is detected after t_{PWM_ON}. Charge pump is enabled. FF = 11 while VCP is below UVLO level. The time for VCP to rise over its UVLO level is t_{VCPUV}.
5. V_{CP} rises over UVLO level and motor outputs turn on, FF back to 00.
6. PWM off starts t_{PWM_OFF} timer.
7. PWM recognized low to turn off motor and charge pump. Fault flag does not check V_{CP} UV when PWM = low.
8. Power down UV fault, FF = 11, when V_{BB} falls below ($V_{BBUVLO} - V_{BBHYS}$).
9. Internal logic reset when below internal V_{3p3} UVLO. This occurs when V_{BB} is approximately 3.6 V.

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Power On / Power Off Timing (continued)

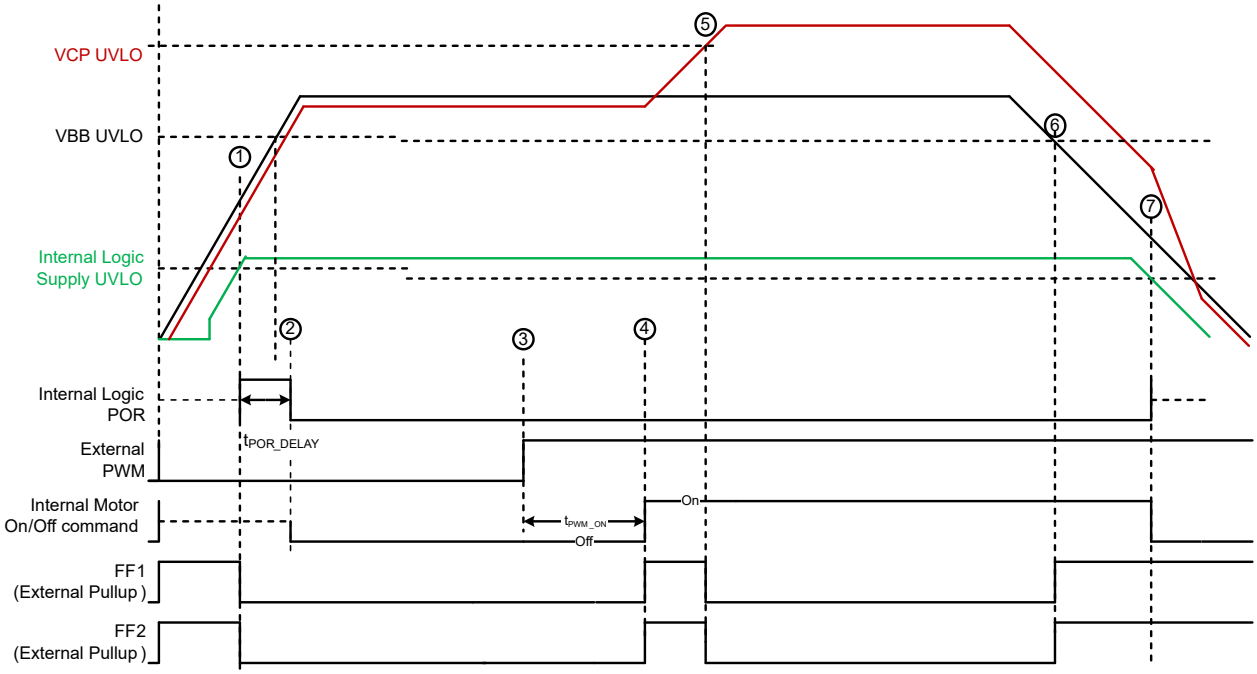

Figure 5: Power On / Power Off Timing, PWM low on power up, high on power down, V_{BB} dv/dt < 80 µs

Conditions: PWM low on power up, high on power down, V_{BB} dv/dt <80 µs.

Description of events:

1. POR delay signal (t_{POR_DELAY}) triggered by UV signal on internal 3p3 power supply. Fault signals driven low during this delay.
2. At end of delay, logic is valid. Fault flag = 00, due to V_{BB} above undervoltage level.
3. PWM ON starts t_{PWM_ON} timer.
4. PWM recognized High to Turn On motor and Charge pump. Fault flag checks VCP UV and pulse high for charge pump power up time. The time for V_{CP} to rise over its UVLO level is t_{VCPUV}.
5. FF = 00 after V_{CPUVLO} is exceeded.
6. Power down UV fault, FF = 11, when V_{BB} falls below ($V_{BBUVLO} - V_{BBHYS}$)
7. Internal logic reset when below internal V_{3p3} UVLO. This occurs when V_{BB} is approximately 3.6 V.

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Startup Sequence

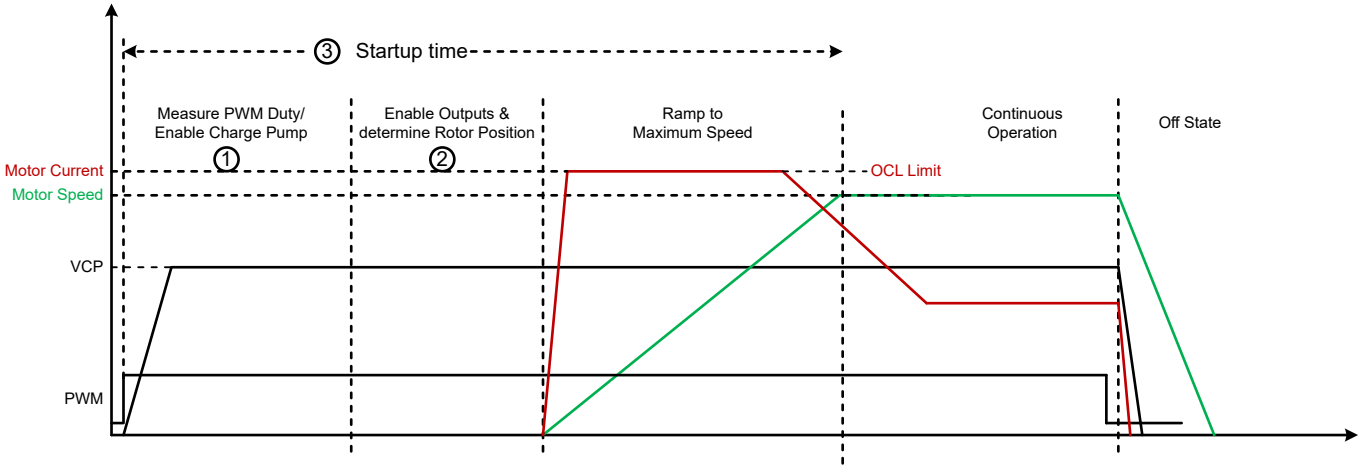

Figure 6: Startup Sequence

PWM Control

Motor will be disabled if PWM duty below DCON threshold of 10%. There is 2.6% hysteresis to DCOFF threshold of 7.4%.

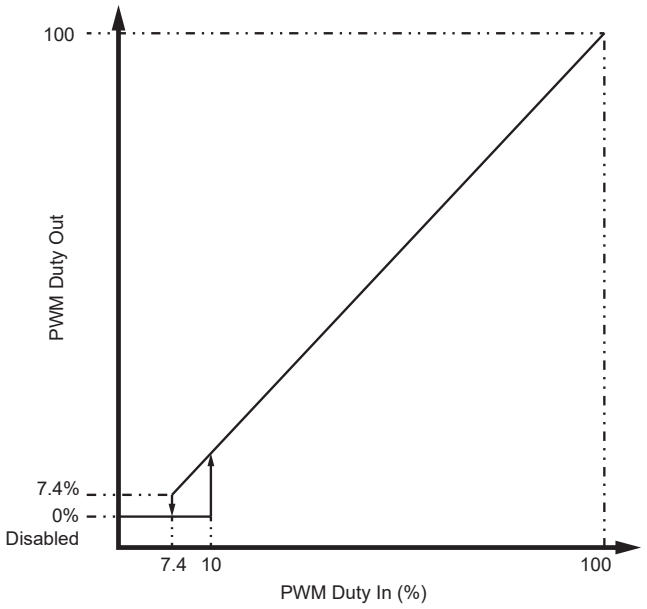

Figure 7: PWM Control

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EEPROM MAP

Table 1: EEPROM Map. Refer to application note and user interface for additional detail.

I2C Register	EE Address	Bits	Name	Description	Default Setting
64	0	15:0	Dev1	Allegro Reserved	n/a
65	1	15:0	Dev1	Allegro Reserved	n/a
66	2	15:0	Dev1	Allegro Reserved	n/a
67	3	15:0	Dev1	Allegro Reserved	n/a
68	4	15:0	Dev1	Allegro Reserved	n/a
69	5	15:0	Dev1	Allegro Reserved	n/a
70	6	15:0	Dev1	Allegro Reserved	n/a
71	7	15:0	Trim1	Allegro Reserved	n/a
72	8	15:0	Trim2	Allegro Reserved	n/a
73	9	0	UVMASK	0 = Normal 1 = Mask	0x005C
		1	OVPDIS	0 = Normal, 1 = Disable	
		2	RETRY	0 = Disable, 1 = Enable	
		3	OVERLAP	0 = Disable, 1 = Enable	
		4	Dev2	Allegro Reserved – Set to 1	
		6:5	Dev2	Allegro Reserved – Set to 10	
74	10	0	DIR	0 = ACB, 1 = ABC	0x480C
		1	FGSTRT	0 = Disable 1 = Enable	
		4:2	BEMFILT	Select Bemf Filter	
		6:5	BEMFHYS	Select Bemf Hysteresis	
		7	WIND	0 = Disable, 1 = Enable	
		8	IPDENB	0 = Disable, 1 = Enable	
		9	IPDDECAY	0 = SLOW, 1 = FAST	
		10	Dev2	Allegro Reserved – Set to 0	
		13:11	STEPS	Select trap states before BEMF detection	
		14	OCL	0 = PWM cycle, 1 = Fixed off-time	
		15	ALIGNOCL	0 = OCL level, 1 = IPDINI step	
75	11	5:0	ALIGN	Align Time	0x0001
76	12	5:0	LOCK	Lock Time	0x002A
77	13	1:0	TOFF	Fixed Off time Current Limit	0cFC4B
		7:2	OSC	Startup Osc	
		9:8	Unused	n/a	
		15:10	COMST	Com State Stall Limit	
78	14	4:0	IPDINI	IPD Start Level	0x148D
		7:5	IPDSTEP	Select IPD steps	
		12:8	OCL	Select Current Limit	
79	15	15:0	Trim2	Allegro Reserved	n/a

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Serial Port

The A89303 uses standard fast mode I²C serial port format to program the EEPROM or to control the IC speed serially. The PWM pin functions as the clock (SCL) input, and the FG pin is the data line (SDA). No special sequence is needed to begin transferring data. If the motor is running, the FG may then pull the data line low while trying to initialize into serial port mode. Once an I²C command is sent, the PWM input is ignored, and the motor will turn off as if a PWM duty command of 0% was sent.

The A89303 7-bit slave address is 0x55.

I²C Timing Diagrams

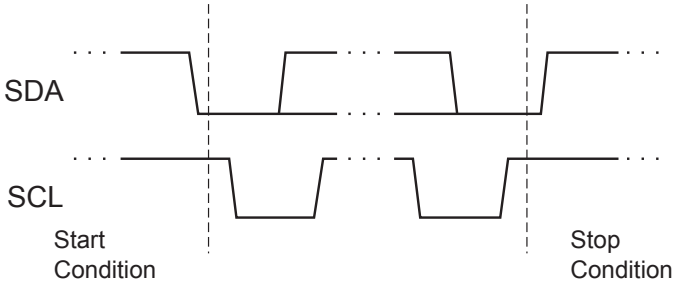

Figure 8: Start and Stop Conditions

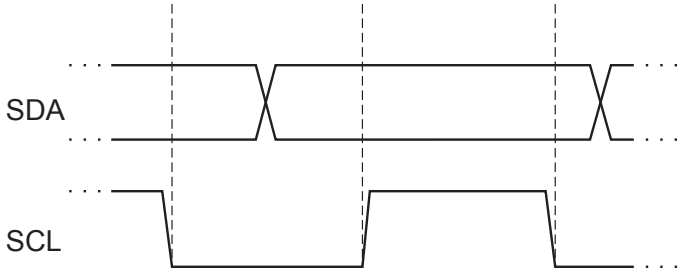

Figure 9: Clock and Data Bit Synchronization

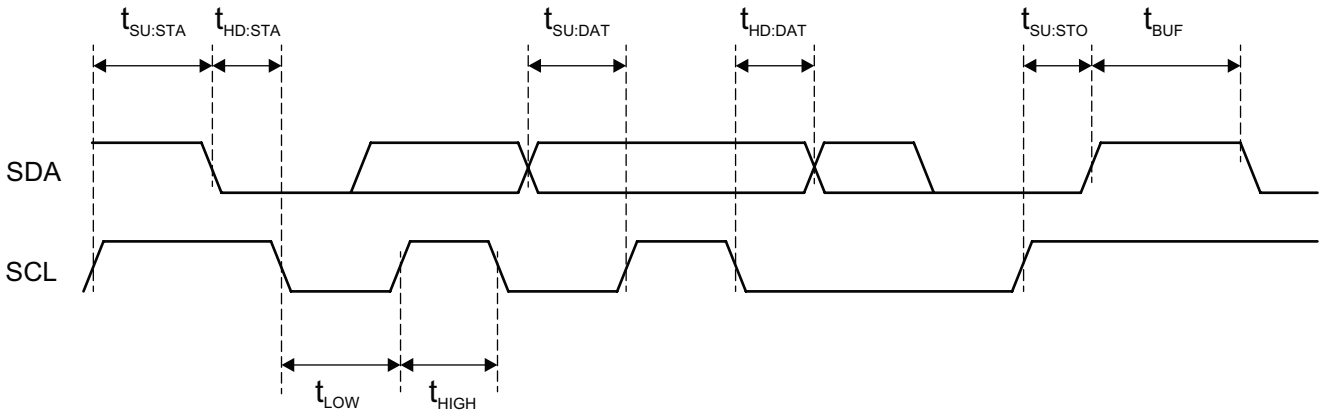

Figure 10: I²C-Compatible Timing Requirements

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Write Command

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address
4. 2 data bytes, MSB first
5. Stop Condition

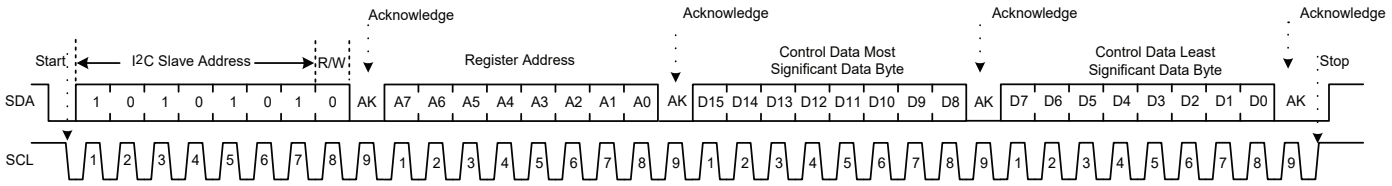

Figure 11: Write Command

Read Command: Two Step Process

1. Start Condition
2. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 0
3. Internal Register Address to be read
4. Stop Condition
5. Start Condition
6. 7-bit I²C Slave Address (Device ID) 1010101, R/W Bit = 1
7. Read 2 data bytes
8. Stop Condition

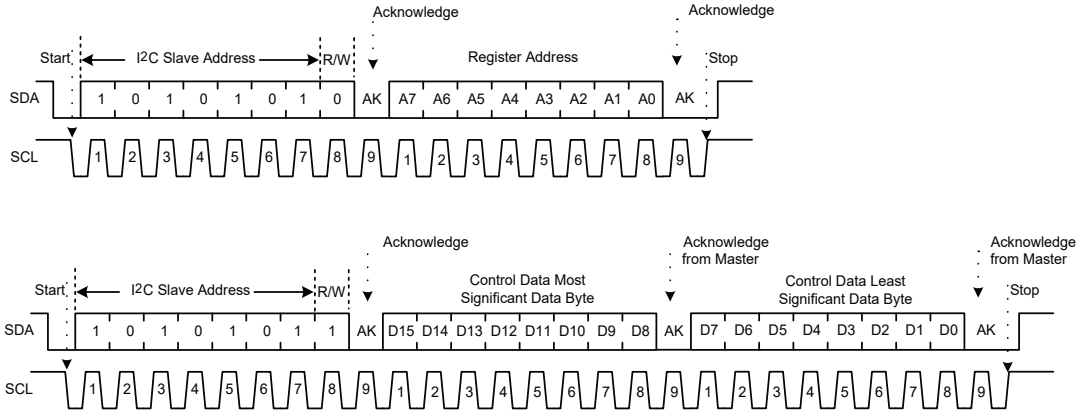

Figure 12: Read Command

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Programming EEPROM

The A89303 contains 16 words of 16-bit length. The EEPROM is controlled with the following I²C registers. Refer to application note for EEPROM definition.

Table 2: EEPROM Control – Register 161 (Used to control programming of EEPROM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM voltage required for writing or erasing
1	ER	Sets mode to erase
2	WR	Sets mode to write
3	RD	Sets mode to read
15:4	n/a	Do not use; always set to zero during programming process

Table 3: EEPROM Address – Register 162 (Used to set the EEPROM address to be altered)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
4:0	eeADDRESS	Used to specify EEPROM address to be changed; there are 16 addresses
15:5	n/a	Do not use; always set to zero during programming process

Table 4: EEPROM DataIn – Register 163 (Used to set the EEPROM new data to be programmed)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed

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Table 5: DataOUT – Register 164 (Used for read operations)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
eeDATAout															

Bit	Name	Description
15:0	eeDATAout	Used to readback EEPROM data from address defined in register 162

There are 3 basic commands: Read, Erase, and Write. To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes 12 ms per word.

Each word must be written individually.

Example #1: Write EEPROM address 9 to 261 (0x0105)

1) Erase the word

	I²C Write REGADDR[Data]	; comment
a.	162[9]	; set EEPROM address to erase
b.	163[0]	; set 0000 as Data In
c.	161[3]	; set control to Erase and Voltage High
d.	Wait 12 ms	; required 12 ms High Voltage Pulse to Write

2) Write the new data

a.	162[9]	; set EEPROM address to write
b.	163[261]	; set Data In = 261
c.	161[5]	; set control to Write and Set Voltage High
d.	Wait 12 ms	; required 12 ms High Voltage Pulse to Write

Example #2: Read EEPROM address 9 to confirm correct data properly programmed

1) Read the word

a.	9[I²C Read]	; read register 9; this will be the contents of EEPROM

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APPLICATION INFORMATION

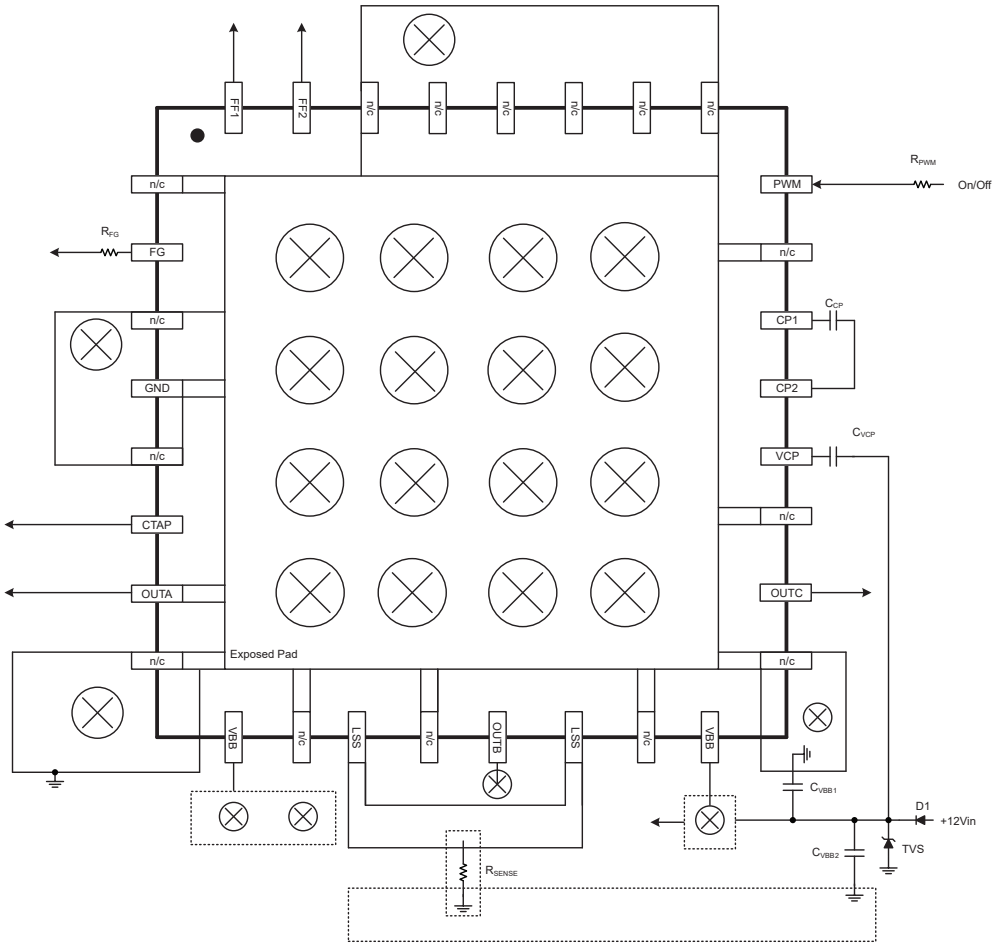

Figure 13: Typical Application Circuit

Table 6: Typical Application Components

Name	Suggested Value	Comment
C_{VBB1}	0.22 µF	Ceramic capacitor required
C_{VBB2}	22 to 220 µF	Power supply stabilization – electrolytic or ceramic OK.
C_{VCP}	0.22 µF	Ceramic capacitor required
C_{CP}	0.22 µF	Ceramic capacitor required
D1	B24013F	Required to isolate motor for reverse polarity protection
TVS	SMBJ33A	TVS to limit max V_{BB} due to transients due to motor generation on power line
R_{FG}, R_{PWM}	500 Ω	Isolate IC pin from noise or overvoltage transients or protect from connector issues
R_{SENSE}	100 mΩ	Resistor for current sensing

Layout Notes:
1. Add thermal vias to exposed pad area.
2. Add ground plane on top and bottom of PCB.
3. Place C_{VBB1} as close as possible to IC, connected to GND plane.

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PIN DIAGRAMS

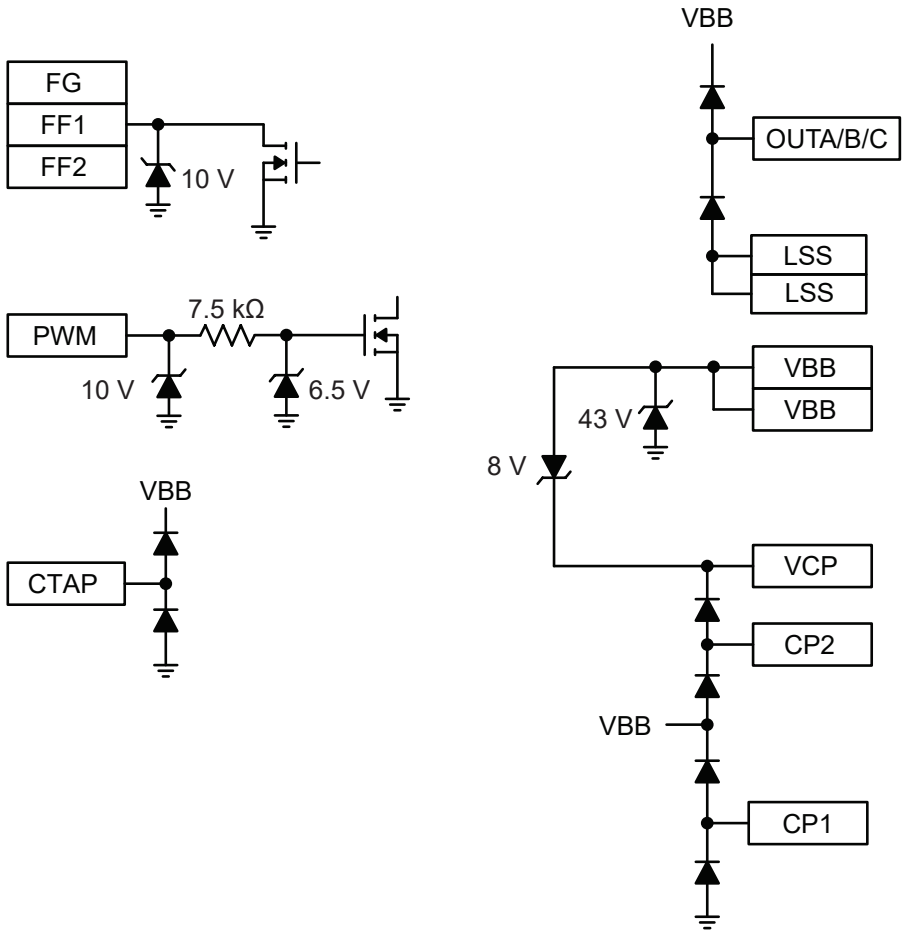

Figure 14: Pin Diagrams

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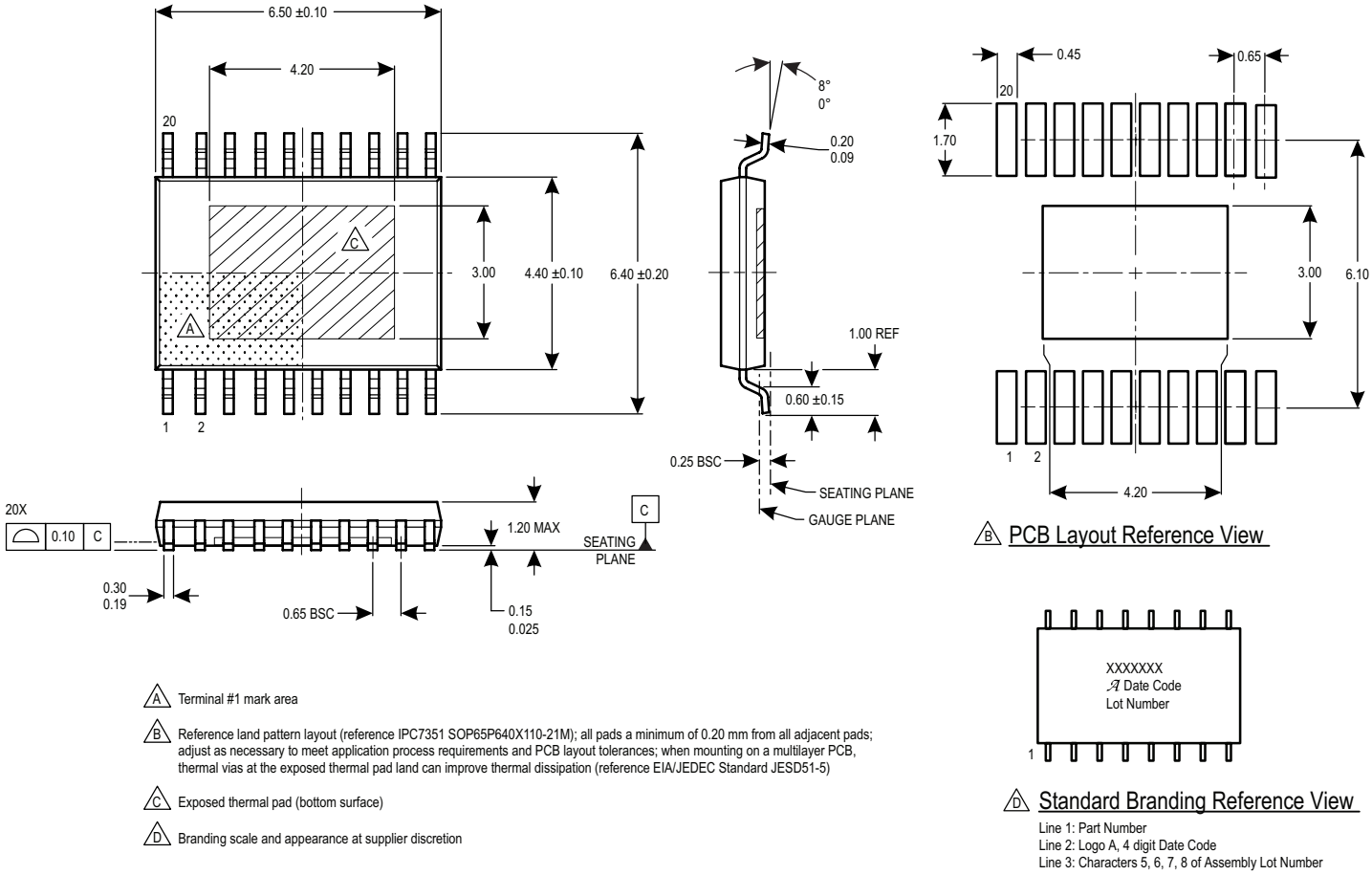
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

Figure 15: Package LP, 20-Lead TSSOP with Exposed Pad

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For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

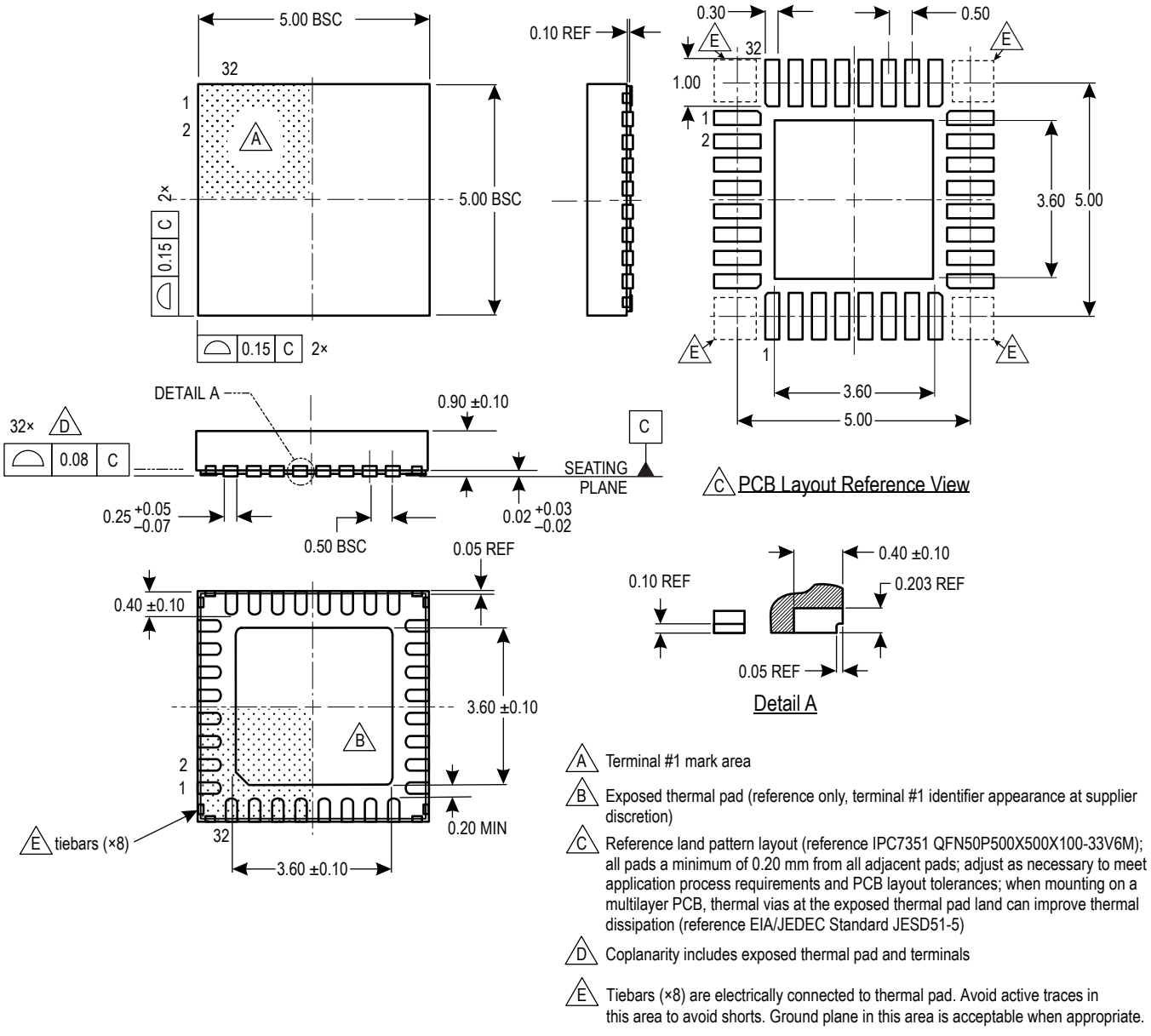

Figure 16: Package ET, 32-Contact QFN with Exposed Pad and Wettable Flank

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Revision History

Number	Date	Description
–	August 27, 2020	Initial release
1	March 10, 2021	Updated product title, typical application (page 1), Logic Input Voltage Range, Logic Output (page 2); added EEPROM Cycles (page 2); corrected CP1 and CP2 pin order in LP pinout diagram (page 3); updated Duty Cycle Off Threshold (page 4), Setup Time for Stop Condition (page 5), DataOUT EEPROM section (page 17), and other minor editorial updates.
2	November 5, 2021	Updated EEPROM map (page 13) and ET-32 package drawing (page 21); corrected typos on pages 16 and 17
3	September 16, 2022	Updated EEPROM map (page 13, I2C Register 73, Bit 1 Description), Table 6 (page 18), and LP-20 package drawing (page 20)

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