

January 1997

**NOT RECOMMENDED
FOR NEW DESIGNS**
 Use CMOS Technology

CD74FCT564, CD74FCT574

**BiCMOS FCT Interface Logic,
Octal D-Type Flip-Flops, Three-State**

Features

- Buffered Inputs
- Typical Propagation Delay: 5.6ns at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Positive Edge Triggered
- CD74FCT564
 - Inverting
- CD74FCT574
 - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT564 and CD74FCT574 are octal D-Type, three-state, positive edge triggered flip-flops which use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC} . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the three state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The CD74FCT564 and CD74FCT574 share the same configurations; the CD74FCT564, however, has inverted outputs and the CD74FCT574 has noninverted outputs.

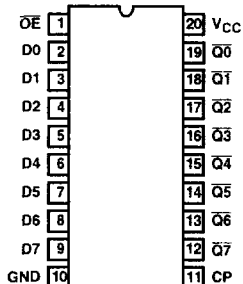
Ordering Information

PART NUMBER	TEMP. RANGE ($^\circ C$)	PACKAGE	PKG. NO.
CD74FCT564E	0 to 70	20 Ld PDIP	E20.3
CD74FCT574E	0 to 70	20 Ld PDIP	E20.3
CD74FCT564M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574SM	0 to 70	20 Ld SSOP	M20.209

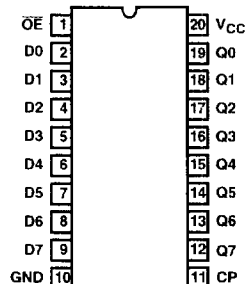
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT564
(PDIP, SOIC, SSOP)
TOP VIEW

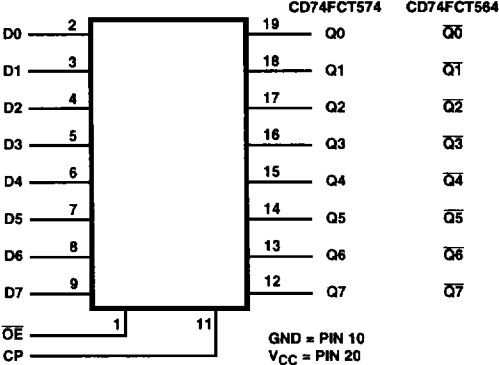


CD74FCT574
(PDIP, SOIC, SSOP)
TOP VIEW



CD74FCT564, CD74FCT574

Functional Diagram



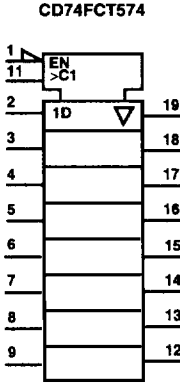
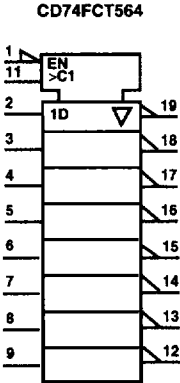
TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS	
			CD74FCT564	CD74FCT574
OE	CP	DN	QN	QN
L	↑	H	L	H
L	↑	L	H	L
L	L	X	Qo	Qo
H	X	X	Z	Z

NOTE:

- 1. H = High Level (Steady State)
- L = Low Level (Steady State)
- X = Don't Care
- ↑ = Transition from low to high level
- Qo = The level of Q before the indicated steady state input conditions were established.
- Z = HIGH Impedance

IEC Logic Symbols



CD74FCT564, CD74FCT574

Absolute Maximum Ratings

DC Supply Voltage (V_{CC})	-0.5V to 6V
DC Diode Current, I_{IK} (For $V_I < -0.5V$)	-20mA
DC Output Diode Current, I_{OK} (for $V_O < -0.5V$)	-50mA
DC Output Sink Current per Output Pin, I_O	70mA
DC Output Source Current per Output Pin, I_O	-30mA
DC V_{CC} Current (I_{CC})	140mA
DC Ground Current (I_{GND})	400mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	135
SOIC Package	125
SSOP Package	130
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$ (SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, V_{CC}	4.75V to 5.25V
DC Input Voltage, V_I	0 to V_{CC}
DC Output Voltage, V_O	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dV/dt	0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A)				UNITS
					25°C		0°C TO 70°C		
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V _{IH}			4.5 to 5.5	2	-	2	-	V
Low Level Input Voltage	V _{IL}			4.5 to 5.5	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I _{IH}	V _{CC}		Max	-	0.1	-	1	μA
Low Level Input Current	I _{IL}	GND		Max	-	-0.1	-	-1	μA
Three-State Leakage Current	I _{OZH}	V _{CC}		Max	-	0.5	-	10	μA
	I _{OZL}	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I _{OS}	V _{CC} = 0 V _{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI _{CC}	3.4V (Note 4)		MAX	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at V_{CC} or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70 $^{\circ}C$.

CD74FCT564, CD74FCT574

Switching Specifications Over Operating Range $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L - See Figure 4

PARAMETER	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A)			UNITS
			25°C	0°C TO 70°C		
			TYP	MIN	MAX	
Propagation Delays						
Clock to Q CD74FCT574	t _{PLH} , t _{PHL}	5	6.6	2	10	ns
Clock to $\overline{Q}$ CD74FCT564	t _{PLH} , t _{PHL}	5	6.6	1.5	10	ns
Output Disable to Q CD74FCT574	t _{PLZ} , t _{PHZ}	5	6	1.5	8	ns
Output Enable to Q CD74FCT574	t _{PZL} , t _{PZH}	5	9	1.5	12.5	ns
Output Disable to $\overline{Q}$ CD74FCT564	t _{PLZ} , t _{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$ CD74FCT564	t _{PZL} , t _{PZH}	5	9	1.5	12.5	ns
Power Dissipation Capacitance	C _{PD} (Note 6)	-	34 Typical			pF
Minimum (Valley) V _{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} (Figure 1)	5	0.5	-	-	V
Maximum (Peak) V _{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance	C _I	-	-	-	10	pF
Three State Output Capacitance	C _O	-	-	-	15	pF

NOTE:

- C_{PD} , measured per flip-flop, is used to determine the dynamic power consumption.
 PD (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 \text{ to } C_L + V_{CC} \Delta I_{CC} D)$ where:
 V_{CC} = supply voltage
 ΔI_{CC} = flow through current x unit load
 C_L = output load capacitance
 D = duty cycle of input high
 f_O = output frequency
 f_I = input frequency

Prerequisite For Switching

PARAMETER	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A)			UNITS
			25°C	0°C TO 70°C		
			TYP	MIN	MAX	
Clock Pulse Width CD74FCT574	t _W	5 (Note 7)		7	-	ns
CD74FCT564	t _W	5		7	-	ns
Setup Time Data to Clock	t _{SU}	5		2	-	ns
Data to Clock Hold Time						
CD74FCT574	t _H	5		2	-	ns
CD74FCT564	t _H	5		2	-	ns
Maximum Clock Frequency	f _{MAX}	5		70	-	MHz

NOTE:

- 5V: minimum is at 4.5V.
5V: minimum is at 4.75V for 0°C to 70°C.
Typical is at 5V.