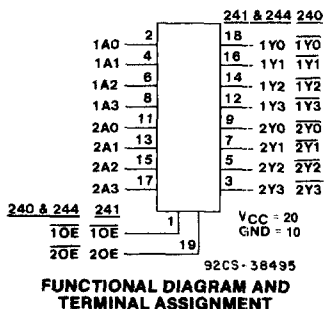


CD54/74HC240/241/244

CD54/74HCT240/241/244

File Number 1656

High-Speed CMOS Logic



Octal Buffer/Line Drivers, 3-State

CD54/74HC/HCT240 Inverting
CD54/74HC/HCT241 Non-Inverting
CD54/74HC/HCT244 Non-Inverting

Type Features:

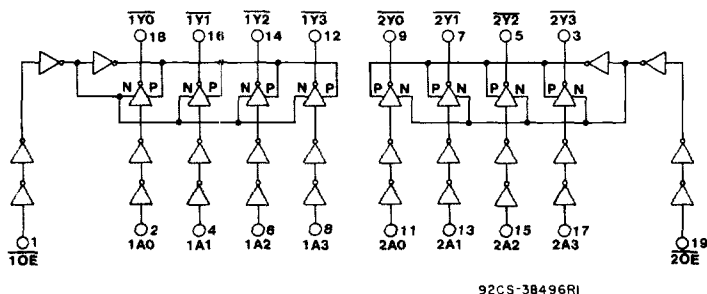
- Typical propagation delay = 8 ns
@ $V_{CC}=5$ V, $C_L=15$ pF, $T_A=25^\circ$ C for HC240
- 3-State outputs
- Buffered inputs
- High-current bus driver outputs

The RCA-CD54/74HC240 and CD54/74HCT240 are inverting 3-state buffers having two active-low output enables. The RCA CD54/74HC/HCT241 and CD54/74HC/HCT244 are non-inverting 3-state buffers that differ only in that the 241 has one active-high and one active-low output enable, and the 244 has two active-low output enables. All three types have identical pinouts.

The CD54HC240/241/244 and CD54HCT240/241/244 are supplied in 20-lead ceramic dual-in-line packages (F suffix). The CD74HC240/241/244 and CD74HCT240/241/244 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line surface mount plastic packages (M suffix). The CD54/74HC/HCT240/241/244 are also supplied in chip form: (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to $+85^\circ$ C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL}=30\%$, $N_{IH}=30\%$ of V_{CC} ; @ $V_{CC}=5$ V
- CD 54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $V_{IL}=0.8$ V Max., $V_{IH}=2$ V Min.
CMOS Input Compatibility
 $I_I \leq 1$ μ A @ V_{OL} , V_{OH}



TRUTH TABLE

INPUTS		OUTPUT
$\overline{1OE}, \overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

(HC/HCT240)

Fig. 1 - CD54/74HC/HCT240 logic diagram.

CD54/74HC240/241/244 CD54/74HCT240/241/244

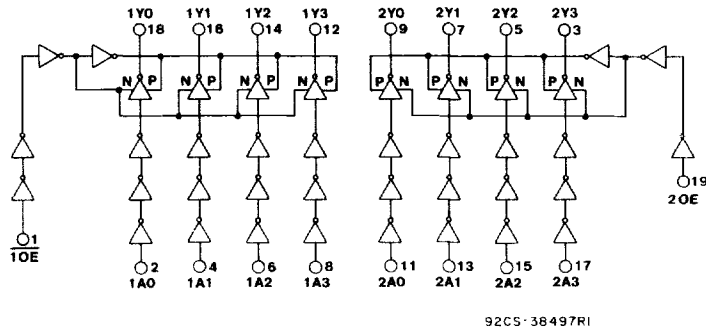


Fig. 2 - CD54/74HC/HCT241 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT	INPUTS		OUTPUT
1OE	1A	1Y	2OE	2A	2Y
L	L	L	L	X	Z
L	H	H	H	L	L
H	X	Z	H	H	H

H=HIGH Voltage Level
L=LOW Voltage Level
X=Immaterial
Z=HIGH Impedance
(HCT/HCT241)

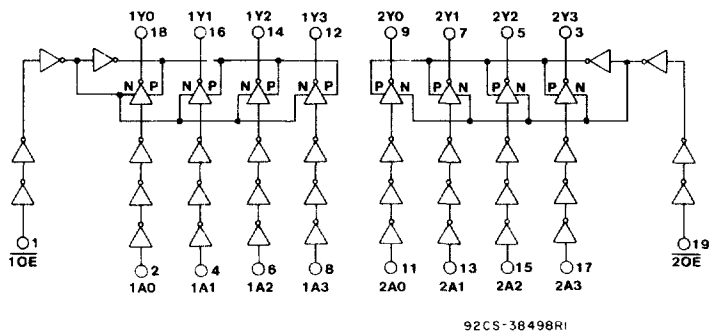


Fig. 3 - CD54/74HC/HCT244 logic diagram.

TRUTH TABLE

INPUTS		OUTPUT
1OE, 2OE	A	Y
L	L	L
L	H	H
H	X	Z

(HC/HCT244)

CD54/74HC240/241/244

CD54/74HCT240/241/244

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	-0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	± 20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} + 0.5$ V)	± 35 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC})	± 70 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE F, H)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/ $^\circ\text{C}$ to 300 mW
For $T_A = -40$ to $+70^\circ\text{C}$ (PACKAGE TYPE M)	400 mW
For $T_A = +70$ to $+125^\circ\text{C}$ (PACKAGE TYPE M)	Derate Linearly at 6 mW/ $^\circ\text{C}$ to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E, M	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm) with solder contacting lead tips only	$+300^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A =Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I , V_O	0	V_{CC}	V
Operating Temperature T_A :			$^\circ\text{C}$
CD74 Types	-40	+85	
CD54 Types	-55	+125	
Input Rise and Fall Times t_r , t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC240/241/244

CD54/74HCT240/241/244

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC240/241/244, CD54HC240/241/244											CD74HCT240/241/244, CD54HCT240/241/244											UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES					
	V _I V	I _O mA	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C		V _I V	V _{CC} V	+25° C			-40/ +85° C		-55/ +125° C					
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max				
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5									V		
			4.5	3.15	—	—	3.15	—	3.15	—		to	2	—	—	2	—	2	—				
			6	4.2	—	—	4.2	—	4.2	—		5.5											
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5									V		
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	—			
			6	—	—	1.8	—	1.8	—	1.8	—	5.5											
High-Level Output Voltage V _{OH} CMOS Loads	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL} or V _{IH}	4.5	4.4	—	—	4.4	—	4.4	—		V		
			4.5	4.4	—	—	4.4	—	4.4	—		to											
			6	5.9	—	—	5.9	—	5.9	—		5.5											
TTL Loads (Bus Driver)	V _{IL} or V _{IH}	-6 -7.8	4.5 6	3.98 5.48	— —	— —	3.84 5.34	— —	3.7 5.2	— —	V _{IL} or V _{IH}	4.5	3.98	—	—	3.84	—	3.7	—		V		
Low-Level Output Voltage V _{OL} CMOS Loads	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL} or V _{IH}	4.5	—	—	0.1	—	0.1	—	0.1	—	V		
			4.5	—	—	0.1	—	0.1	—	0.1		to											
			6	—	—	0.1	—	0.1	—	0.1		5.5											
TTL Loads (Bus Driver)	V _{IL} or V _{IH}	6 7.8	4.5 6	— —	— —	0.26 0.26	— —	0.33 0.33	— —	0.4 0.4	V _{IL} or V _{IH}	4.5	—	—	0.26	—	0.33	—	0.4	—	V		
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage between V _{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	—	μA		
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	—	μA		
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1 to 5.5	4.5 to 5.5	—	100	360	—	450	—	490	—	μA		
3-state leakage current I _{OZ}	V _{IL} or V _{IH}	V _O =V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{IH}	5.5	—	—	±0.5	—	±5	—	±10	—	μA		

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

CD54/74HC240/241/244 CD54/74HCT240/241/244

HCT Input Loading Tables

CD54/74HCT240	
Input	Unit Loads*
nA0-A3	1.5
1OE	0.7
2OE	0.7

CD54/74HCT241	
Input	Unit Loads*
nA0-A3	0.7
1OE	0.7
2OE	1.5

CD54/74HCT244	
Input	Unit Loads*
nA0-A3	0.7
1OE	0.7
2OE	0.7

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μ A max. @ 25° C.

SWITCHING CHARACTERISTICS ($V_{CC}=5$ V, $T_A=25^\circ$ C, Input t_i , $t_i=6$ ns)

CHARACTERISTIC	SYMBOL	C _L pF	Typical Values						UNITS
			240		241		244		
			HC	HCT	HC	HCT	HC	HCT	
Propagation Delay Data to Output	t _{PHL} , t _{PLH}	15	8	9	9	10	9	10	ns
Output Disable/Enable to Outputs	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	15	12	12	12	12	12	12	ns
Power Dissipation Capacitance	C _{PD} *	—	38	40	34	38	46	40	pF

C_{PD} is used to determine the dynamic power consumption per channel.

$$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$$

f_i = input frequency.

C_L = output load capacitance.

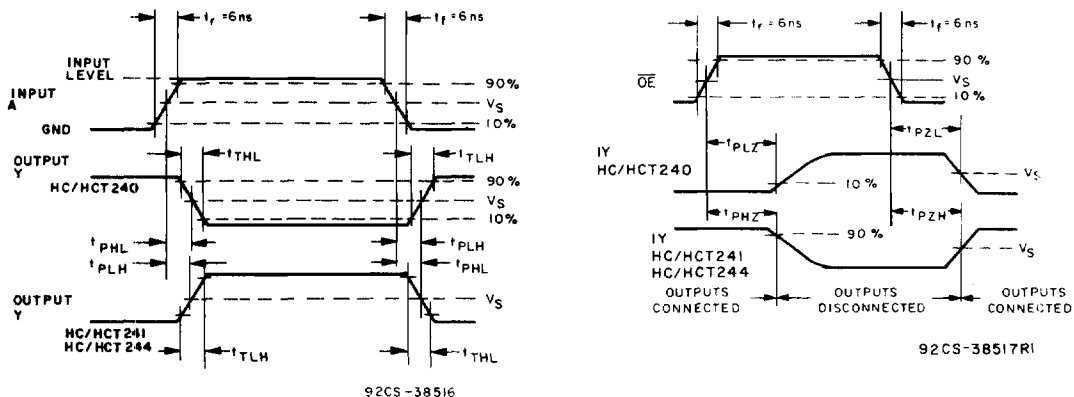
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS ($C_L=50$ pF, Input t_i , $t_i=6$ ns)

CHARACTERISTIC	SYMBOL	V _{CC}	25° C				-40° C to +85° C				-55° C to +125° C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, Data to Outputs	t _{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	—	ns
HC/HCT 240	t _{PHL}	4.5	—	20	—	22	—	25	—	28	—	30	—	33	
		6	—	17	—	—	—	21	—	—	—	26	—	—	
Data to Outputs	t _{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT241	t _{PHL}	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Data to Outputs	t _{PLH}	2	—	110	—	—	—	140	—	—	—	165	—	—	ns
HC/HCT 244	t _{PHL}	4.5	—	22	—	25	—	28	—	31	—	33	—	38	
		6	—	19	—	—	—	24	—	—	—	28	—	—	
Output Enable and Disable Times	t _{PZH}	2	—	150	—	—	—	190	—	—	—	225	—	—	ns
	t _{PZL}	4.5	—	30	—	30	—	38	—	38	—	45	—	45	
	t _{PHZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
	t _{PLZ}														
Output Transition Time	t _{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
	t _{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C _i		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C _o		—	20	—	20	—	20	—	20	—	20	—	20	pF

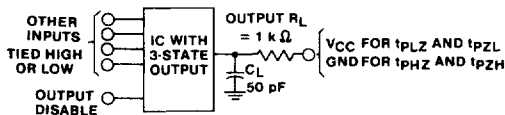
CD54/74HC240/241/244

CD54/74HCT240/241/244



	54/74HC	54/74HCT
Input Level	V _{CC}	3 V
Switching Voltage, V _S	50% V _{CC}	1.3 V

Fig. 2 - Transition times and propagation delay times.



92CS-35130R2

Fig. 4 - Three-state propagation delay test circuit.