

SN54LVTR245, SN74LVTR245 3.3-V ABT OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCAS428 – OCTOBER 1993

- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Supports Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Reduced Output Structure on A Port Minimizes V_{OHV}
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)

description

These octal bus transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVTR245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

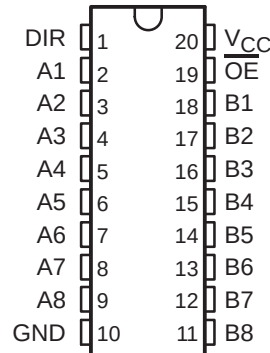
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The A port is designed to minimize the undershoot exhibited on high to low transition during simultaneous switching conditions.

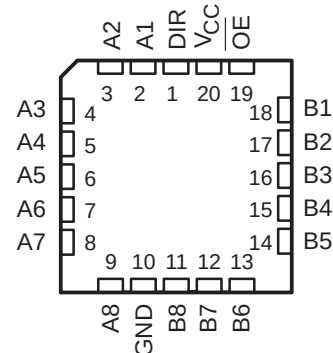
The SN74LVTR245 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVTR245 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74LVTR245 is characterized for operation from -40°C to 85°C .

SN54LVTR245 . . . J PACKAGE
SN74LVTR245 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTR245 . . . FK PACKAGE
(TOP VIEW)

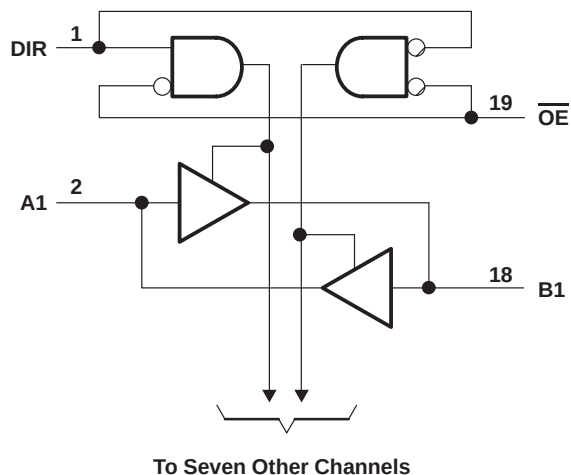
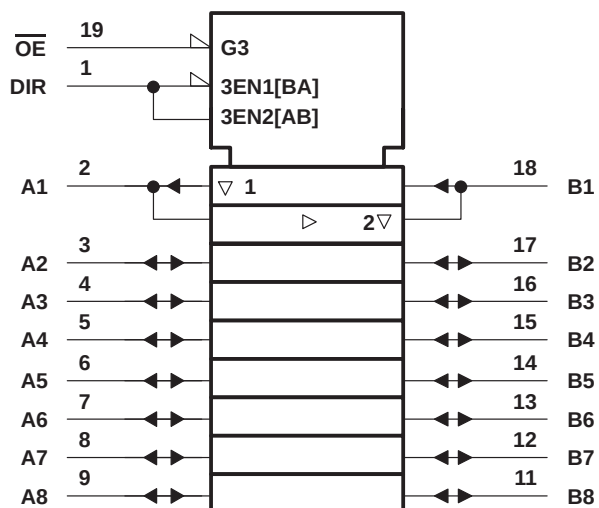


FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}		-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)		-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)		-0.5 V to 7 V
Current into any output in the low state, I_O : SN54LVTR245		96 mA
SN74LVTR245		128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTR245		48 mA
SN74LVTR245		64 mA
Input clamp current, I_{IK} ($V_I < 0$)		-50 mA
Output clamp current, I_{OK} ($V_O < 0$)		-50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): DB package		0.65 W
DW package		0.85 W
PW package		0.6 W
Storage temperature range		-65°C to 150°C

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

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recommended operating conditions

			SN54LVTR245		SN74LVTR245		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current	B port		–24		–32	mA
		A port		–8		–12	
I_{OL}	Low-level output current			24		32	mA
$I_{OL}^{\dagger}$	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

[†] Current duty cycle $\leq 50\%$, $f \geq 1$ kHz

SN54LVTR245, SN74LVTR245

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTR245		SN74LVTR245		UNIT	
			MIN	TYP†	MAX	MIN		TYP†
V _{IK}	V _{CC} = 2.7 V, I _I = −18 mA		−1.2		−1.2		V	
V _{OH}	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA		B port	V _{CC} − 0.2		V _{CC} − 0.2		V
	V _{CC} = 2.7 V, I _{OH} = − 8 mA			2.4		2.4		
	V _{CC} = 3 V	I _{OH} = − 24 mA		2				
		I _{OH} = − 32 mA				2		
	V _{CC} = MIN to MAX‡, I _{OH} = −100 μA		A port	V _{CC} − 0.2		V _{CC} − 0.2		
	V _{CC} = 2.7 V, I _{OH} = − 1 mA			2.4		2.4		
	V _{CC} = 3 V	I _{OH} = − 3 mA		2.4		2.4		
		I _{OH} = − 8 mA		2				
		I _{OH} = − 12 mA				2		
V _{OL}	V _{CC} = 2.7 V	I _{OL} = 100 μA		0.2		0.2		V
		I _{OL} = 24 mA		0.5		0.5		
	V _{CC} = 3 V	I _{OL} = 16 mA		0.4		0.4		
		I _{OL} = 32 mA		0.5		0.5		
		I _{OL} = 48 mA		0.55				
		I _{OL} = 64 mA				0.55		
I _I	V _{CC} = 3.6 V, V _I = V _{CC} or GND		Control pins	±1		±1		μA
	V _{CC} = 0 or MAX‡, V _I = 5.5 V			10		10		
	V _{CC} = 3.6 V	V _I = 5.5 V	A or B ports§	100		20		
		V _I = V _{CC}		5		5		
		V _I = 0		−5		−5		
I _I (hold)	V _{CC} = 3 V	V _I = 0.8 V	A or B ports	75		75		μA
		V _I = 2 V		−75		−75		
I _{OZH}	V _{CC} = 3.6 V, V _O = 3 V		1		1		μA	
I _{OZL}	V _{CC} = 3.6 V, V _O = 0.5 V		−1		−1		μA	
I _{CC}	V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high	0.13	0.5	0.13	0.19	mA
			Outputs low	8.8	14	8.8	12	
			Outputs disabled	0.13	0.5	0.13	0.19	
ΔI _{CC} ¶	V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.3		0.2		mA	
C _i	V _I = 3 V or 0		4		4		pF	
C _{io}	V _O = 3 V or 0		10		10		pF	

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at V_{CC} or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTR245 T _A = −55°C to 125°C				SN74LVTR245 T _A = −40°C to 85°C				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t _{PLH}	A	B	1.1	4.3	4.8		1.1	2.5	4.2	4.7		ns
	B	A	1.4	4.5	5.4		1.4	2.7	4.4	5.3		
t _{PHL}	A	B	1.1	4.7	5.9		1.1	2.6	4.6	5.8		ns
	B	A	1	4.2	5.3		1	2.3	4.1	5.1		
t _{PZH}	OE	B	1.3	5.9	7		1.3	3.1	5.5	6.7		ns
		A	1.6	6.1	8.4		1.6	3.6	6	8.3		
t _{PZL}	OE	B	2	6.7	8.1		2	3.9	6.6	8		ns
		A	1.8	6.5	7.7		1.8	3.8	6.4	7.6		
t _{PHZ}	OE	B	2.7	6.5	7		2.7	4.2	6.1	6.7		ns
		A	2.5	6.2	6.8		2.5	4	5.8	6.4		
t _{PLZ}	OE	B	2.4	5.6	5.6		2.4	3.7	5.2	5.4		ns
		A	2.4	5.5	5.6		2.4	3.7	5.2	5.3		

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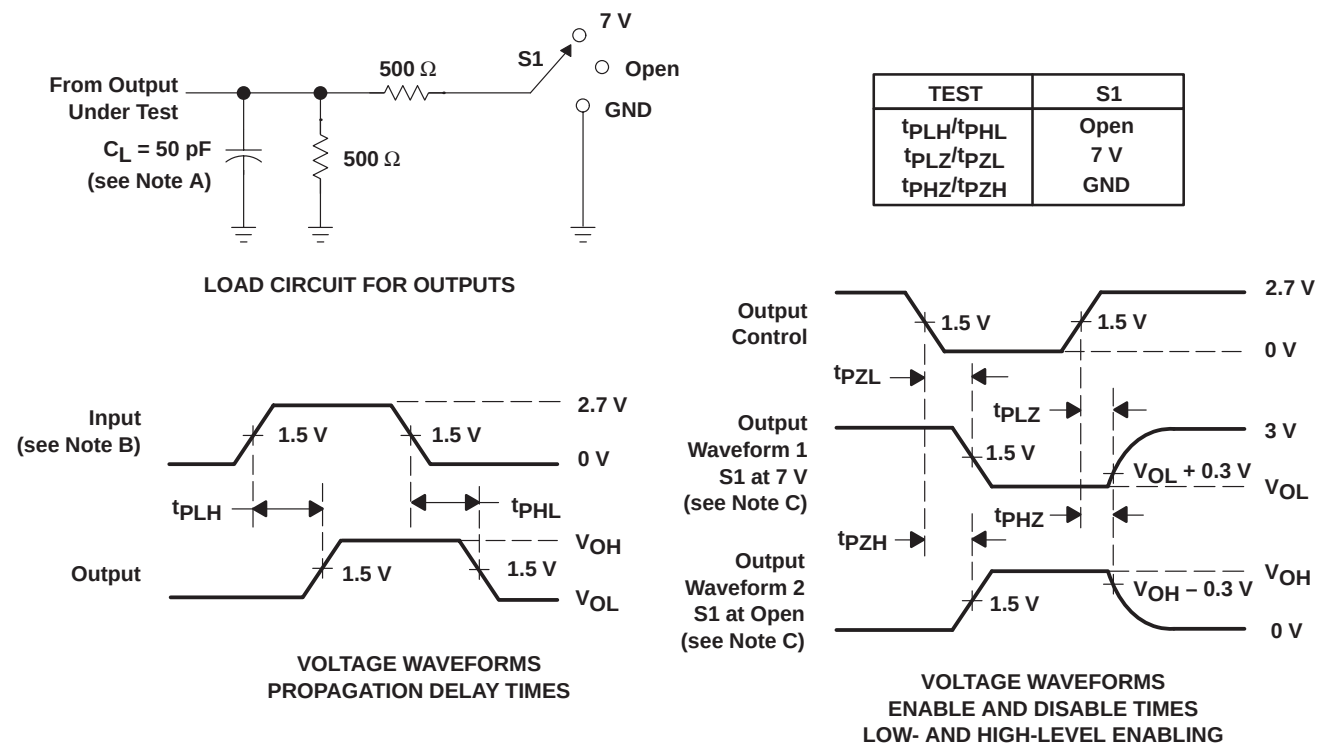
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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SN74LVTR245, 3.3-V ABT Octal Bus Transceivers With 3-State Outputs And Series Resistors

DEVICE STATUS: **ACTIVE**

FEATURES

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TECHNICAL DOCUMENTS

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DATASHEET

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Full datasheet in Acrobat PDF: [sn74lvtr245.pdf](#) (117 KB) (Updated: 10/01/1993)

APPLICATION NOTES

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- [16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA \(Rev. B\)](#) (SZZA029B - Updated: 05/22/2002)
- [Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs \(Rev. A\)](#) (SCBA012A - Updated: 08/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)

- [Implications of Slow or Floating CMOS Inputs \(Rev. C\)](#) (SCBA004C - Updated: 02/01/1998)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [LVT Family Characteristics \(Rev. A\)](#) (SCEA002A - Updated: 03/01/1998)
- [LVT-to-LVTH Conversion](#) (SCEA010 - Updated: 12/08/1998)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)
- [Logic Solutions For IEEE Std 1284](#) (SCEA013 - Updated: 06/01/1999)
- [Low Voltage Logic Families \(Rev. A\)](#) (SCVAE01A - Updated: 06/01/1998)
- [Power-Up 3-State \(PU3S\) Circuits in TI Standard Logic Devices](#) (SZZA033 - Updated: 05/10/2002)
- [Quad Flatpack No-Lead Logic Packages \(Rev. A\)](#) (SCBA017A - Updated: 09/10/2002)
- [Understanding Advanced Bus-Interface Products Design Guide](#) (SCAA029, 253 KB - Updated: 05/01/1996)

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- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Low Voltage Solutions](#) (SGYN139, 103 KB - Updated: 04/04/2001)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG							▲Back to Top			REPORTED DISTRIBUTOR INVENTORY		
DEVICE INFORMATION							TI INVENTORY STATUS			AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LVTR245NSR	ACTIVE	SOP (NS) 20	-40 TO 85	View Contents	1KU 1.54	2000	N/A*	3815 14 Oct	4 WKS			
								>10k 21 Oct				

Table Data Updated on: 9/26/2002