

DM74LS165

8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs HIGH inhibits clocking, and holding either clock input LOW with the load input HIGH enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is HIGH. Parallel loading is inhibited as long as the load input is HIGH. Data at the parallel inputs are loaded directly into the register on a HIGH-to-LOW transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

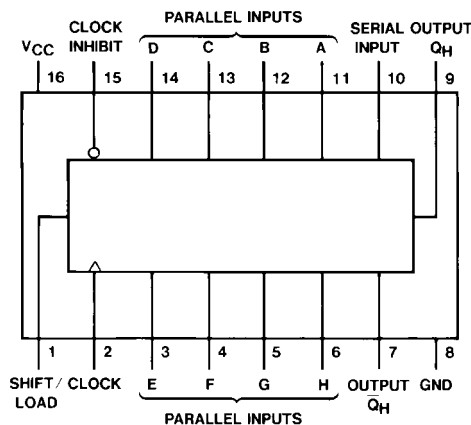
- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Ordering Code:

Order Number	Package Number	Package Description
DM74LS165M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS165WM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
DM74LS165N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Internal		Output
Shift/Load	Clock Inhibit	Clock	Serial	Parallel A...H	Outputs QA QB	
L	X	X	X	a...h	a b	h
H	L	L	X	X	QA0 QB0	QH0
H	L	↑	H	X	H QA _n	QG _n
H	L	↑	L	X	L QA _n	QG _n
H	H	X	X	X	QA0 QB0	QH0

H = HIGH Level (steady state)

L = LOW Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from LOW-to-HIGH level

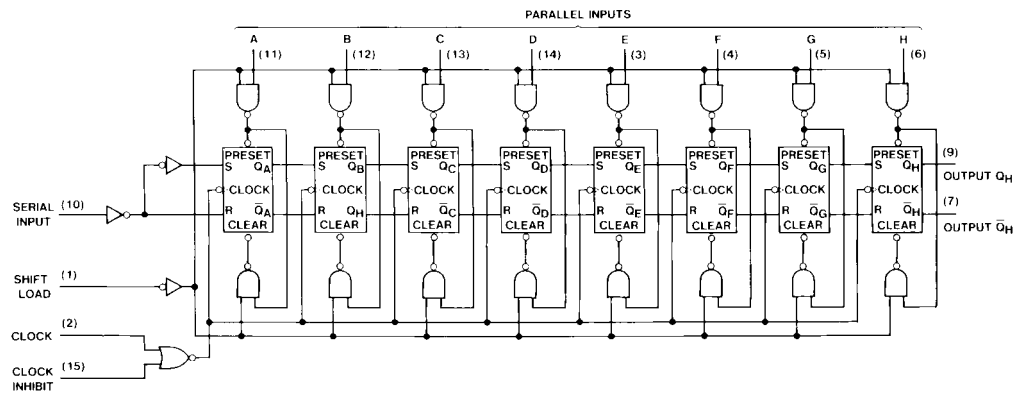
a...h = The level of steady-state input at inputs A through H, respectively.

QA0, QB0, QH0 = The level of QA, QB, or QH, respectively, before the indicated steady-state input conditions were established.

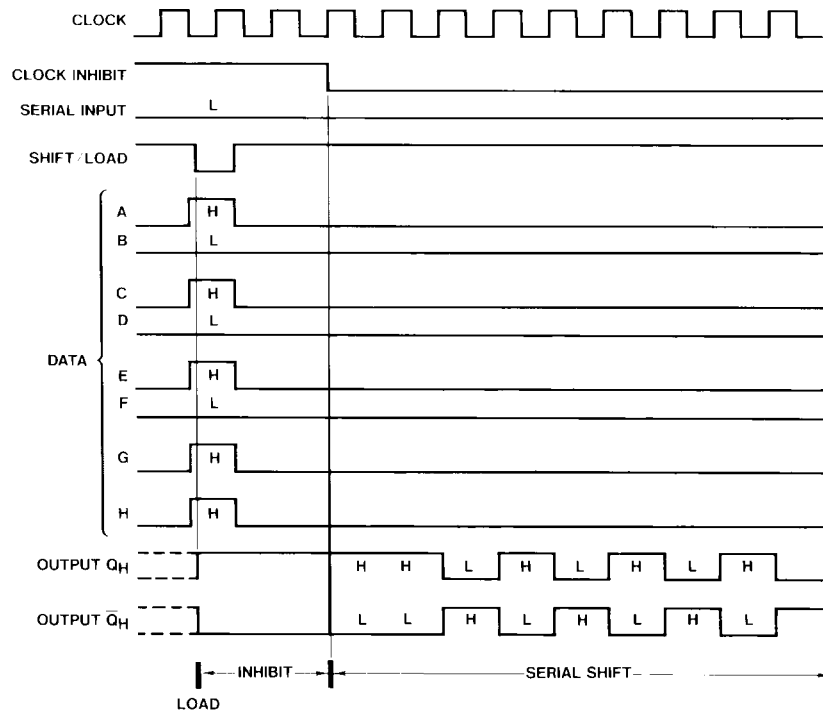
QA_n, QG_n = The level of QA or QG, respectively, before the most recent

↑ transition of the clock.

Logic Diagram



Timing Diagram



Typical Shift, Load, and Inhibit Sequences

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			-0.4	mA
I_{OL}	LOW Level Output Current			8	mA
f_{CLK}	Clock Frequency (Note 2)	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)	0		20	MHz
t_W	Pulse Width (Note 3)	Clock	25		ns
		Load	15		
t_{SU}	Setup Time (Note 4)	Parallel	10		ns
		Serial	20		
		Enable	30		
		Shift	45		
t_H	Hold Time (Note 4)	0			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 2: $C_L = 15$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V

Note 3: $C_L = 50$ pF, $R_L = 2$ k Ω , $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V

Note 4: $T_A = 25^\circ\text{C}$ and $V_{CC} = 5$ V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = \text{Min}$, $I_I = -18$ mA			-1.5	V
V_{OH}	HIGH Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OH} = \text{Max}$ $V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	$V_{CC} = \text{Min}$, $I_{OL} = \text{Max}$			0.4	V
		$V_{IL} = \text{Max}$, $V_{IH} = \text{Min}$		0.35	0.5	
		$I_{OL} = 4$ mA, $V_{CC} = \text{Min}$		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = \text{Max}$, $V_I = 7$ V	Shift/Load		0.3	mA
			Others		0.1	
I_{IH}	HIGH Level Input Current	$V_{CC} = \text{Max}$	Shift/Load		60	μA
		$V_I = 2.7$ V	Others		20	
I_{IL}	LOW Level Input Current	$V_{CC} = \text{Max}$	Shift/Load		-1.2	mA
		$V_I = 0.4$ V	Others		-0.4	
I_{OS}	Short Circuit Output Current	$V_{CC} = \text{Max}$ (Note 6)		-20	-100	mA
I_{CC}	Supply Current	$V_{CC} = \text{Max}$ (Note 7)		21	36	mA

Note 5: All typicals are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

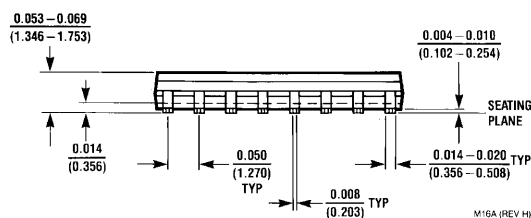
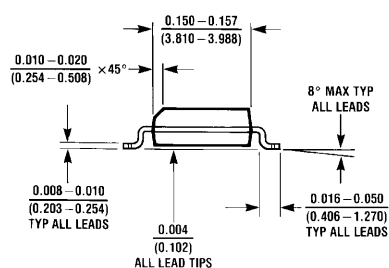
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs OPEN, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25^\circ C$

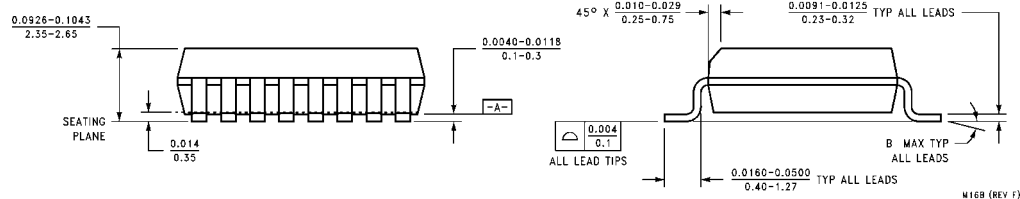
Symbol	Parameter	From (Input) To (Output)	$C_L = 15\text{ pF}$		$R_L = 2\text{ k}\Omega, C_L = 50\text{ pF}$		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Load to Any Q		35		37	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Load to Any Q		35		42	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Any Q		40		42	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Any Q		40		47	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	H to Q_H		25		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	H to Q_H		30		37	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	H to $\overline{Q}_H$		30		32	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	H to $\overline{Q}_H$		25		32	ns



Technical drawing of a 16-pin D-subminiature connector. The drawing shows the top and side views. The top view shows 16 pins numbered 1 to 16. The side view shows the connector's profile with dimensions. Key dimensions include:

- Pin 1 to Pin 16 pitch: 0.3977-0.4133 (10.10-10.50)
- Pin 1 to Pin 16 width: 0.2914-0.2992 (7.4-7.6)
- Pin 1 to Pin 16 height: 0.3940-0.4190 (10.00-10.65)
- Pin 1 to Pin 16 depth: 0.050 (1.27)
- Pin 1 to Pin 16 thickness: 0.118-0.0200 (0.350-0.508)

The drawing also shows a lead identification feature and a pin 1 identification feature.



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