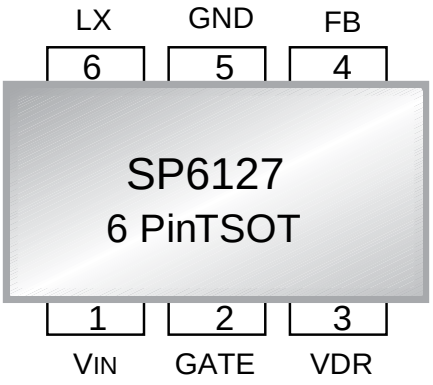
High-Voltage, Step-Down Controller in TSOT6

FEATURES

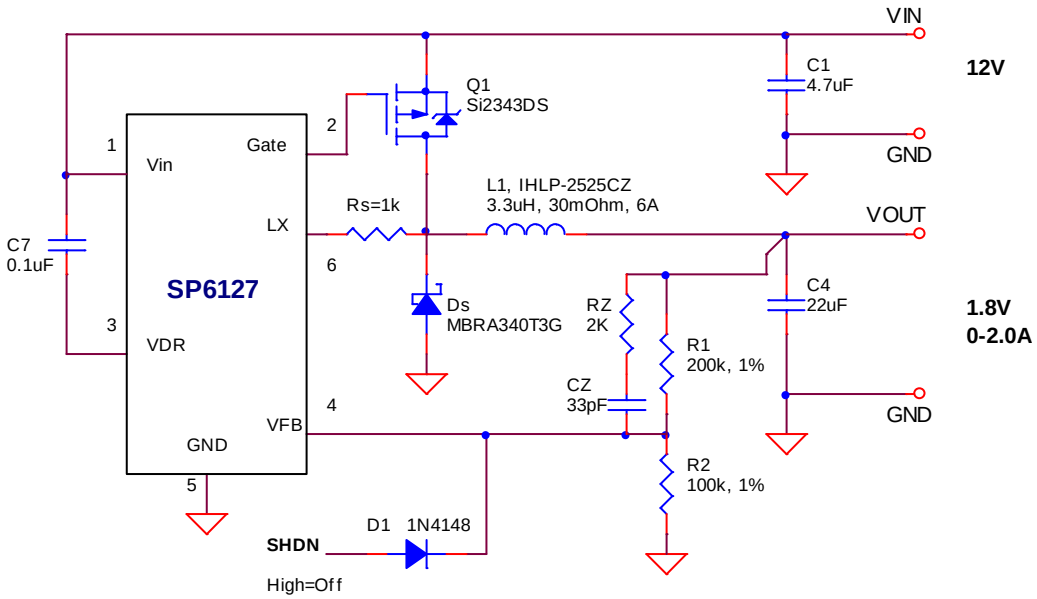
- Wide 4.5V – 29V Input Voltage Range
- Internal compensation
- Built-in High-Current PMOS Driver
- Adjustable Overcurrent Protection
- Internal soft start
- 900kHz Constant Frequency Operation
- 0.6V Reference Voltage
- 1% output setpoint accuracy
- Lead Free, RoHS Compliant Package: Small 6-pin TSOT



DESCRIPTION

The SP6127 is a PWM controlled step down (buck) voltage mode regulator with VIN feedforward and internal Type-II compensation. It operates from 4.5V to 29V VIN, making it suitable for 5V, 12V and 24V applications. By using a PMOS driver, this device is capable of operating at 100% duty cycle. The high-side driver is designed to drive the gate 5V below VIN. The programmable overcurrent protection is based on the high-side MOSFET's ON resistance sensing and allows setting the overcurrent protection value up to 300mV threshold (measured between VIN-LX). The SP6127 is available in a space-saving 6-pin TSOT package making it the smallest controller available capable of operating from 24VDC supplies.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only, and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage…..-0.3V to 30V
Lx……-2V to 30V
FB…….-0.3V to 5.5V
Storage Temperature..……..…….-65 °C to 150 °C
Junction Temperature.....-40°C to 125°C
Lead Temperature (Soldering, 10 sec)…..……..300 °C
ESD Rating…….……1kV LX, 2kV all other nodes, HBM

ELECTRICAL SPECIFICATIONS

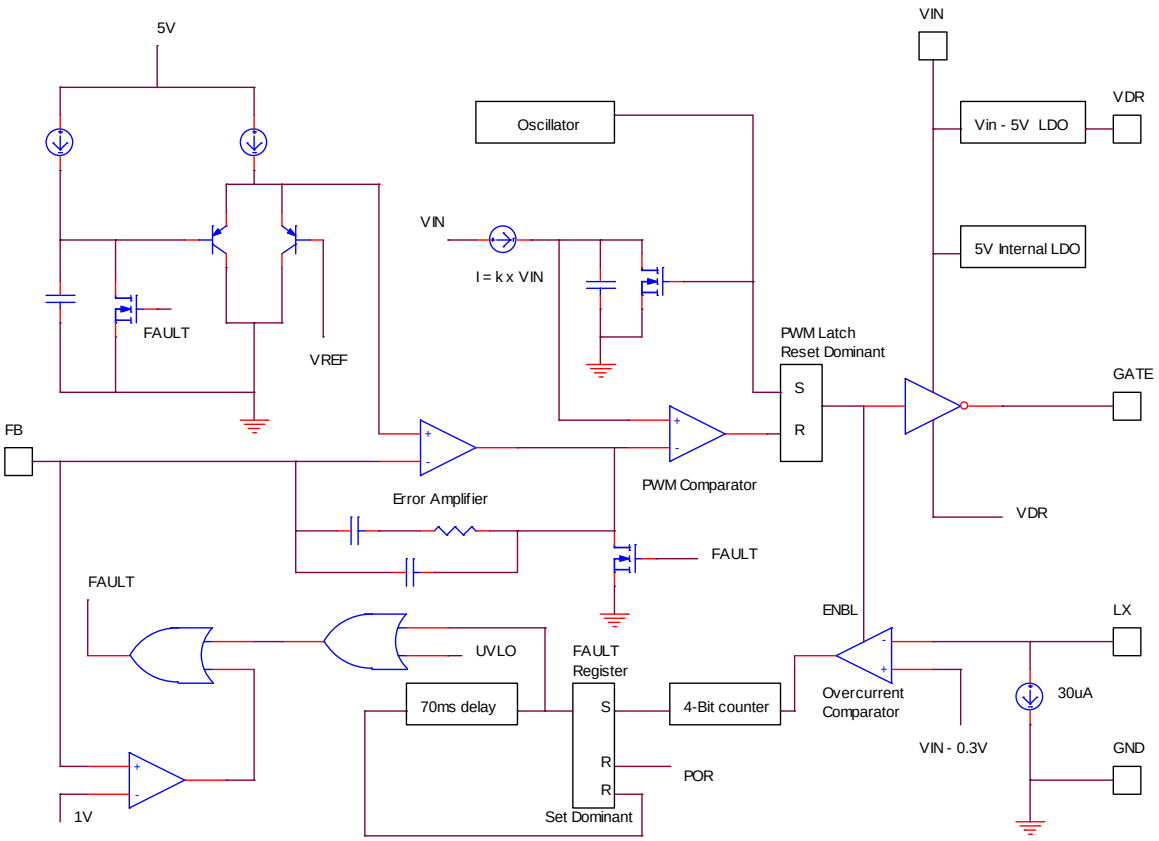
Specifications are for $T_{AMB}=T_J=25°C$, and those denoted by ♦ apply over the full operating range, -40°C< T_j <125°C. Unless otherwise specified: VIN =4.5V to 29V, C_{IN} = 4.7µF.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
UVLO Turn-On Threshold	4.2	4.35	4.5	V		0°C< T_j <125°C
UVLO Turn-Off Threshold	4.0	4.15	4.4	V		0°C< T_j <125°C
UVLO Hysteresis		0.2		V		
Operating Input Voltage Range	4.5		29	V		0°C< T_j <125°C
Operating Input Voltage Range	7		29	V	♦	
Operating VCC Current		0.3	3	mA		VFB=1.2V
Reference Voltage Accuracy		0.5	1	%		
Reference Voltage Accuracy		0.5	2	%	♦	
Reference Voltage	0.594	0.6	0.606	V		
Reference Voltage	0.588	0.6	0.612	V	♦	
Switching Frequency	750	900	1050	kHz		
Peak-to-peak ramp Voltage		V_{IN}/5		V		
Minimum ON-Pulse Duration		40	100	ns	♦	
Minimum Duty Cycle			0	%		
Maximum Duty Cycle	100			%		
Gate Driver Turn-Off Resistance		50	60	kΩ		Internal resistor between GATE and VIN
Gate Driver Pull-Down Resistance		4	8	Ω		VIN=12V, V_{FB}=0.5V, Measure resistance between GATE and VDR
Gate Driver Pull-up Resistance		3	6	Ω		VIN=12V, V_{FB}=0.7V, Measure resistance between GATE and VIN
VIN - VDR voltage difference	4.5		5.5	V	♦	Measure VIN – VDR, VIN>7V
Overcurrent Threshold	270	300	330	mV		Measure VIN - LX
LX pin Input Current	25	30	35	uA		V_{LX} = VIN
OFF interval during hiccup		70		ms		
Soft start time	3	5	9	ms		VFB=0.58V, measure between VIN=4.5V and first GATE pulse
SHDN Threshold	0.8	1.0	1.2	V	♦	Apply voltage to FB
SHDN Threshold Hysteresis		100		mV		

PIN DESCRIPTION

PIN #	PIN NAME	DESCRIPTION
1	VIN	Input power supply for the controller. Place input decoupling capacitor as close as possible to this pin.
2	GATE	Connect to the gate terminal of the external P-channel MOSFET.
3	VDR	Power supply for the internal driver. This voltage is internally regulated to about 5V below VIN. Place a 0.1µF decoupling capacitor between VDR and VIN as close as possible to the IC.
4	FB	Regulator feedback input. Connect to a resistive voltage-divider network to set the output voltage. This pin can be also used for ON/OFF control. If this pin is pulled above 1V the P-channel driver is disabled and controller resets internal soft start circuit.
5	GND	Ground pin.
6	LX	This pin is used as a current limit input for the internal current limit comparator. Connect to the drain pin of the external MOSFET through an optional resistor. Internal threshold is pre-set to 300mV nominal and can be decreased by changing the external resistor based on the following formula: V_{TRSHLD} = 300mV – 30uA * R

BLOCK DIAGRAM



The SP6127 is a fixed frequency, Voltage-mode, non-synchronous PWM controller optimized for minimum component, small form factor and cost effectiveness. It has been designed for single-supply operation ranging from 4.5V to 29V. SP6127 has Type-II internal compensation for use with Electrolytic/Tantalum output capacitors. For ceramic capacitors Type-III compensation can be implemented by simply adding an R and C between output and Feedback. A precision 0.6V reference, present on the positive terminal of the Error Amplifier, permits programming of the output voltage down to 0.6V via the FB pin. The output of the Error Amplifier is internally compared to a feed-forward (V_{IN}/5 peak-to-peak) ramp and generates the PWM control. Timing is governed by an internal oscillator that sets the PWM frequency at 900kHz.

SP6127 contains useful protection features. Overcurrent protection is based on the high-side MOSFET's $R_{DS(ON)}$ and is programmable via a resistor placed at LX node. Under-Voltage Lock-Out (UVLO) ensures that the controller starts functioning only when sufficient voltage exists for powering IC's internal circuitry.

SP6127 Loop Compensation

The SP6127 includes Type-II internal compensation components for loop compensation. External compensation components are not required for systems with tantalum or aluminum electrolytic output capacitors with sufficiently high ESR. Use the condition below as a guideline to determine whether or not the internal compensation is sufficient for your design.

Type-II internal compensation is sufficient if the following condition is met:

$$f_{ESRZERO} < f_{DBPOLE} \quad \text{..... (1)}$$

where:

$$f_{ESRZERO} = \frac{1}{2.\pi.R_{ESR}.C_{OUT}} \quad \text{..... (2)}$$

$$f_{DBPOLE} = \frac{1}{2.\pi.\sqrt{L \cdot C_{OUT}}} \quad \text{..... (3)}$$

Creating a Type-III compensation Network

The above condition requires the ESR zero to be at a lower frequency than the double-pole from the LC filter. If this condition is not met, Type-III compensation should be used and can be accomplished by placing a series RC combination in parallel with R1 as shown below. The value of CZ can be calculated as follows and RZ selected from table 1.

$$CZ = \frac{\sqrt{L \cdot C}}{1.25 \times R1} \quad \text{..... (4)}$$

$f_{ESRZERO}$/ f_{DBPOLE}	Rz
1X	50KΩ
2X	40KΩ
3X	30KΩ
5X	10KΩ
>= 10X	2KΩ

Table1- Selection of Rz

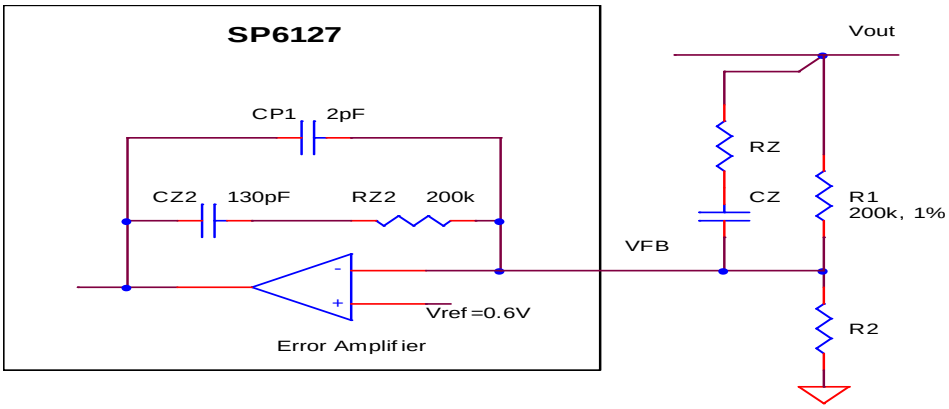


Figure 1- RZ and CZ in conjunction with internal compensation components form a Type-III compensation network

Loop Compensation Example 1- A converter utilizing a SP6127 has a 3.3µH inductor and a 22µF/5mΩ ceramic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{ESRZERO}$ = 1.45MHz. From equation (3) f_{DBPOLE} = 18.4 kHz. Since the condition specified in (1) is not met, Type-III compensation must be used by adding external components RZ and CZ. Using equation (4) CZ is calculated to be 34pF (use 33pF). Following the guideline given in table 1, a 2kΩ RZ should be used.

The steps followed in example 1 were used to compensate the typical application circuit shown on page 1. Satisfactory frequency response of the circuit, seen in figure 2, validates the above procedure.

Loop Compensation Example 2- A converter utilizing the SP6127 has a 3.3µH inductor and a 220µF, 82mΩ Aluminum Electrolytic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{ESRZERO}$ = 8.8kHz. From equation (3) f_{DBPOLE} = 5.9kHz. Since the condition specified in (1) is not met, Type-III compensation needs to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 108pF (use 100 pF). Since $f_{ESRZERO}$ /f_{DBPOLE} is approximately 2, RZ must be set at 40kΩ.

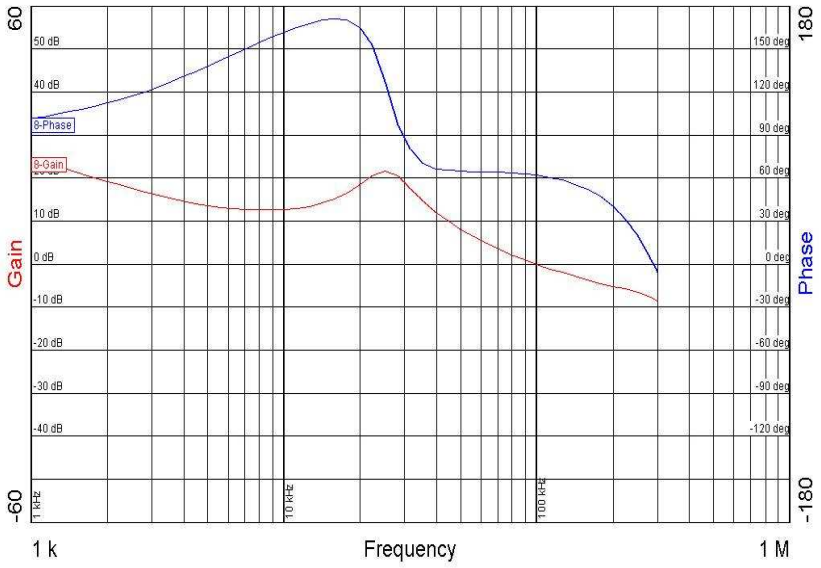


Figure 2- Satisfactory frequency response of typical application circuit shown on page 1. Crossover frequency f_C is 100kHz with a corresponding phase margin of 60 degrees.

Overcurrent Protection (OCP)

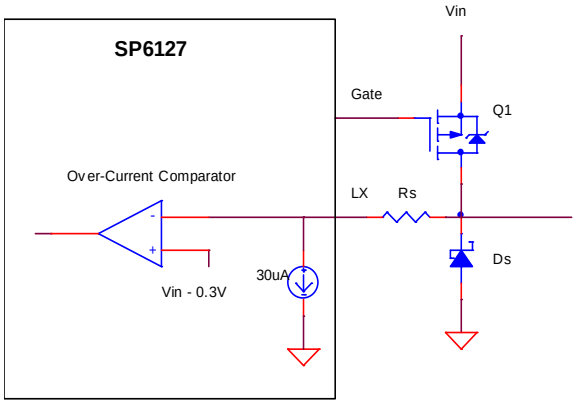


Figure 3 Overcurrent protection circuit

The overcurrent protection (OCP) circuit functions by monitoring the voltage across the high-side FET Q1. When this voltage exceeds 0.3V, the overcurrent comparator triggers and the controller enters hiccup mode. For example if Q1 has $R_{DS(ON)}$=0.1Ω, then the overcurrent will trigger at I = 0.3V/0.1Ω=3A. To program a lower overcurrent use a resistor Rs as shown in figure 1. Calculate Rs from:

$$Rs = \frac{0.3 - (1.15 \times Iout \times Rds(on) \times Kt)}{30uA} \quad ...(5)$$

Where:

1.15 is used to calculate peak inductor current which is nominally 15% higher than average output current
$R_{DS(ON)}$ is MOSFET ON-resistance rating
Kt is a multiplier that accounts for increase in $R_{DS(ON)}$ due to temperature

Example: A switching MOSFET used with SP6127 has $R_{DS(ON)}$ of 0.08Ω and Kt is 1.5. Program the over-current circuit so that maximum output is 2A.

$$Rs = \frac{0.3 - (1.15 \times 2A \times 0.08Ohm \times 1.5)}{30uA}$$

Rs=800Ω

Using the above equation there is good agreement between calculated and test results for Rs in the range of 0.5kΩ to 3kΩ. For Rs larger than 3kΩ, test results are lower than those predicted by (5), due to circuit parasitics. Therefore the maximum value of Rs should be limited to 3kΩ.

Note that in order to safeguard against false overcurrent trigger due to transients, there is a 150ns delay between the turn on of the MOSFET and when OCP circuit is activated. As a consequence at very high Vo/V_{IN} ratio, where MOSFET on-time is less than 150ns, the OCP circuit will not detect overcurrent.

Using the ON/OFF Function

The Feedback pin serves a dual role of ON/OFF control. The MOSFET driver is disabled when a voltage greater than 1V is applied at the FB pin. Maximum voltage rating of this pin is 5.5V. The controlling signal should be applied through a small signal diode as shown on page 1.

Please note that an optional 10kΩ bleeding resistor across the output helps keep the output capacitor discharged under no load condition.

Programming the Output Voltage

To program the output voltage, calculate R2 using the following equation:

$$R2 = \frac{R1}{\left(\frac{Vout}{Vref} - 1\right)}$$

Where:

V_{REF}=0.6 is the reference voltage of the SP6127
R1=200kΩ is a fixed-value resistor that, in addition to being a voltage divider, it is part of the compensation network. In order to simplify compensation calculations, R1 is fixed at 200kΩ.

Soft Start

Soft Start is preset internally to 5ms (nominal). Internal Soft Start eliminates the need for the external capacitor CSS that is commonly used to program this function.

MOSFET Gate Drive

The P-channel drive is derived through an internal regulator that generates VIN-5V. This pin (VDR) must be connected to VIN with a 0.1µF decoupling capacitor. The gate drive circuit swings between VIN and VIN-5 and employs powerful drivers for efficient switching of the P-channel MOSFET.

Power MOSFET Selection

Select the Power MOSFET for Voltage rating BVDSS, On resistance RDS(ON), and thermal resistance RTHJA. BVDSS should be about twice as high as VIN in order to guard against switching transients. The recommended MOSFET voltage rating for VIN of 5V, 12V and 24V is 12V, 30V and 40V respectively. RDS(ON) must be selected such that when operating at peak current and junction temperature, the Overcurrent threshold of the SP6127 is not exceeded. Allowing 50% for temperature coefficient of RDS(ON) and 15% for inductor current ripple, the following expression can be used:

$$RDS(ON) \le \left(\frac{0.3V}{1.5 \times 1.15 \times Iout} \right)$$

Within this constraint, selecting MOSFETs with lower RDS(ON) will reduce conduction losses at the expense of increased switching losses. As a rule of thumb, select the highest RDS(ON) MOSFET that meets the above criteria. Switching losses can be assumed to roughly equal to the conduction losses. A simplified expression for conduction losses is given by:

$$Pcond = Iout^2 \times RDS(ON) \times \left(\frac{Vout}{Vin} \right)$$

The MOSFET's junction temperature can be estimated from:

$$T = \left(2 \times Pc \times Rthja\right) + Tambient$$

Schottky Rectifier selection

Select the Schottky Diode for Voltage rating V_R, Forward voltage V_f, and thermal resistance RTHJA. The Voltage rating should be selected using the same guidelines outlined for MOSFET voltage selection. For a low duty cycle application such as the circuit shown on first page, the Schottky diode is conducting most of the time and its conduction losses are the largest component of losses in the converter. Conduction losses can be estimated from:

$$Pc = Vf \times Iout \times \left(1 - \frac{Vout}{Vin}\right)$$

where:
VF is diode forward voltage at IOUT

The Schottky diode's AC losses due to its switching capacitance are negligible.

Inductor Selection

Select the Inductor for inductance L and saturation current ISAT. Select an inductor with ISAT higher than the programmed overcurrent. Calculate inductance from:

$$L = \left(Vin - Vout\right) \times \left(\frac{Vout}{Vin}\right) \times \left(\frac{1}{f}\right) \times \left(\frac{1}{Irip}\right)$$

where:

VIN is converter input voltage
VOUT is converter output voltage
f is switching frequency
IRIP is inductor peak-to-peak current ripple (nominally set to 30% of IOUT)

Keep in mind that a higher IRIP results in a smaller inductor which has the advantages of small size, low DC equivalent resistance DCR, high saturation current ISAT and allows the use of a lower output capacitance to meet a given step load transient. A higher IRIP, however, increases the output voltage ripple and increases the current at which converter enters Discontinuous Conduction Mode. The output current at which converter enters DCM is ½ of IRIP. Note that a negative current step load that drives the converter into DCM will result in a large output voltage transient. Therefore the lowest current for a step load should be larger than ½ of IRIP.

Output Capacitor Selection

Select the output capacitor for voltage rating, capacitance and Equivalent Series Resistance (ESR). Nominally the voltage rating is selected to be twice as large as the output voltage. Select the capacitance to satisfy the specification for output voltage overshoot/undershoot caused by current step load. A steady-state output current I_{OUT} corresponds to inductor stored energy of ½ L I_{OUT}^2. A sudden decrease in I_{OUT} forces the energy surplus in L to be absorbed by C_{OUT}. This causes an overshoot in output voltage that is corrected by the reduced duty cycle of the power switch. Use the following equation to calculate C_{OUT}:

$$Cout = L \times \left(\frac{I_2^{\,2} - I_1^{\,2}}{\mathrm{Vos}^2 - \mathrm{Vout}^2} \right)$$

Where:

L is the output inductance
I_2 is the step load high current
I_1 is the step load low current
Vos is output voltage including overshoot
V_{OUT} is steady state output voltage

Output voltage undershoot calculation is more complicated. Test results for SP6127 buck circuits show that undershoot is approximately equal to overshoot. Therefore the above equation provides a satisfactory method for calculating C_{OUT}.

Select ESR such that output voltage ripple (V_{RIP}) specification is met. There are two components to V_{RIP}: The first component arises from charge transferred to and from C_{OUT} during each cycle. The second component of V_{RIP} is due to inductor ripple current flowing through the output capacitor's ESR. It can be calculated from:

$$Vrip = Irip \times \sqrt{ESR^2 + \left(\frac{1}{8 \times Cout \times fs} \right)^2}$$

Where:
I_{RIP} is inductor ripple current
f_S is switching frequency
C_{OUT} is output capacitor calculated above

Note that a smaller inductor results in a higher I_{RIP}, therefore requiring a larger C_{OUT} and/or lower ESR in order to meet V_{RIP}.

Input Capacitor Selection

Select the input capacitor for Voltage, Capacitance, ripple current, ESR and ESL. Voltage rating is nominally selected to be twice the input voltage. The RMS value of the input capacitor current, assuming a low inductor ripple current (I_{RIP}), can be calculated from:

$$Icin = Iout \times \sqrt{D(1-D)}$$

In general, total input voltage ripple should be kept below 1.5% of V_{IN} (not to exceed 180mV). Input voltage ripple has three components: ESR and ESL cause a step voltage drop upon turn on of the MOSFET. During on time, the capacitor discharges linearly as it supplies I_{OUT}-I_{IN}. The contribution to Input voltage ripple by each term can be calculated from:

$$\Delta V, Cin = \frac{Iout \times Vout \times (Vin - Vout)}{fs \times Cin \times Vin^2}$$

$$\Delta V, ESR = ESR(Iout - 0.5Irip)$$

$$\Delta V, ESL = ESL \frac{(Iout - 0.5Irip)}{Trise}$$

Where T_{RISE} is the rise time of current through capacitor

Total input voltage ripple is sum of the above:

$$\Delta V, Tot = \Delta V, Cin + \Delta V, ESR + \Delta V, ESL$$

In circuits where converter input voltage is applied via a mechanical switch, excessive ringing may be present at turn-on that may interfere with smooth startup of the SP6127. The addition of an inexpensive 100µF Aluminum Electrolytic capacitor at the input will help reduce ringing and restore a smooth startup.

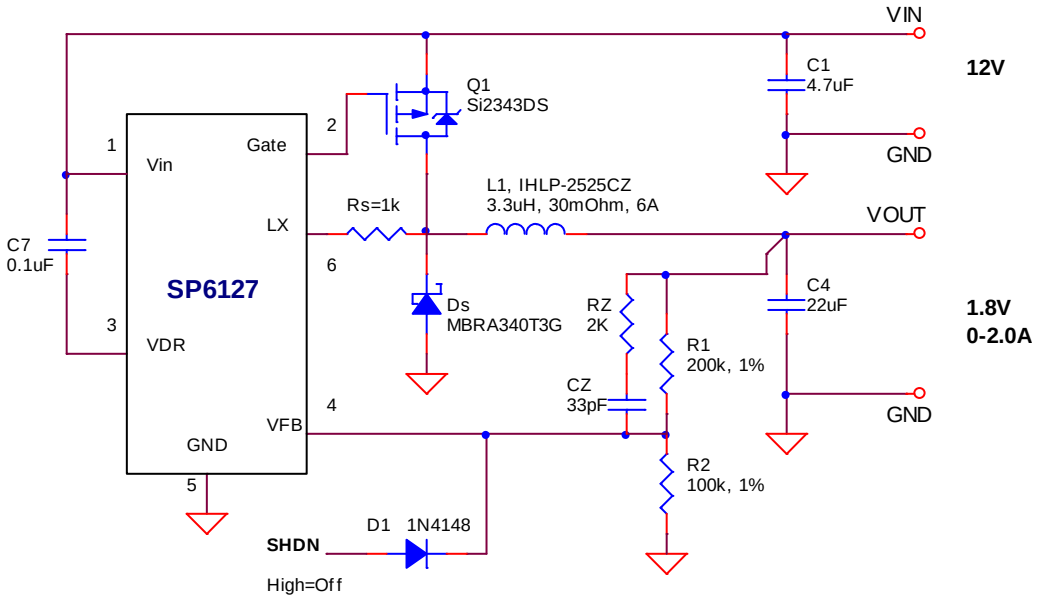


Figure 4- Application circuit

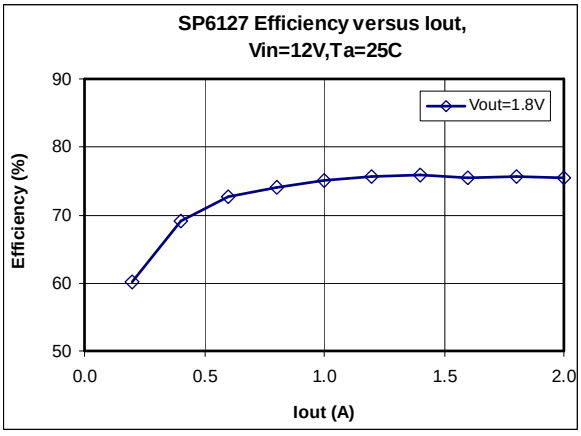


Figure 5- Efficiency, natural convection

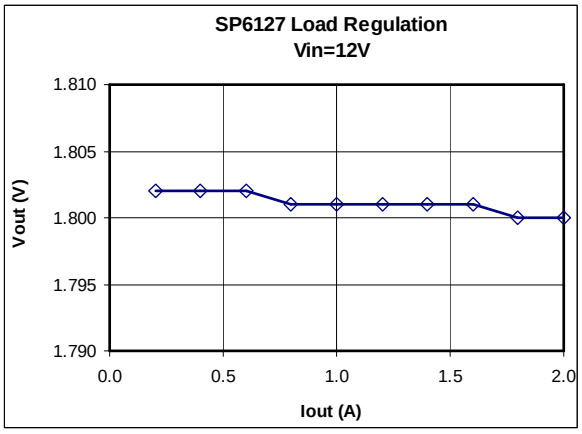


Figure 6- Load regulation

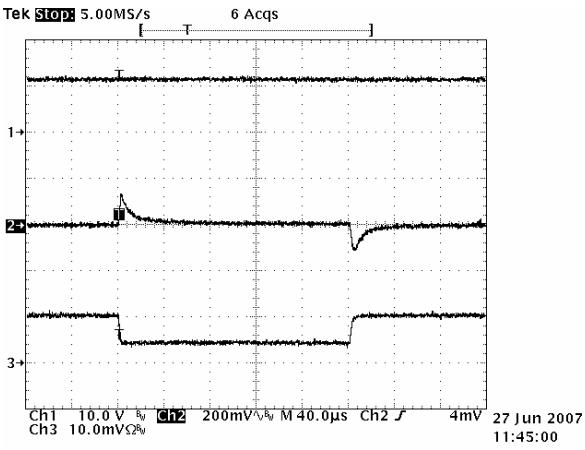


Figure 7- Step load 1-2A

ch1: VIN ch2: VOUT, ch3: IOUT

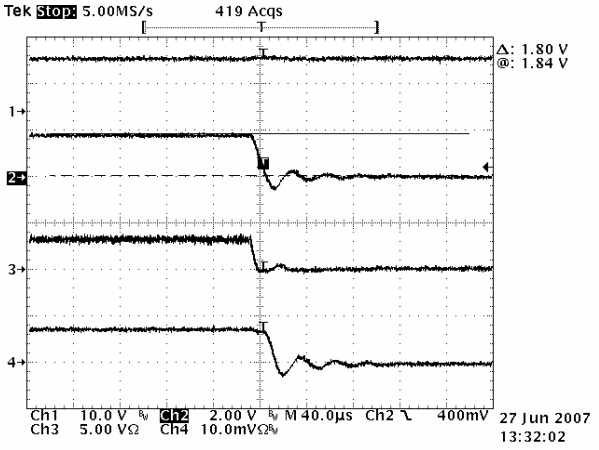


Figure 8- Overcurrent shutdown

ch1: VIN, ch2: VOUT, ch3: Inductor current, ch4: IOUT

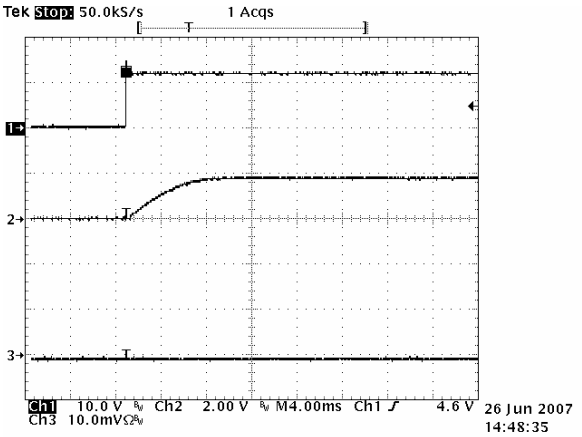


Figure 9- Startup no load

ch1: VIN, ch2: VOUT, ch3: IOUT

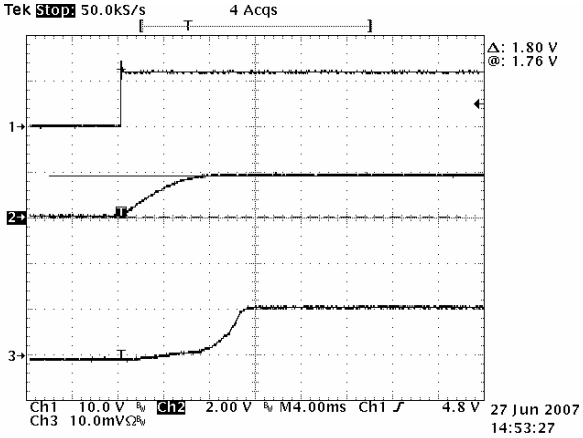


Figure 10- Start up 2A

ch1: VIN ch2: VOUT, ch3: IOUT

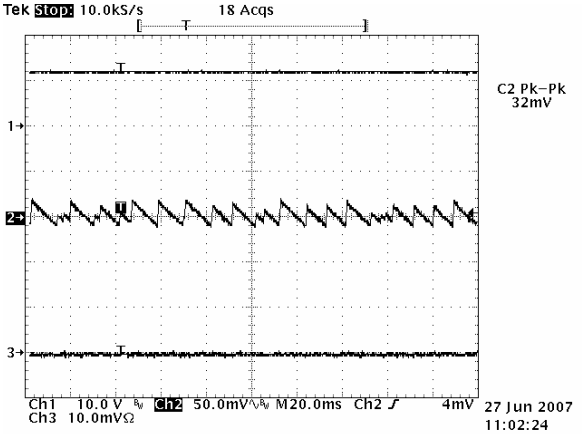


Figure 11- Output ripple at 0A is 32mV

ch1: VIN, ch2: VOUT, ch3: IOUT

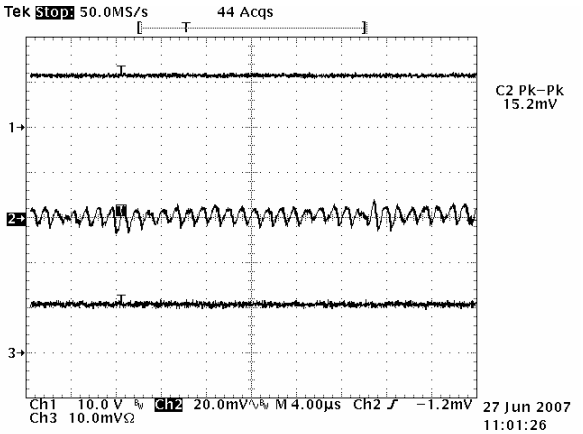
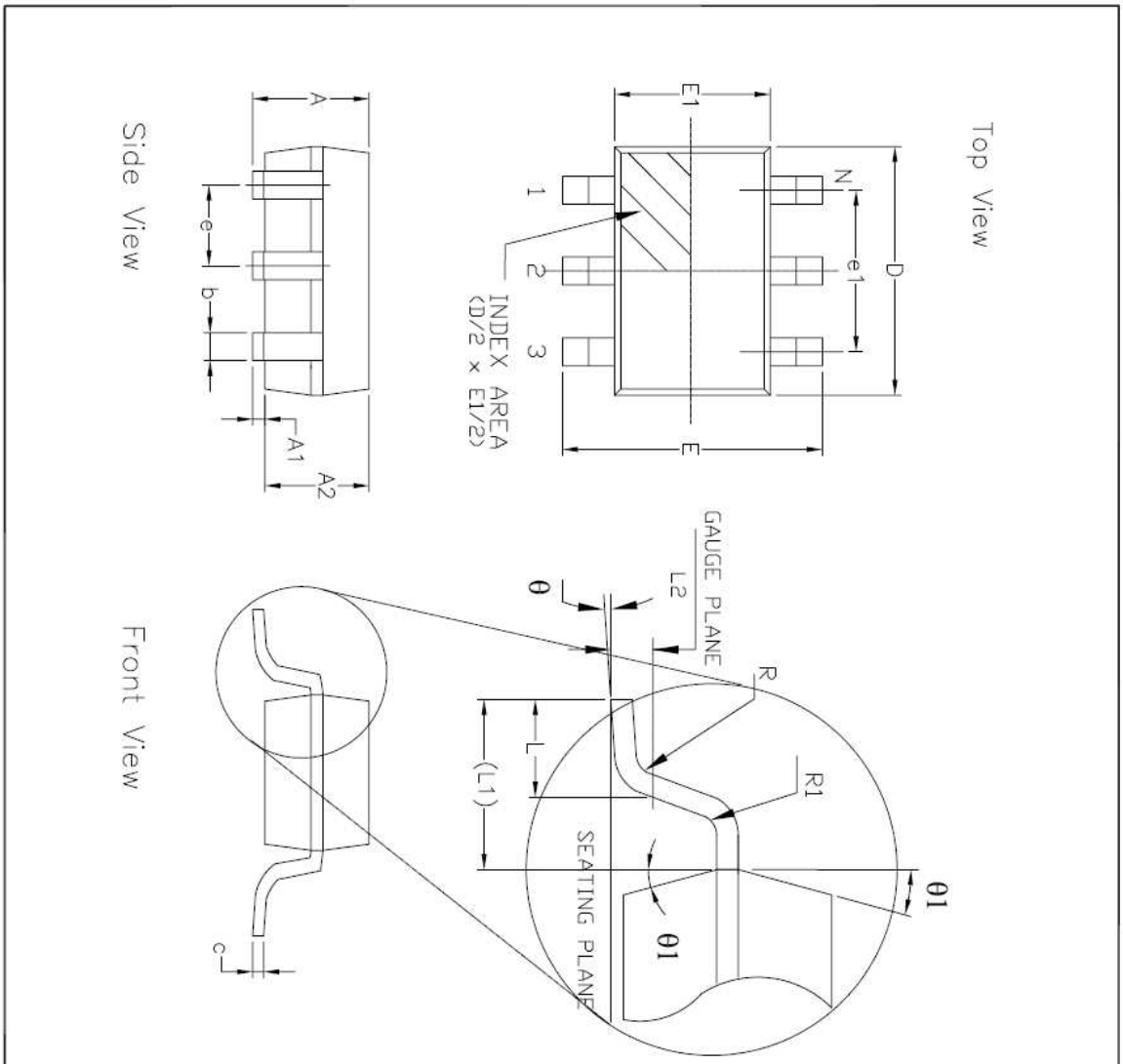


Figure 12- Output ripple at 2A is 12mV

ch1: VIN, ch2: VOUT, ch3: IOUT



REVISION HISTORY

REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/03/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL

6 Pin TSOT JEDEC MO-193 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	6			6		

EXAR CORPORATION

6 PIN TSOT PACKAGE OUTLINE

Packaging Approval:	Drawing No:	6-PIN TSOT	
By: JL	Date: 09/13/06	Revision: B	Sheet: 1 OF 1

ORDERING INFORMATION

Part Number	Temperature Range	Package
SP6127EK1-L	-40°C to +125°C	(Lead Free) 6 Pin TSOT
SP6127EK1-L/TR	-40°C to +125°C	(Lead Free) 6 Pin TSOT

/TR = Tape and Reel
Pack Quantity for Tape and Reel is 2500

For further assistance:

Email: customersupport@exar.com
EXAR Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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