

RJF0409JSP

40V, 5A Silicon N Channel Thermal FET
Power Switching

R07DS1228EJ0300
Rev.3.00
Jul 28, 2015

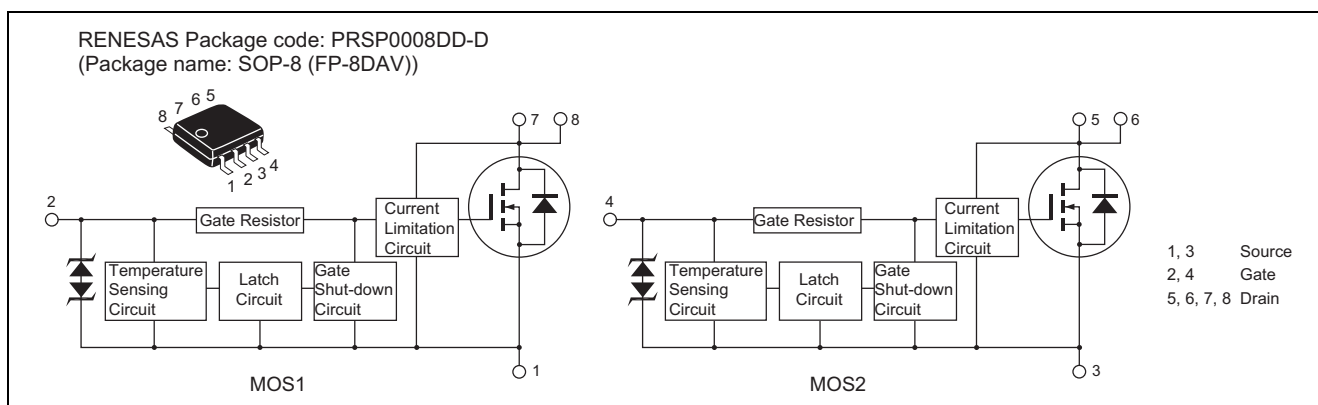
Description

This FET has the over temperature shut-down capability sensing to the junction temperature. This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc..

Features

- Logic level operation (4 V Gate drive).
- Built-in the over temperature shut-down circuit.
- High endurance capability against to the short circuit.
- Latch type shut down operation (need 0 voltage recovery).
- Built-in the current limitation circuit.
- High density mounting
- Power supply voltage applies 12 V.
- AEC-Q101 Compliant

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	40	V
Gate to source voltage	V_{GS}	16	V
Gate to source voltage	V_{GS}	-2.5	V
Drain current	I_D Note4	5	A
Body-drain diode reverse drain current	I_{DR}	5	A
Avalanche current	I_{AP} Note 3	1.5	A
Avalanche energy	E_{AR} Note 3	15	mJ
Channel dissipation	P_{ch} Note 1	1	W
Channel dissipation	P_{ch} Note 2	1.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. 1 Drive operation : When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s

2. 2 Drive operation : When using the glass epoxy board (FR4 40 × 40 × 1.6 mm), PW ≤ 10 s

3. T_{ch} = 25°C, R_g ≥ 50 Ω

4. It provides by the current limitation lower bound value.

Typical Operation Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	3.5	—	—	V	
	V _{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	100	μA	V _i = 8 V, V _{DS} = 0
	I _{IH2}	—	—	50	μA	V _i = 3.5 V, V _{DS} = 0
	I _{IL}	—	—	1	μA	V _i = 1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH(sD)1}	—	0.8	—	mA	V _i = 8 V, V _{DS} = 0
	I _{IH(sD)2}	—	0.35	—	mA	V _i = 3.5 V, V _{DS} = 0
Shut down temperature	T _{SD}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{OP}	3.5	—	12	V	
Drain current (Current limitation value)	I _D limit	5	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 5}

Notes: 5. Pulse test

Electrical Characteristics

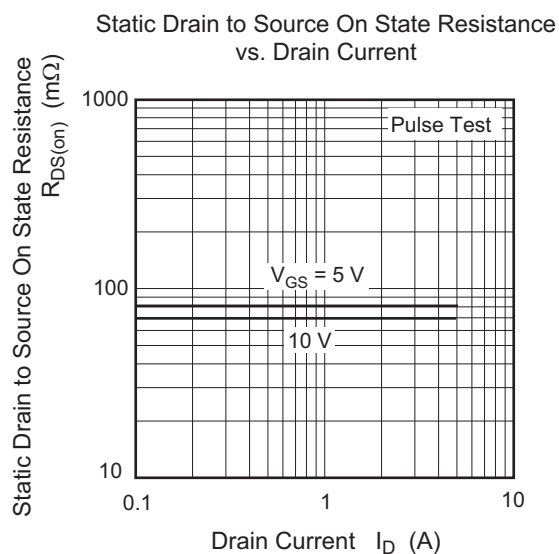
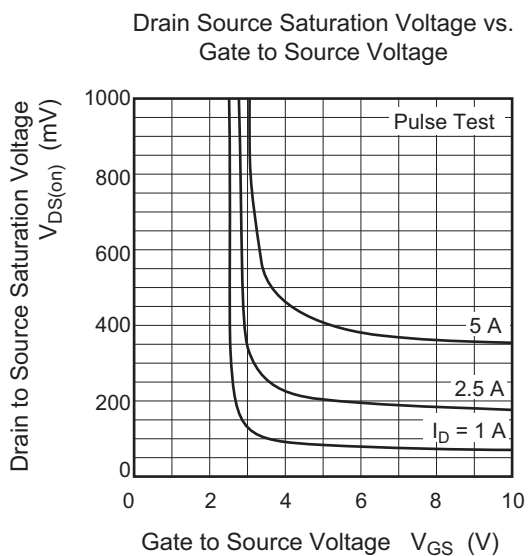
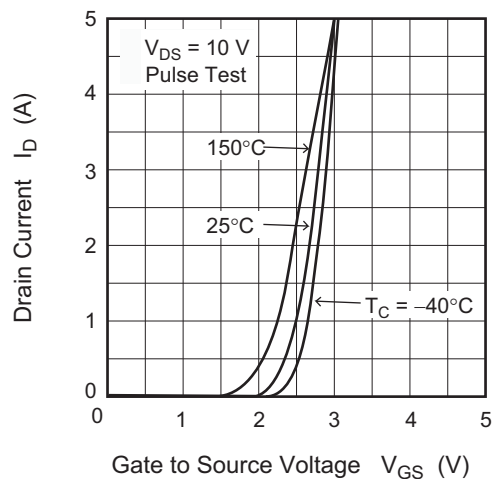
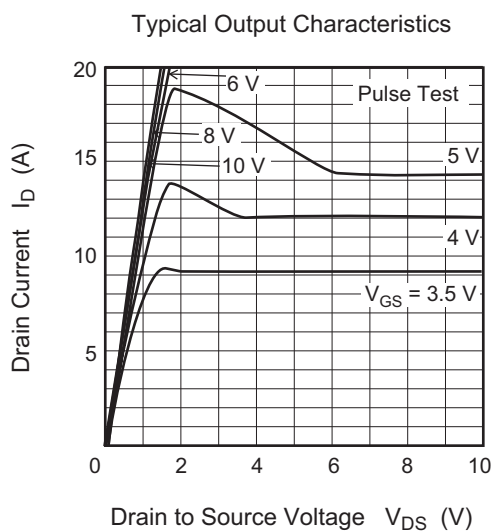
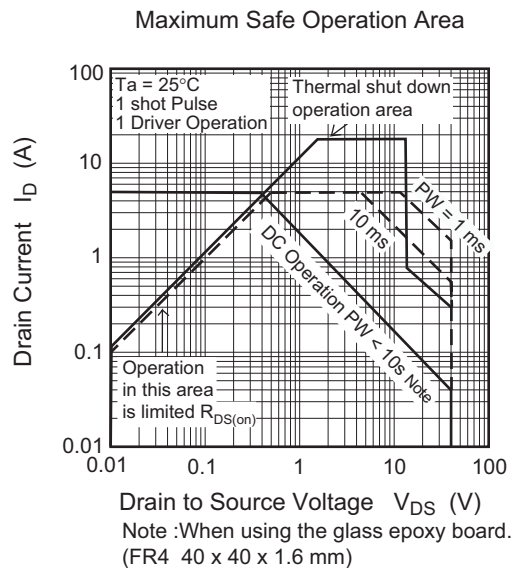
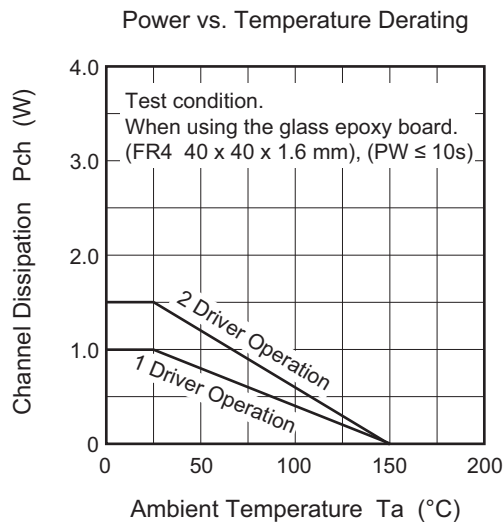
(Ta = 25°C)

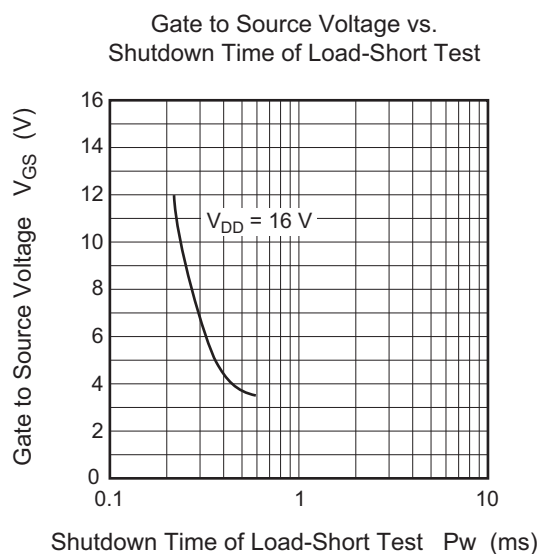
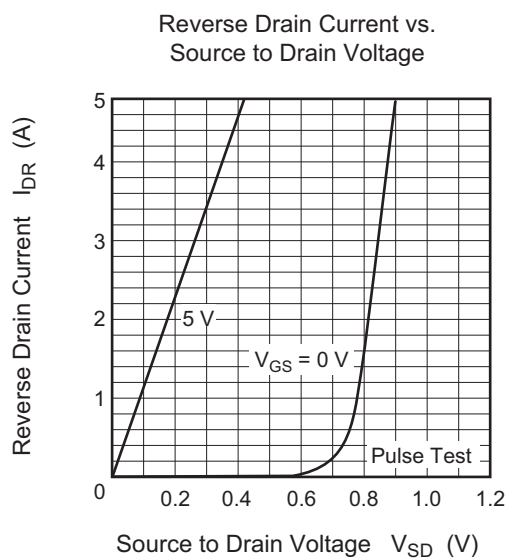
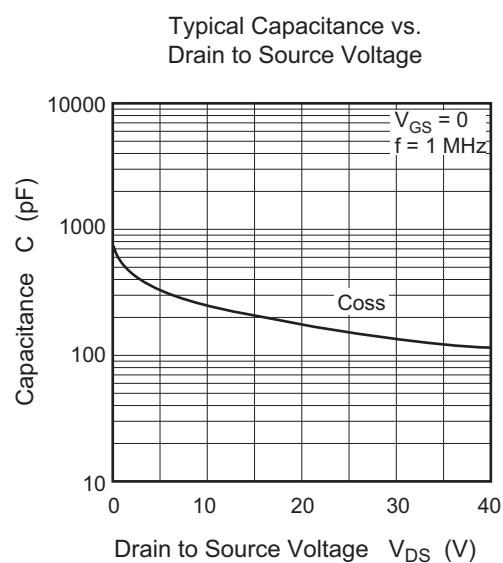
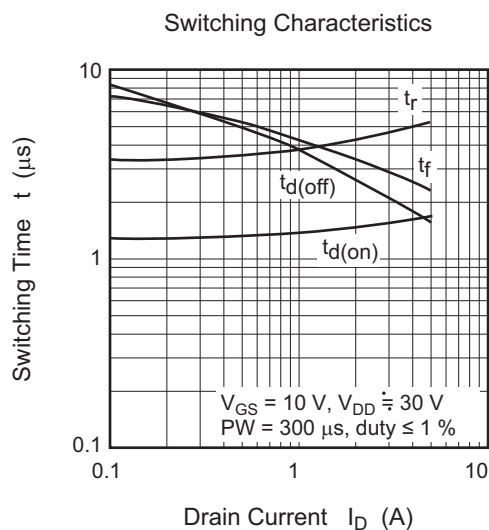
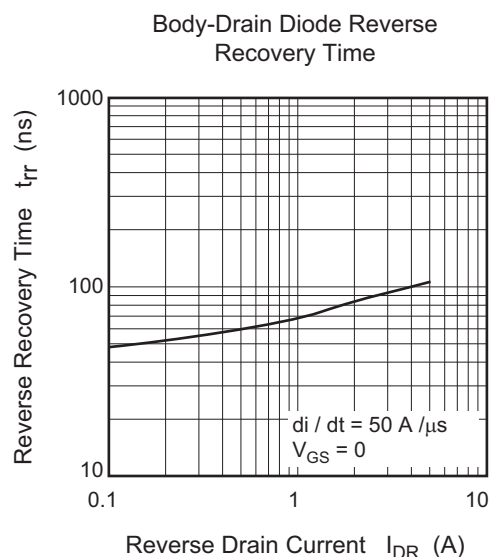
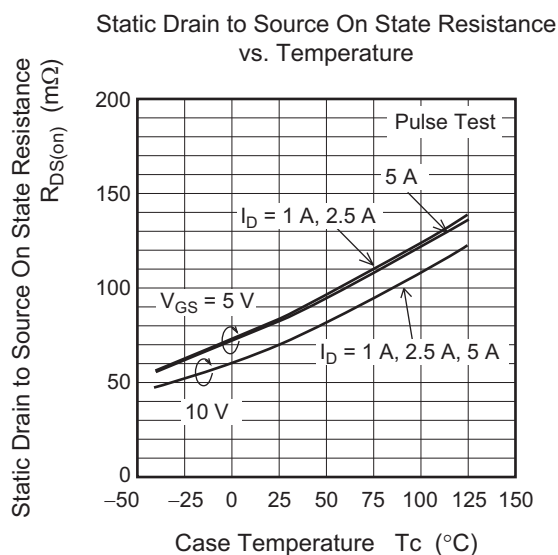
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I _{D1}	—	—	14	A	V _{GS} = 3.5 V, V _{DS} = 10 V ^{Note 6}
	I _{D2}	—	—	10	mA	V _{GS} = 1.2 V, V _{DS} = 10 V
	I _{D3}	5	—	—	A	V _{GS} = 5 V, V _{DS} = 10 V ^{Note 6}
Drain to source breakdown voltage	V _{(BR)DSS}	40	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	16	—	—	V	I _G = 800 μA, V _{DS} = 0
	V _{(BR)GSS}	-2.5	—	—	V	I _G = -100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS1}	—	—	100	μA	V _{GS} = 8 V, V _{DS} = 0
	I _{GSS2}	—	—	50	μA	V _{GS} = 3.5 V, V _{DS} = 0
	I _{GSS3}	—	—	1	μA	V _{GS} = 1.2 V, V _{DS} = 0
	I _{GSS4}	—	—	-100	μA	V _{GS} = -2.4 V, V _{DS} = 0
Input current (shut down)	I _{GS(OP)1}	—	0.8	—	mA	V _{GS} = 8 V, V _{DS} = 0
	I _{GS(OP)2}	—	0.35	—	mA	V _{GS} = 3.5 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	10	μA	V _{DS} = 32 V, V _{GS} = 0 Ta = 125°C
Gate to source cutoff voltage	V _{GS(off)}	1.1	—	2.1	V	I _D = 1 mA, V _{DS} = 10 V
Forward transfer admittance	y _{fs}	4	7	—	S	I _D = 2.5 A, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS(on)}	—	81	100	mΩ	I _D = 2.5 A, V _{GS} = 5 V ^{Note 6}
	R _{DS(on)}	—	70	86	mΩ	I _D = 2.5 A, V _{GS} = 10 V ^{Note 6}
Output capacitance	C _{oss}	—	245	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1MHz
Turn-on delay time	t _{d(on)}	—	1.65	—	μs	I _D = 2.5 A, V _{GS} = 10 V R _L = 12 Ω
Rise time	t _r	—	4.50	—	μs	
Turn-off delay time	t _{d(off)}	—	2.35	—	μs	
Fall time	t _f	—	3.0	—	μs	
Body-drain diode forward voltage	V _{DF}	—	0.89	—	V	I _F = 5 A, V _{GS} = 0 ^{Note 6}
Body-drain diode reverse recovery time	t _{rr}	—	106	—	ns	I _F = 5 A, V _{GS} = 0 di _F /dt = 50 A/μs
Over load shut down operation time ^{Note 7}	t _{OS}	—	0.37	—	ms	V _{GS} = 5 V, V _{DD} = 16 V

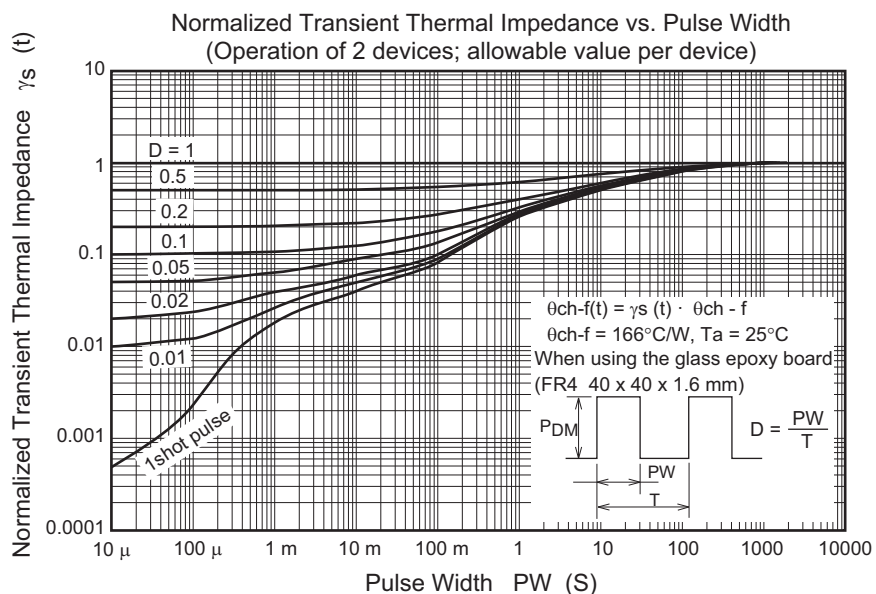
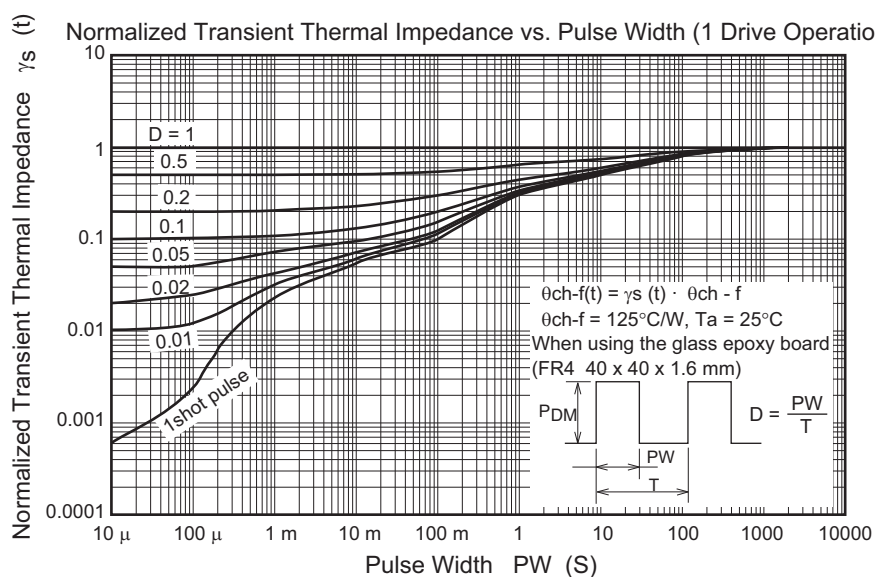
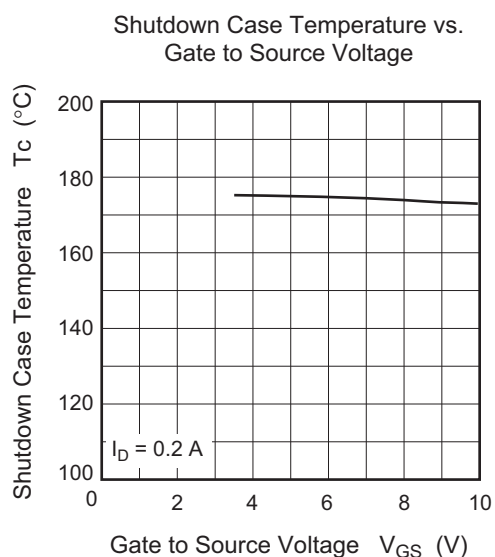
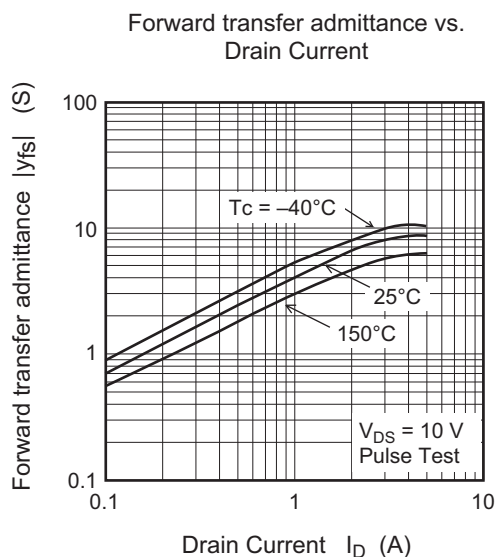
Notes: 6. Pulse test

7. Including the junction temperature rise of the over loaded condition.

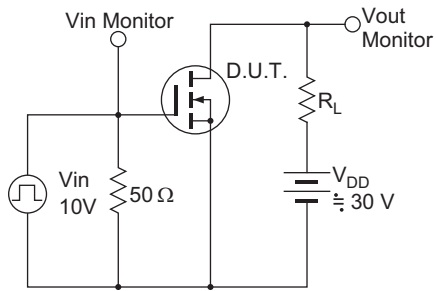
Main Characteristics



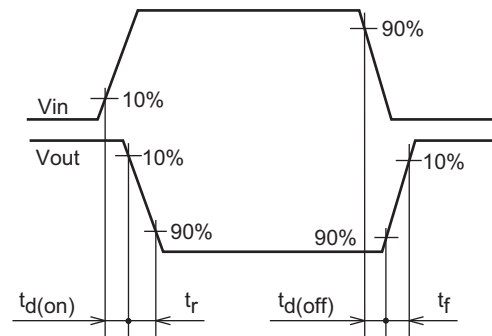




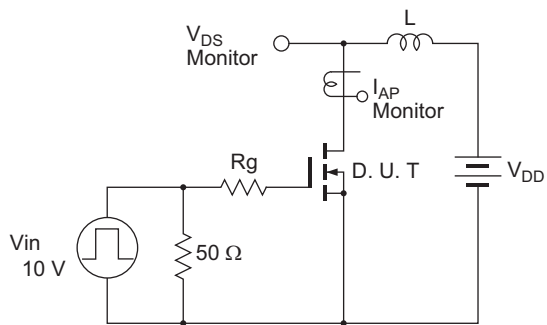
Switching Time Test Circuit



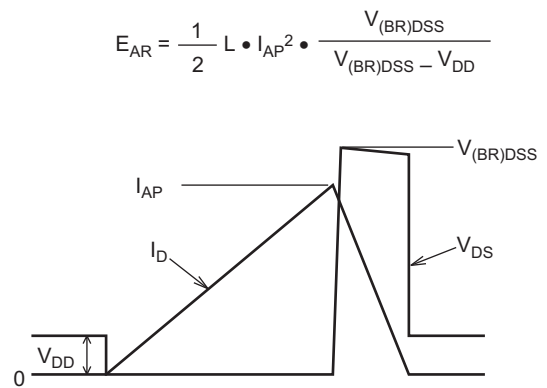
Waveform



Avalanche Test Circuit

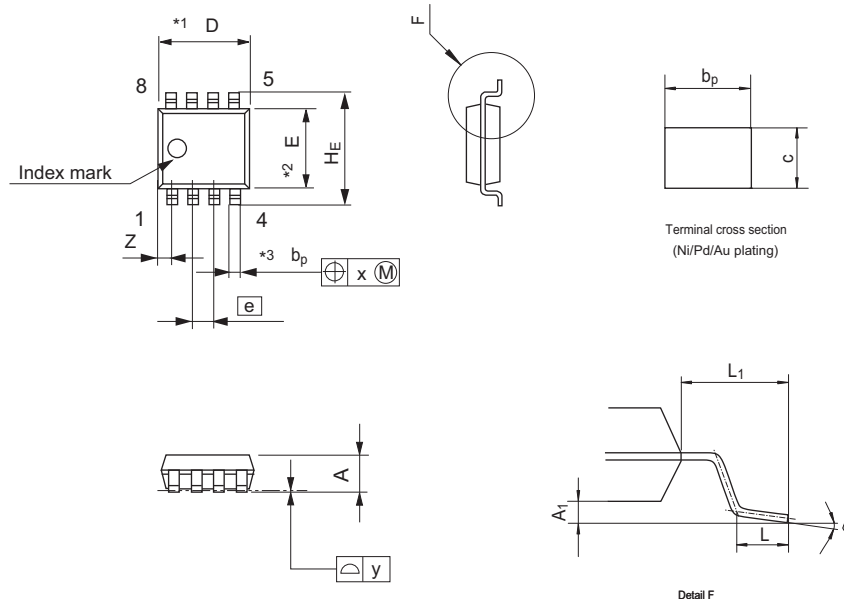


Avalanche Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SOP-8	P-SOP8-3.95 x 4.9-1.27	PRSP0008DD-D	FP-8DAV	0.085g



NOTE)
 1. DIMENSIONS $*1$ (Nom) AND $*2$ DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION $*3$ DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A ₂	—	—	—
A ₁	0.10	0.14	0.25
A	—	—	1.75
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
H _E	5.80	6.10	6.20
ϕ	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L ₁	—	1.08	—

Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJF0409JSP-00-J0	2500 pcs/reel	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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