# CA3049, CA3102

## Dual High Frequency Differential Amplifiers For Low Power Applications Up to 500MHz

December 1998

### Features

- **Power Gain 23dB (Typ) . . . . . 200MHz**
- **Noise Figure 4.6dB (Typ). . . . . 200MHz**
- **Two Differential Amplifiers on a Common Substrate**
- **Independently Accessible Inputs and Outputs**
- **Full Military Temperature Range . . . . . -55°C to 125°C**

### Applications

- **VHF Amplifiers**
- **VHF Mixers**
- **Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF**
- **IF Amplifiers (Differential and/or Cascode)**
- **Product Detectors**
- **Doubly Balanced Modulators and Demodulators**
- **Balanced Quadrature Detectors**
- **Cascade Limiters**
- **Synchronous Detectors**
- **Balanced Mixers**
- **Synthesizers**
- **Balanced (Push-Pull) Cascode Amplifiers**
- **Sense Amplifiers**

### Description

The CA3049T and CA3102 consist of two independent differential amplifiers with associated constant current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general purpose devices which exhibit low 1/f noise and a value of $f_T$ in excess of 1GHz. These feature make the CA3049T and CA3102 useful from DC to 500MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3049T and CA3102 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual channel applications where matched performance of the two channels is required.

The CA3102 is like the CA3049T except that it has a separate substrate connection for greater design flexibility.

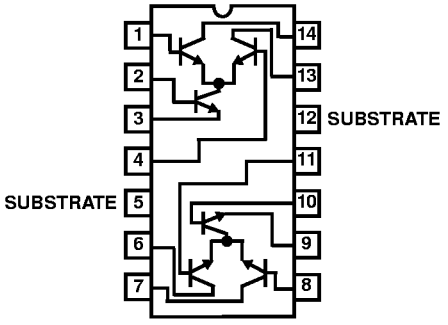
Formerly Developmental Type No. TA6228.

### Ordering Information

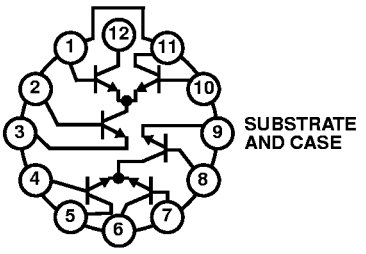
| PART NUMBER (BRAND) | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA3049T | -55 to 125 | 12 Pin Metal Can | T12.B |
| CA3102E | -55 to 125 | 14 Ld PDIP | E14.3 |
| CA3102M (3102) | -55 to 125 | 14 Ld SOIC | M14.15 |
| CA3102M96 (3102) | -55 to 125 | 14 Ld SOIC Tape and Reel | M14.15 |

### Pinouts

**CA3102**
**(PDIP, SOIC)**
TOP VIEW




**CA3049**
**(METAL CAN)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.



File Number **611.4**

## Absolute Maximum Ratings

Collector-to-Emitter Voltage, $V_{CEO}$ . . . . . 15V
Collector-to-Base Voltage, $V_{CBO}$ . . . . . 20V
Collector-to-Substrate Voltage, $V_{CIO}$ (Note 1) . . . . . 20V
Emitter-to-Base Voltage, $V_{EBO}$ . . . . . 5V
Collector Current, $I_C$ . . . . . 50mA

## Operating Conditions

Temperature Range . . . . . $-55^oC$ to $125^oC$

## Thermal Information

| Thermal Resistance (Typical, Note 2) | $\theta_{JA}$ ($^oC/W$) |
|---|---|
| Metal Can Package | 225 |
| PDIP Package | 130 |
| SOIC Package | 140 |

Maximum Power Dissipation (Any One Transistor) . . . . . 300mW
Maximum Junction Temperature (Can Package) . . . . . $175^oC$
Maximum Junction Temperature (Plastic Package) . . . . . $150^oC$
Maximum Storage Temperature Range . . . . . $-65^oC$ to $150^oC$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^oC$
(SOIC - Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. The collector of each transistor of the CA3049T and CA3102 is isolated from the substrate by an integral diode. The substrate (Terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications $T_A = 25^oC$

| PARAMETER | SYMBOL | TEST CONDITIONS | | CA3102 MIN | CA3102 TYP | CA3102 MAX | CA3049 MIN | CA3049 TYP | CA3049 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| **DC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER** | | | | | | | | | | |
| Input Offset Voltage (Figures 1, 4) | $V_{IO}$ | | | - | 0.25 | 5.0 | - | 0.25 | - | mV |
| Input Offset Current (Figure 1) | $I_{IO}$ | $I_3 = I_9 = 2mA$ | | - | 0.3 | 3.0 | - | 0.3 | - | µA |
| Input Bias Current (Figures 1, 5) | $I_B$ | | | - | 13.5 | 33 | - | 13.5 | 33 | µA |
| Temperature Coefficient Magnitude of Input Offset Voltage | $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$ | | | - | 1.1 | - | - | 1.1 | - | $\mu V/^oC$ |
| **DC CHARACTERISTICS FOR EACH TRANSISTOR** | | | | | | | | | | |
| DC Forward Base-to-Emitter Voltage (Figure 6) | VBE | $V_{CE} = 6V$, $I_C = 1mA$ | | 674 | 774 | 874 | - | 774 | - | mV |
| Temperature Coefficient of Base-to-Emitter Voltage (Figure 6) | $\frac{\Delta V_{BE}}{\Delta T}$ | $V_{CE} = 6V$, $I_C = 1mA$ | | - | -0.9 | - | - | -0.9 | - | $mV/^oC$ |
| Collector Cutoff Current (Figure 7) | $I_{CBO}$ | $V_{CB} = 10V$, $I_E = 0$ | | - | 0.0013 | 100 | - | 0.0013 | 100 | nA |
| Collector-to-Emitter Breakdown Voltage | $V_{(BR)CEO}$ | $I_C = 1mA$, $I_B = 0$ | | 15 | 24 | - | 15 | 24 | - | V |
| Collector-to-Base Breakdown Voltage | $V_{(BR)CBO}$ | $I_C = 10µA$, $I_E = 0$ | | 20 | 60 | - | 20 | 60 | - | V |
| Collector-to-Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_C = 10µA$, $I_B = I_E = 0$ | | 20 | 60 | - | 20 | 60 | - | V |
| Emitter-to-Base Breakdown Voltage | $V_{(BR)EBO}$ | $I_E = 10µA$, $I_C = 0$ | | 5 | 7 | - | 5 | 7 | - | V |
| **DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER** | | | | | | | | | | |
| 1/f Noise Figure (For Single Transistor) (Figure 12) | NF | f = 100kHz, $R_S = 500\Omega$, $I_C = 1mA$ | | - | 1.5 | - | - | 1.5 | - | dB |
| Gain Bandwidth Product (For Single Transistor) (Figure 11) | $f_T$ | $V_{CE} = 6V$, $I_C = 5mA$ | | - | 1.35 | - | - | 1.35 | - | GHz |
| Collector-Base Capacitance (Figure 8) | $C_{CB}$ | $I_C = 0$, $V_{CB} = 5V$ | Note 3 | - | 0.28 | - | - | 0.28 | - | pF |
| | | | Note 4 | - | 0.15 | - | - | 0.28 | - | pF |
| Collector-Substrate Capacitance (Figure 8) | $C_{CI}$ | $I_C = 0$, $V_{CI} = 5V$ | | - | 1.65 | - | - | 1.65 | - | pF |

## Electrical Specifications $T_A = 25^oC$ (Continued)

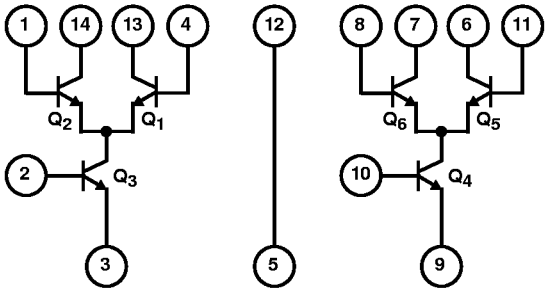
| PARAMETER | SYMBOL | TEST CONDITIONS | | CA3102 MIN | CA3102 TYP | CA3102 MAX | CA3049 MIN | CA3049 TYP | CA3049 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| Common Mode Rejection Ratio | CMRR | $I_3 = I_9 = 2mA$ | | - | 100 | - | - | 100 | - | dB |
| AGC Range, One Stage (Figure 2) | AGC | Bias Voltage = -6V | | - | 75 | - | - | 75 | - | dB |
| Voltage Gain, Single-Ended Output (Figures 2, 9, 10) | A | Bias Voltage = -4.2V, f = 10MHz | | 18 | 22 | - | - | 22 | - | dB |
| Insertion Power Gain (Figure 3) | $G_P$ | $V_{CC}$ = 12V, For Cascode Configuration $I_3 = I_9 = 2mA$. For Diff. Amp. Configuration $I_3 = I_9 = 4mA$ (Each Collector $I_C \cong 2mA$) f = 200MHz | Cascode | - | 23 | - | - | 23 | - | dB |
| Noise Figure (Figure 3) | NF | | Cascode | - | 4.6 | - | - | 4.6 | - | dB |
| Input Admittance | $Y_{11}$ | | Cascode (Figures 14, 16, 18) | - | 1.5 + j2.45 | - | - | 1.5 + j2.45 | - | mS |
| | | | Diff. Amp. (Figures 15, 17, 19) | - | 0.878 + j1.3 | - | - | 0.878 + j1.3 | - | mS |
| Reverse Transfer Admittance | $Y_{12}$ | | Cascode | - | 0.0 - j0.008 | - | - | 0.0 - j0.008 | - | mS |
| | | | Diff. Amp. | - | 0.0 - j0.013 | - | - | 0.0 - j0.013 | - | mS |
| Forward Transfer Admittance | $Y_{21}$ | | Cascode (Figures 26, 28, 30) | - | 17.9 - j30.7 | - | - | 17.9 - j30.7 | - | mS |
| | | | Diff. Amp. (Figures 27, 29, 31) | - | -10.5 + j13 | - | - | -10.5 + j13 | - | mS |
| Output Admittance | $Y_{22}$ | | Cascode (Figures 20, 22, 24) | - | -0.503 - j15 | - | - | -0.503 - j15 | - | mS |
| | | | Diff. Amp. (Figures 21, 23, 25) | - | 0.071 + j0.62 | - | - | 0.071 + j0.62 | - | mS |

NOTES:

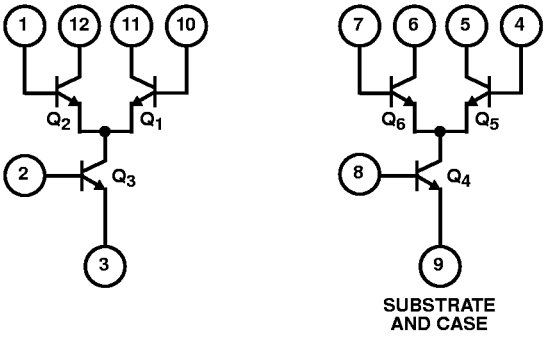
3. Terminals 1 and 14 or 7 and 8 (CA3102). Terminals 1 and 12 or 6 and 7 (CA3049T).
4. Terminals 13 and 4 or 6 and 11 (CA3102). Terminals 10 and 11 or 4 and 5 (CA3049T).

## Schematic Diagrams

**CA3102E, CA3102M**




**CA3049T**



## Test Circuits

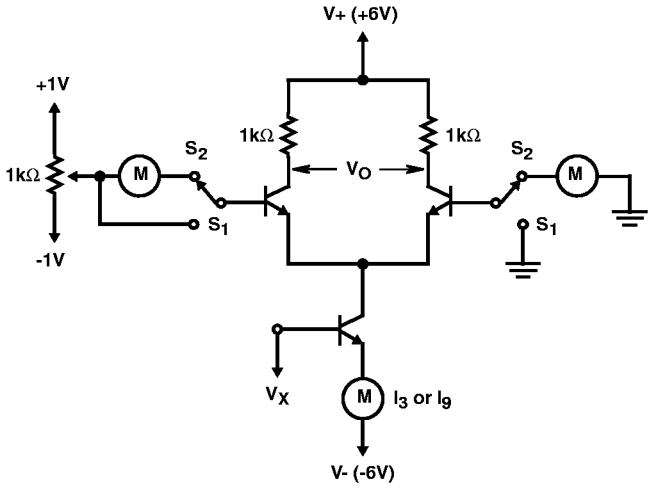



FIGURE 1. DC CHARACTERISTICS TEST CIRCUIT FOR CA3102

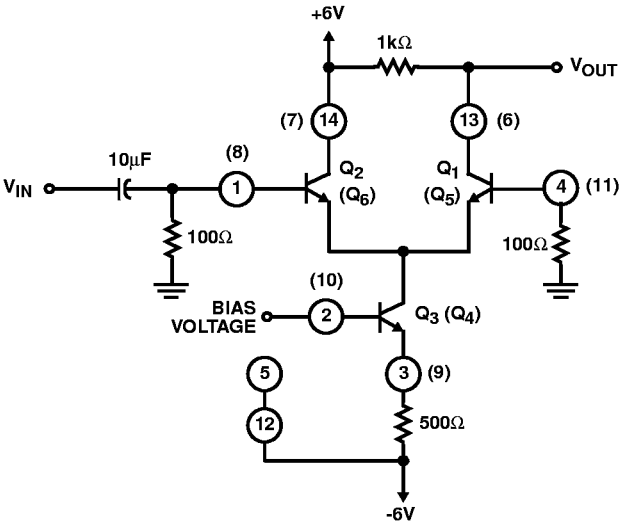
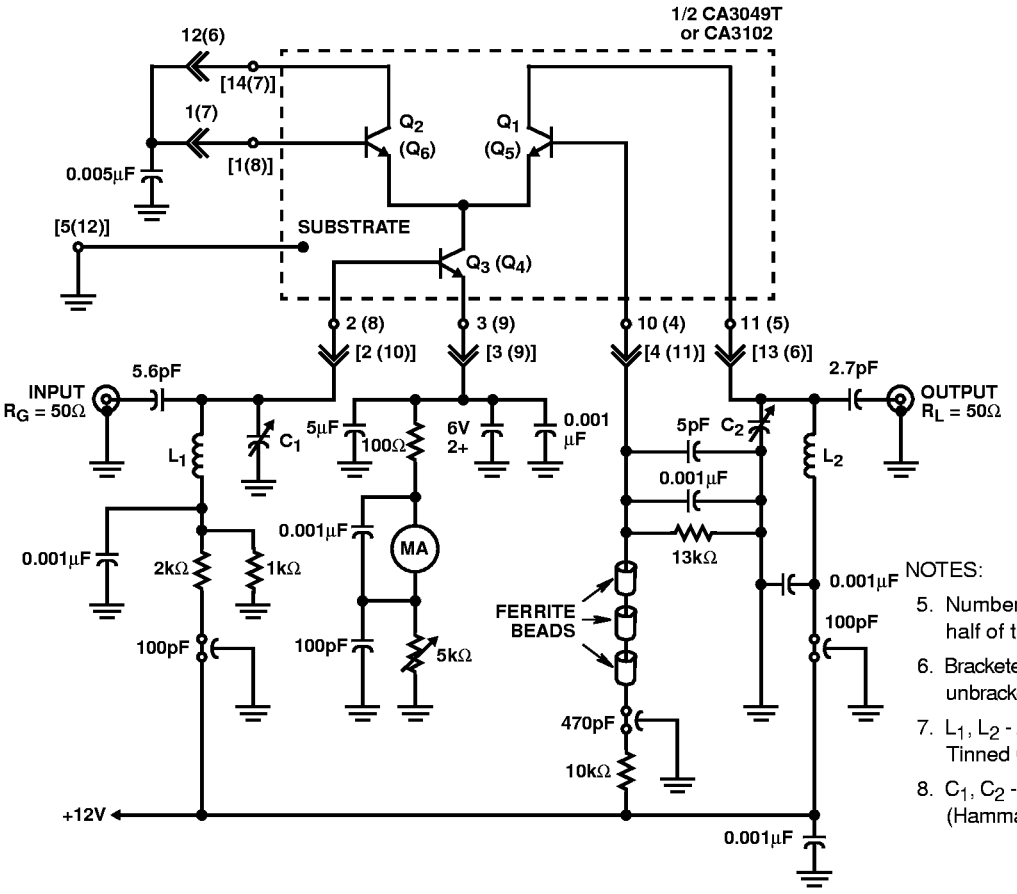



FIGURE 2. AGC RANGE AND VOLTAGE GAIN TEST CIRCUIT FOR CA3102




NOTES:

5. Numbers in parentheses refer to other half of the CA3049T or CA3102.
6. Bracketed numbers refer to CA3102, unbracketed numbers refer to CA3049T.
7. $L_1$, $L_2$ - Approximately $^1/_2$ Turn #18 Tinned Copper Wire, 5/8" Diameter.
8. $C_1$, $C_2$ - 15pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent).

FIGURE 3. 200MHz CASCODE POWER GAIN AND NOISE FIGURE TEST CIRCUIT

## Typical Performance Curves

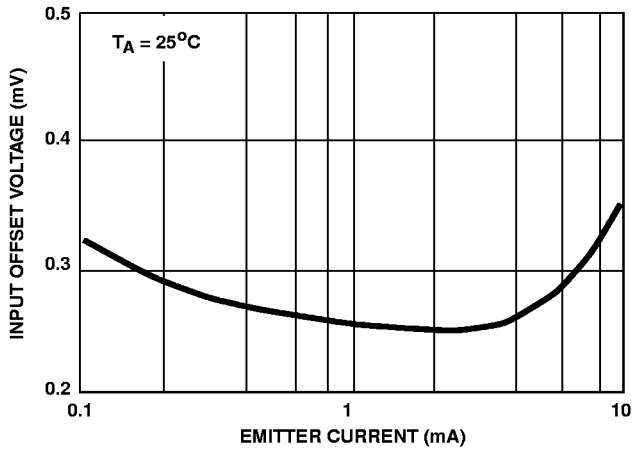



FIGURE 4. INPUT OFFSET VOLTAGE vs EMITTER CURRENT

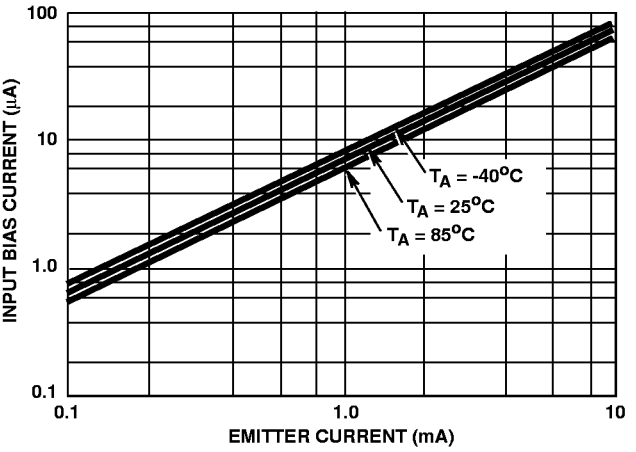



FIGURE 5. INPUT BIAS CURRENT vs EMITTER CURRENT

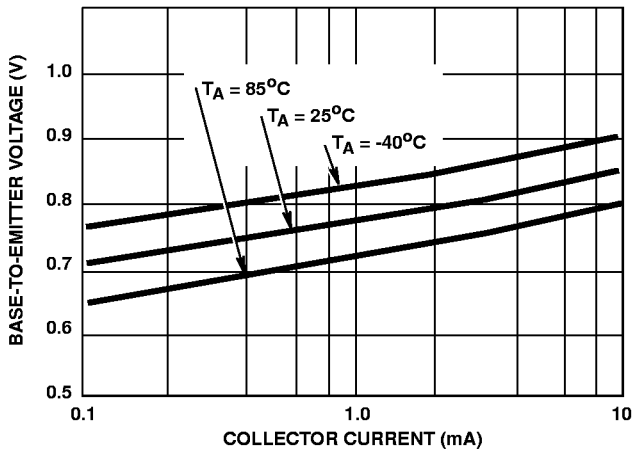



FIGURE 6. BASE-TO-EMITTER VOLTAGE vs COLLECTOR CURRENT

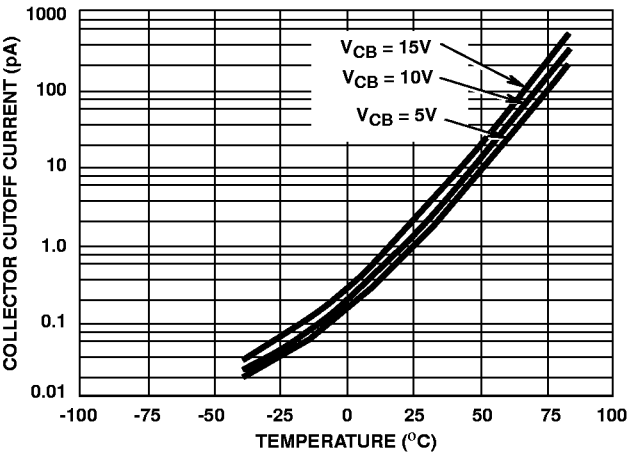



FIGURE 7. COLLECTOR CUTOFF CURRENT vs TEMPERATURE

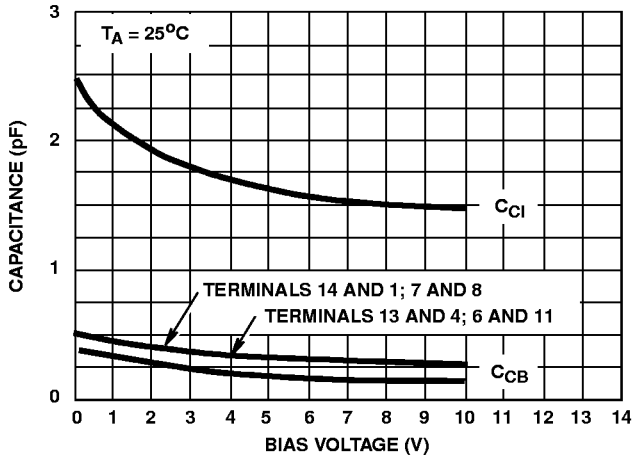



FIGURE 8. CAPACITANCE vs DC BIAS VOLTAGE

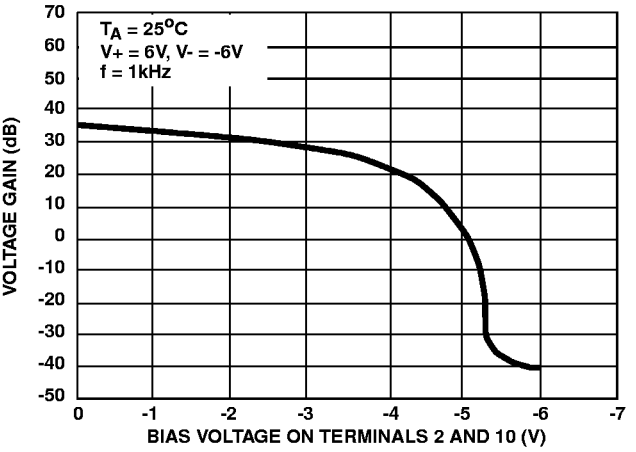



FIGURE 9. VOLTAGE GAIN vs DC BIAS VOLTAGE

## Typical Performance Curves (Continued)

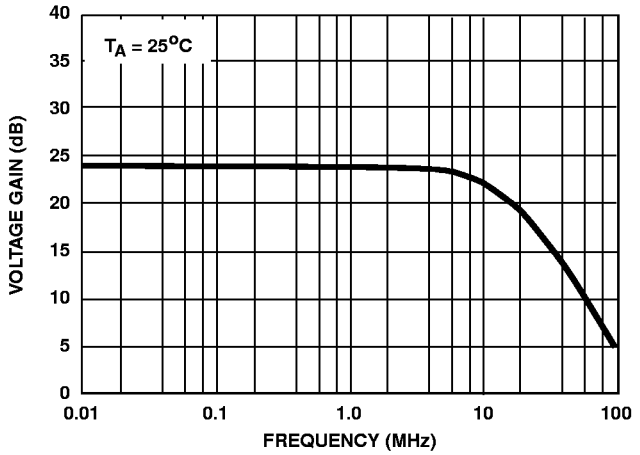



FIGURE 10. VOLTAGE GAIN vs FREQUENCY

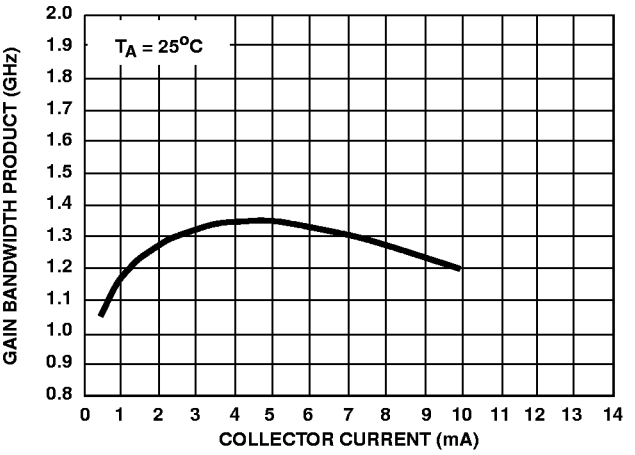



FIGURE 11. GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT

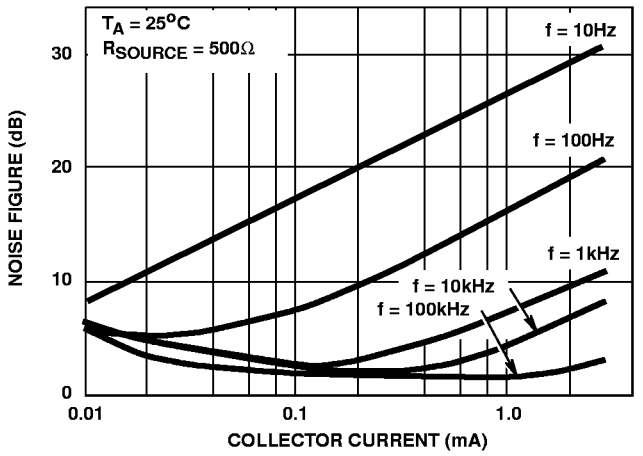



FIGURE 12. 1/f NOISE FIGURE vs COLLECTOR CURRENT

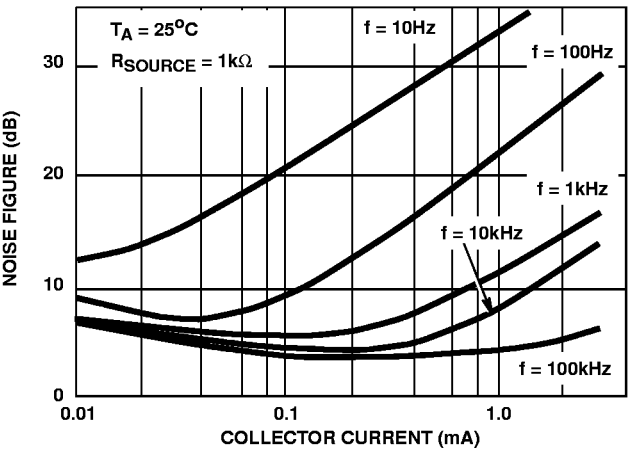



FIGURE 13. 1/f NOISE FIGURE vs COLLECTOR CURRENT

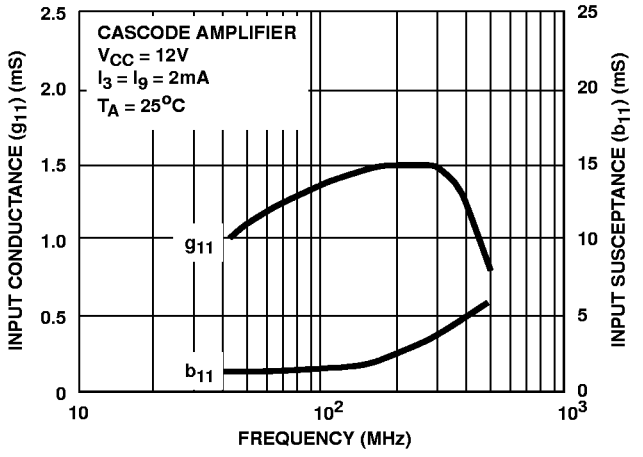



FIGURE 14. INPUT ADMITTANCE ($Y_{11}$) vs FREQUENCY

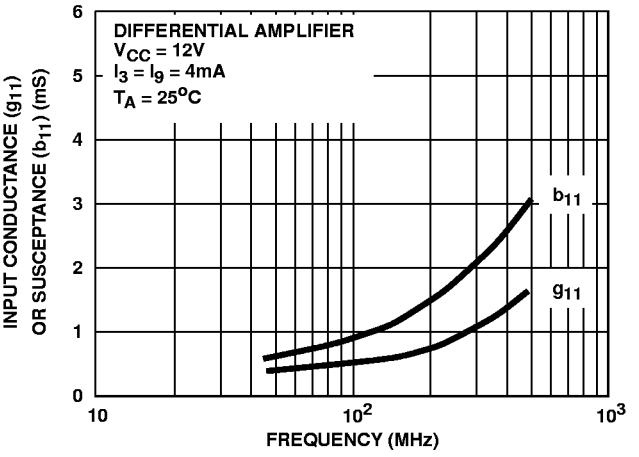



FIGURE 15. INPUT ADMITTANCE ($Y_{11}$) vs FREQUENCY

## Typical Performance Curves (Continued)

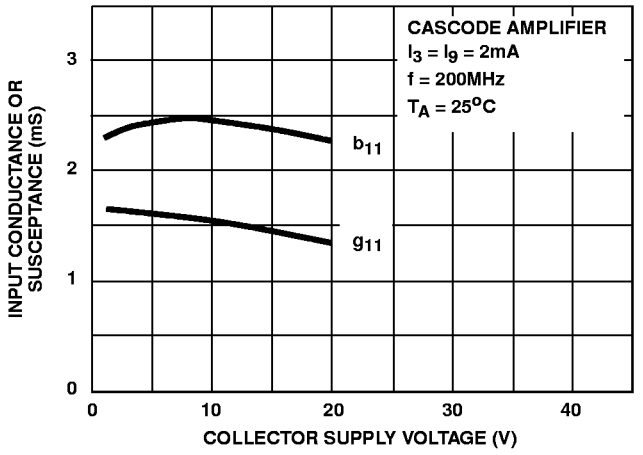



FIGURE 16. INPUT ADMITTANCE ($Y_{11}$) vs COLLECTOR SUPPLY VOLTAGE

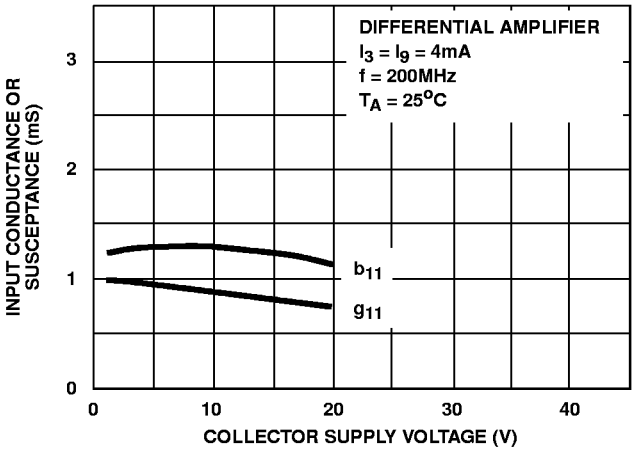



FIGURE 17. INPUT ADMITTANCE ($Y_{11}$) vs COLLECTOR SUPPLY VOLTAGE

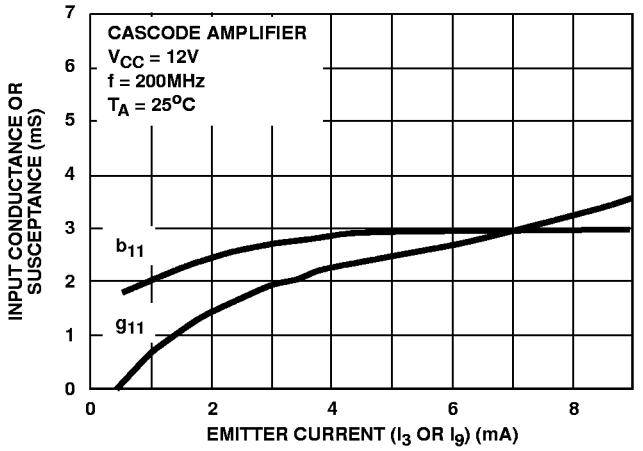



FIGURE 18. INPUT ADMITTANCE ($Y_{11}$) vs EMITTER CURRENT

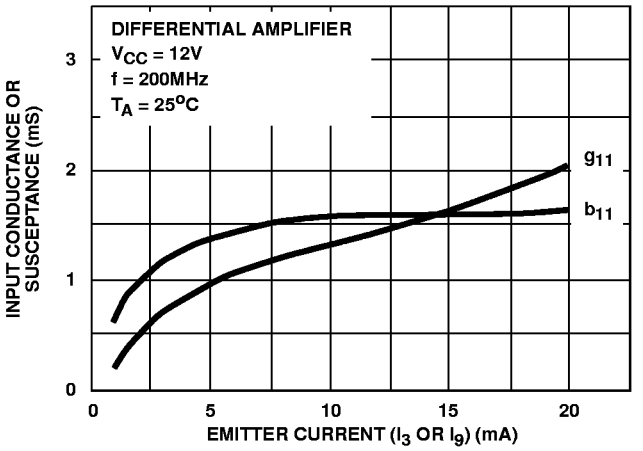



FIGURE 19. INPUT ADMITTANCE ($Y_{11}$) vs EMITTER CURRENT

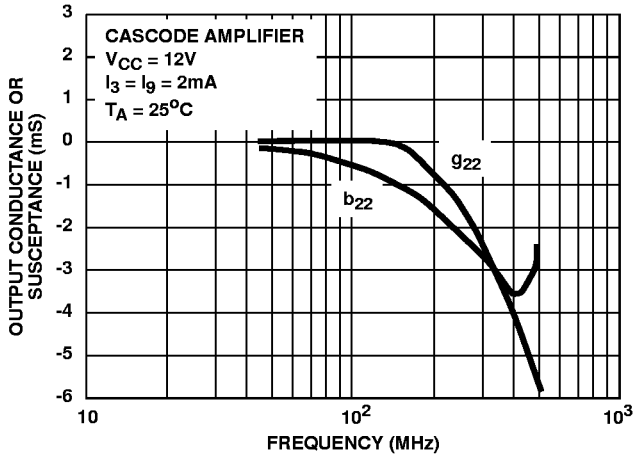



FIGURE 20. OUTPUT ADMITTANCE ($Y_{22}$) vs FREQUENCY

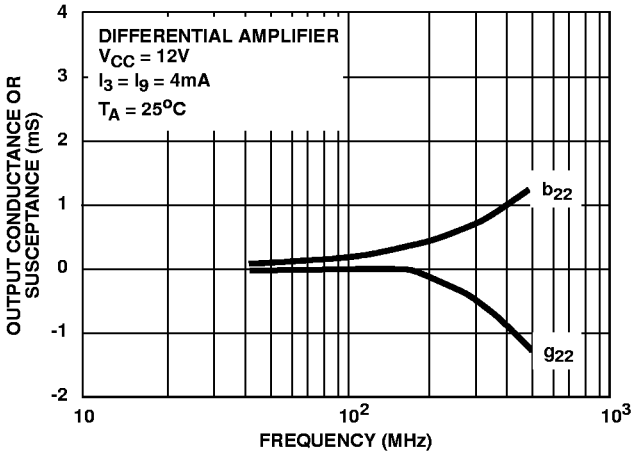



FIGURE 21. OUTPUT ADMITTANCE ($Y_{22}$) vs FREQUENCY

## Typical Performance Curves (Continued)

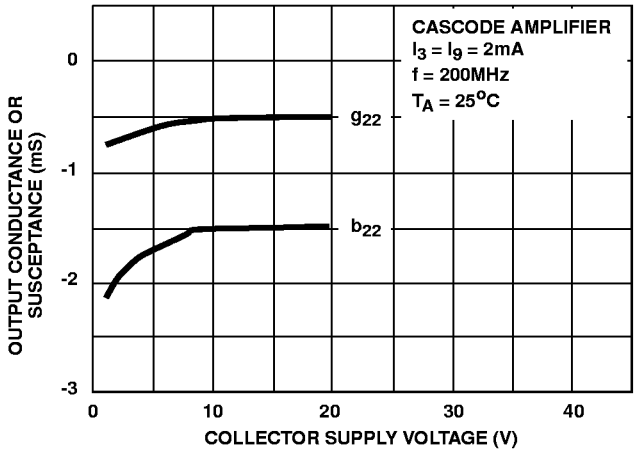



FIGURE 22. OUTPUT ADMITTANCE ($Y_{22}$) vs COLLECTOR SUPPLY VOLTAGE

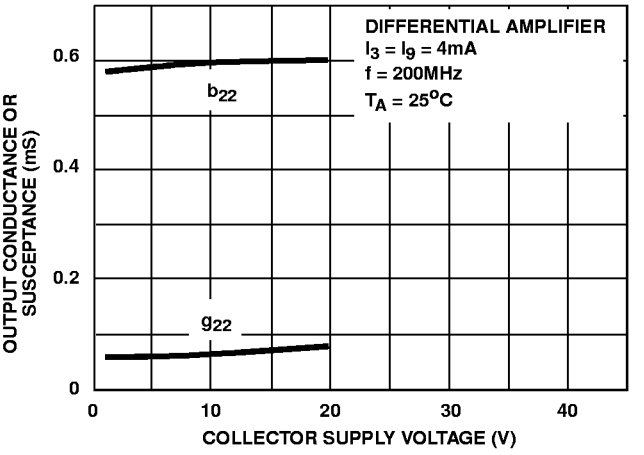



FIGURE 23. OUTPUT ADMITTANCE ($Y_{22}$) vs COLLECTOR SUPPLY VOLTAGE

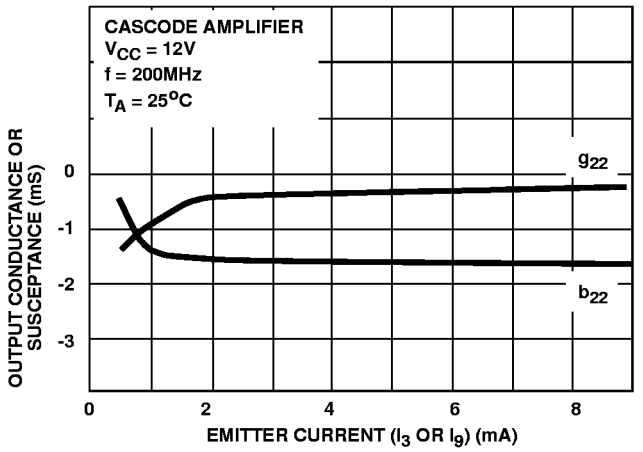



FIGURE 24. OUTPUT ADMITTANCE ($Y_{22}$) vs EMITTER CURRENT

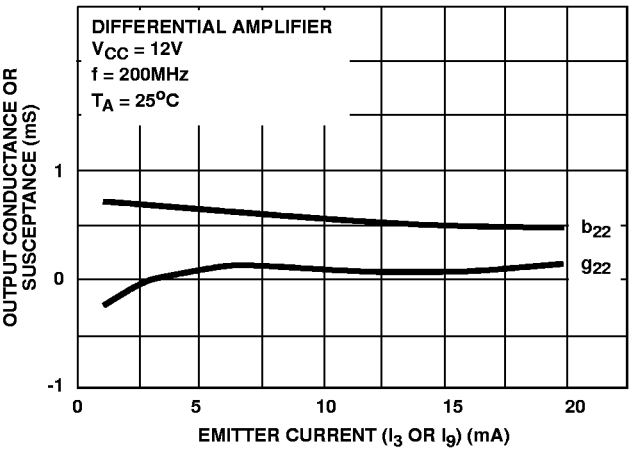



FIGURE 25. OUTPUT ADMITTANCE ($Y_{22}$) vs EMITTER CURRENT

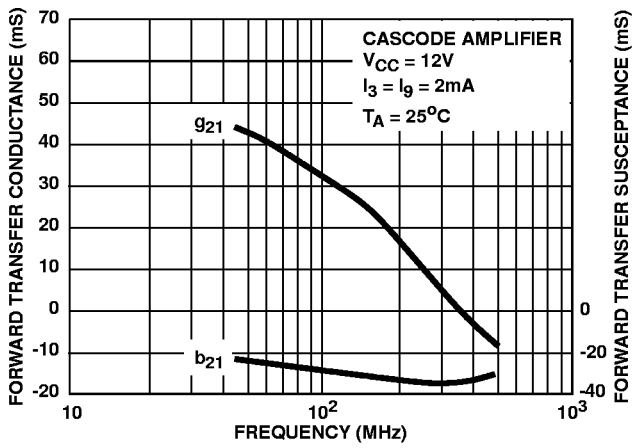



FIGURE 26. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs FREQUENCY

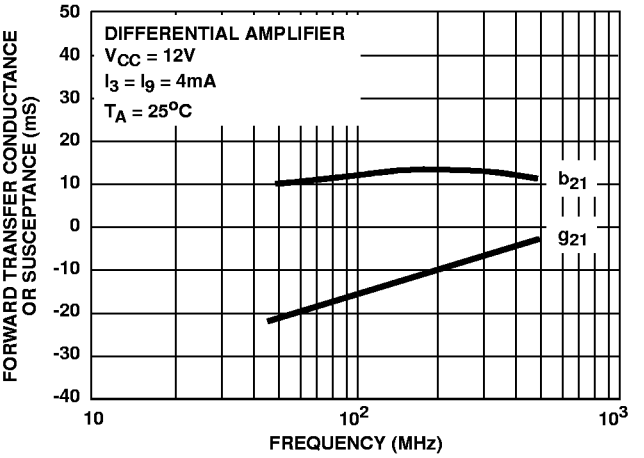



FIGURE 27. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs FREQUENCY

## Typical Performance Curves (Continued)

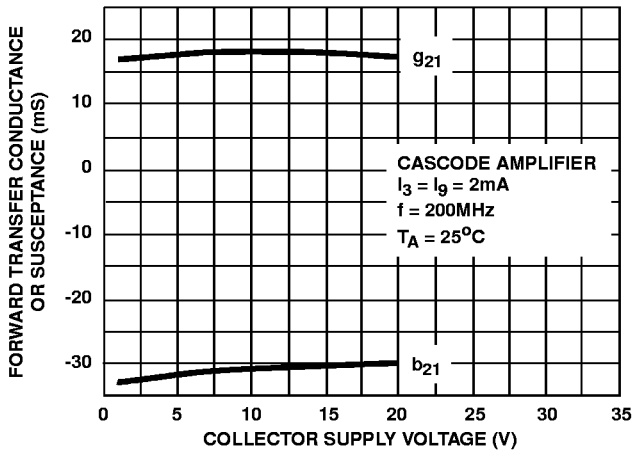



FIGURE 28. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs COLLECTOR SUPPLY VOLTAGE

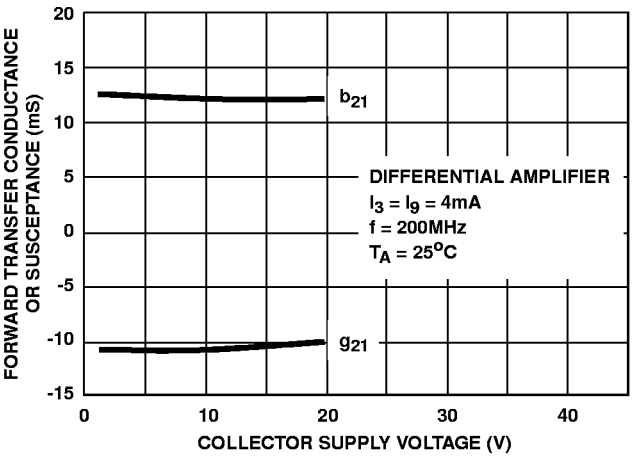



FIGURE 29. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs COLLECTOR SUPPLY VOLTAGE

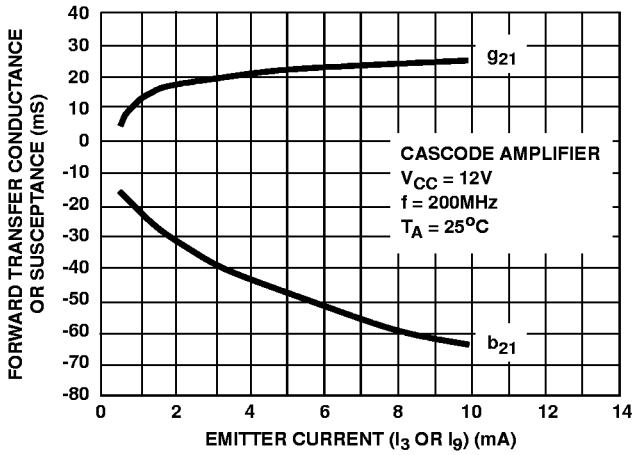



FIGURE 30. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs EMITTER CURRENT

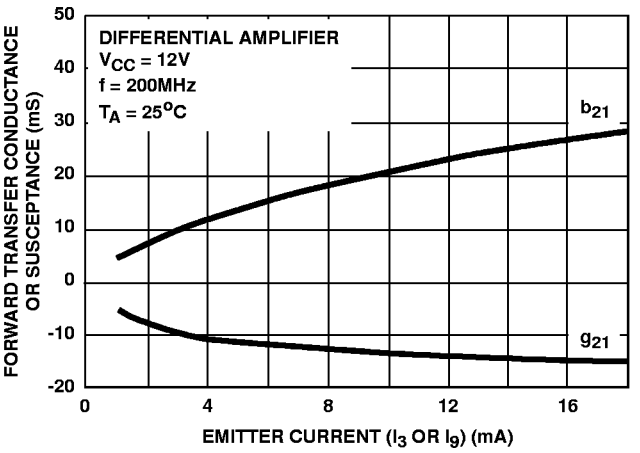



FIGURE 31. FORWARD TRANSFER ADMITTANCE ($Y_{21}$) vs EMITTER CURRENT