A4992

Automotive Stepper Driver

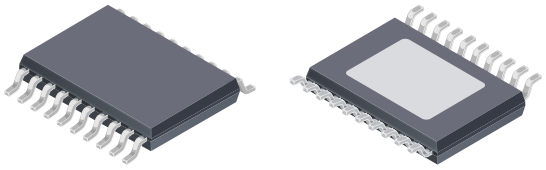
FEATURES AND BENEFITS

- Low $R_{DS(on)}$ outputs, 0.5 Ω source and sink typical
- Continuous operation at high ambient temperature
- 3.5 to 50 V supply operation
- Adaptive mixed current decay
- Synchronous rectification for low power dissipation
- Internal overvoltage and undervoltage lockout
- Hot warning and overtemperature shutdown
- Crossover-current protection
- Short circuit and open load diagnostics
- Stall detect features
- Configurable through serial interface

APPLICATIONS:

- Automotive stepper motors
- Engine management
- Headlamp positioning

PACKAGE: 20-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

The A4992 is a flexible microstepping motor driver with integrated phase current control and a built-in translator for easy operation. It is a single chip solution designed to operate bipolar stepper motors in full, half, quarter, eighth, and sixteenth step modes, at up to 28 V. At power-on, the A4992 is configured to drive most small stepper motors with simple step and direction inputs.

The current regulator operates with fixed frequency PWM. It uses adaptive mixed current decay to reduce audible motor noise and increase step accuracy.

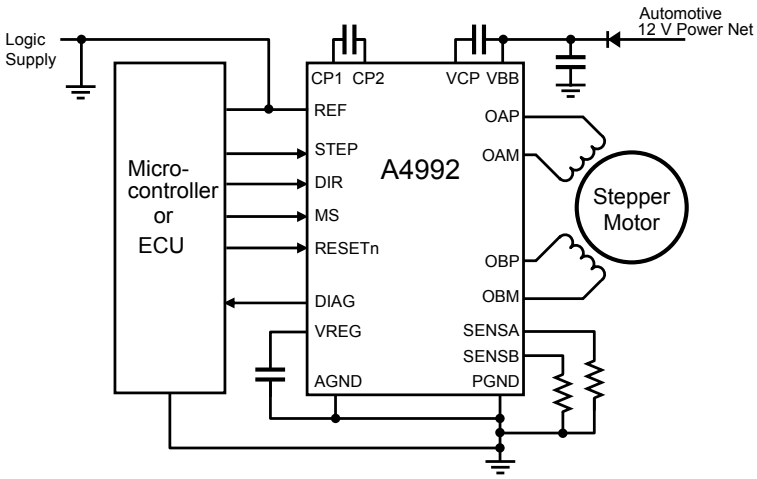
The current in each phase of the motor is controlled through a DMOS full bridge using synchronous rectification to improve power dissipation. Internal circuits and timers prevent cross-conduction and shoot-through when switching between high-side and low-side drives.

The outputs are protected from short circuits. Features for low load current and stalled rotor detection are included. Chip-level protection includes hot thermal warning, overtemperature shutdown, and overvoltage and undervoltage lockout.

An optional serial interface mode, using the STEP, DIR, and MS inputs, can be used to configure several motor control parameters and diagnostics.

The A4992 is supplied in a 20-pin TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin lead frame plating.

Typical Application Diagram



SELECTION GUIDE

Part Number	Packing*	Package
A4992KLPTR-T	4000 pieces per 13-in. reel	4.4 mm × 6.5 mm, 1.2 mm nominal height 20-pin TSSOP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS with respect to PGND

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
Pin CP1			–0.3 to V_{BB}	V
Pin CP2, VCP			–0.3 to V_{BB} + 8	V
Pins STEP, DIR, MS			–0.3 to 6	V
Pin VREG			–0.3 to 8.5	V
Pin RESETn		Can be pulled to VBB with 38 kΩ	–0.3 to 6	V
Pin DIAG			–0.3 to 6	V
Pin REF			–0.3 to 6	V
Pins OAP, OAM, OBP, OBM			–0.3 to V_{BB}	V
Pin SENSA, SENSB			–0.3 to 1	V
Pin AGND			–0.1 to 0.1	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, ensured by design and characterization.	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Estimated, on 4-layer PCB based on JEDEC standard	29	°C/W

*Additional thermal information available on the Allegro website.

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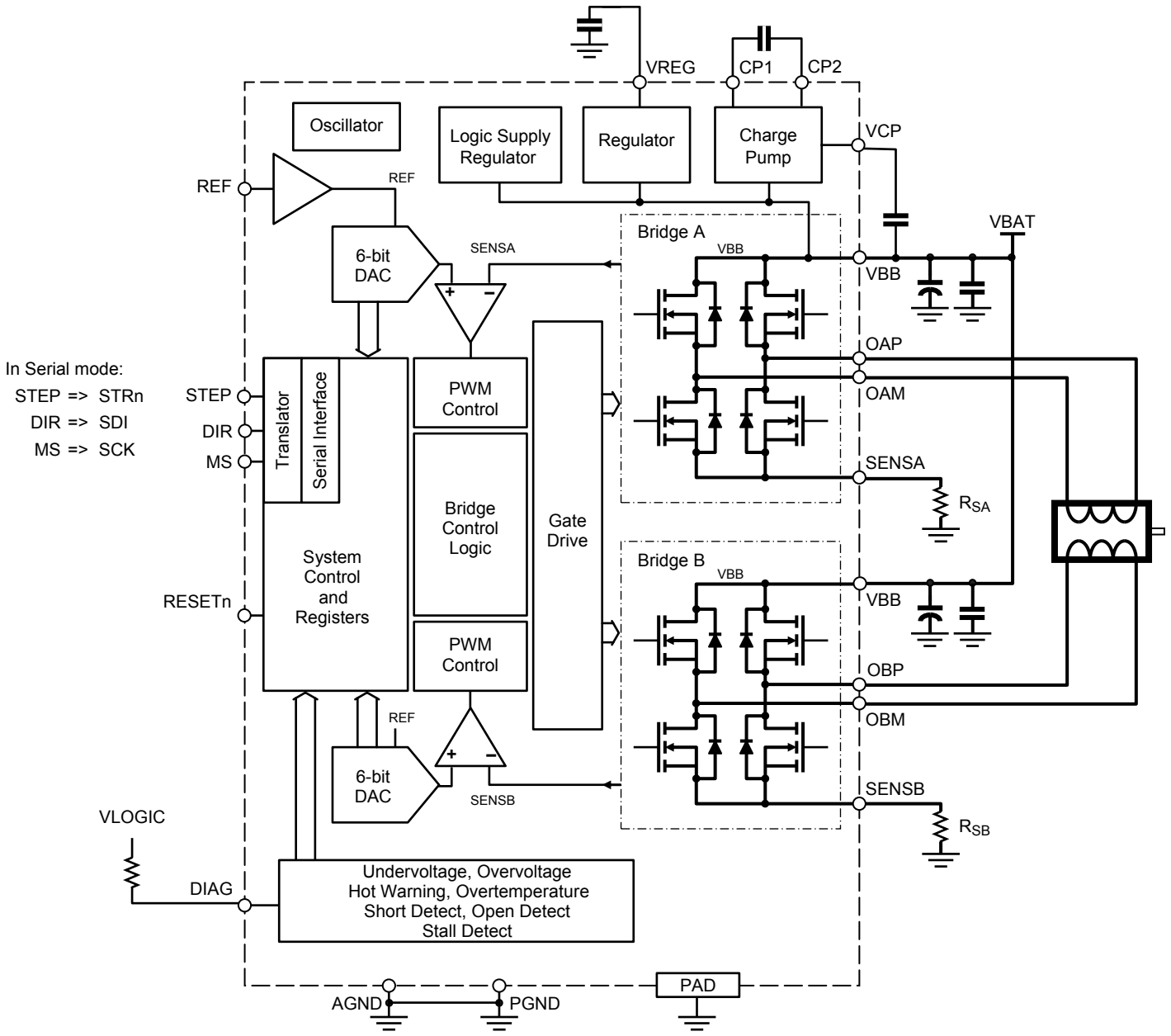

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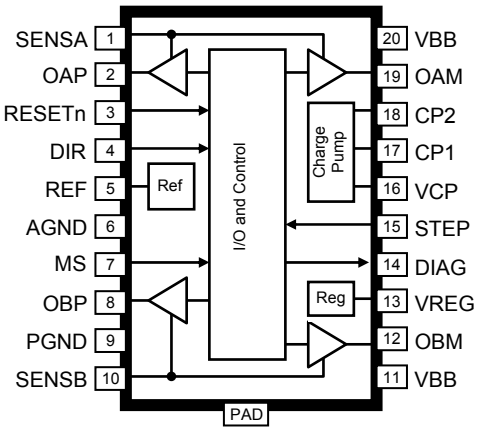
Pinout Diagram



Terminal List Table

Name	Number	Function
AGND	6	Analog reference ground
CP1	17	Charge pump capacitor
CP2	18	Charge pump capacitor
DIAG	14	Diagnostic output, active low (inverted for serial transfer acknowledgement)
DIR	4	Direction select input (SDI in Serial mode: serial word input)
MS	7	Microstep select input (SCK in Serial mode: serial clock input)
OAP	2	Bridge A positive output
OAM	19	Bridge A negative output
OBP	8	Bridge B positive output
OBM	12	Bridge B negative output
PAD	–	Exposed thermal pad
PGND	9	Power ground
REF	5	Reference input voltage
RESETn	3	Chip reset, active low
SENSA	1	Current sense node – bridge A
SENSB	10	Current sense node – bridge B
STEP	15	Step input (STRn in Serial mode: active low serial data strobe and serial access enable input)
VBB	11	Motor supply voltage
VBB	20	Motor supply voltage
VCP	16	Pump storage capacitor
VREG	13	Regulated voltage

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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 28 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLIES						
Supply Voltage Range [1]	V_{BB}	Functional, no unsafe states	0	–	50	V
		Outputs driving	3.8	–	V_{BBOV}	V
Supply Quiescent Current	I_{BBQ}	DIS = 1	–	–	15	mA
		RESETn < 0.5 V	–	1	10	µA
Charge Pump Voltage	V_{CP}	With respect to VBB, V_{BB} >7.5 V, DIS=1, RESETn = 1	–	6.7	–	V
Internal Regulator Voltage	V_{REG}	DIS = 1, RESETn = 1, V_{BB} >7.5 V	–	7.2	–	V
Internal Regulator Dropout Voltage	V_{REGDO}	DIS = 1, RESETn = 1, V_{BB} > 6 V	–	100	200	mV
MOTOR BRIDGE OUTPUT						
High-Side On-Resistance [2]	$R_{DS(on)H}$	V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = –1 A, T_J = 25°C	–	625	750	mΩ
High-Side Body Diode Forward Voltage	V_{fH}	I_f = 1 A	–	–	1.4	V
Low-Side On-Resistance	$R_{DS(on)L}$	V_{BB} =13.5 V, I_{OUT} = 1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = 1 A, T_J = 25°C	–	625	750	mΩ
Low-Side Body Diode Forward Voltage [2]	V_{fL}	I_f = –1 A	–	–	1.4	V
Output Leakage Current [2]	$I_{OUT(Lkg)}$	DIS = 1, RESETn = 1, V_{OUT} = V_{BB}	–120	–65	–	µA
		DIS = 1, RESETn = 1, V_{OUT} = 0 V	–200	–120	–	µA
		DIS = 1, RESETn = 0, V_{OUT} = V_{BB}	–	< 1.0	20	µA
		DIS = 1, RESETn = 0, V_{OUT} = 0 V	–20	< 1.0	–	µA
CURRENT CONTROL						
Internal Oscillator Frequency	f_{OSC}		3.6	4	4.4	MHz
Blank Time [3]	t_{BLANK}	Default blanking time	–	3.5	–	µs
PWM Frequency [3]	f_{PWM}	Default frequency	–	21.7	–	kHz
Reference Input Voltage	V_{REF}		0.8	–	2	V
Internal Reference Voltage	V_{REFint}	V_{REF} > 2.5 V	1.1	1.2	1.3	V
Reference Input Current [2]	I_{REF}		–3	0	3	µA
Maximum Sense Voltage	V_{SMAX}		–	125	–	mV
Current Trip Point Error [4]	E_{ITrip}	V_{REF} = 2 V	–	–	±5	%

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUT AND OUTPUT – DC PARAMETERS						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input Low Voltage for Sleep Mode	V_{ILS}	RESETn input only	–	–	0.5	V
Input High Voltage	V_{IH}		2.0	–	–	V
Input Hysteresis	V_{IHys}		100	300	–	mV
Input Pull-Down Resistor	R_{PD}		–	50	–	k□Ω
Output Low Voltage	V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
Output Leakage[2]	$I_{O(Lkg)}$	0 V < V_O < 5 V	–1	–	1	µA
LOGIC INPUT AND OUTPUT – DYNAMIC PARAMETERS (SEE FIGURES 1 AND 4)						
Reset Pulse Width	t_{RST}		1	–	6	µs
Reset Shutdown Pulse Width	t_{RSD}		40	–	–	µs
Input Pulse Filter Time	t_{PIN}	STEP, DIR	–	80	–	ns
STEP High	t_{STPL}		1	–	–	µs
STEP Low	t_{STPH}		1	–	–	µs
Setup Time	t_{SU}	MS, DIR; from control input change to STEP change	200	–	–	ns
Hold Time	t_H	MS, DIR; from STEP change to control input change	200	–	–	ns
Wake-Up from Reset	t_{EN}		–	–	1	ms
SERIAL INTERFACE – DYNAMIC PARAMETERS (SEE FIGURES 2 AND 3)						
Clock High Time	t_{SCKH}	Reference A	50	–	–	ns
Clock Low Time	t_{SCKL}	Reference B	50	–	–	ns
Strobe Lead Time	t_{STLD}	Reference C	30	–	–	ns
Strobe Lag Time	t_{STLG}	Reference D	30	–	–	ns
Strobe High Time	t_{STRH}	Reference E	1100	–	–	ns
Data In Setup Time to Clock Rising	t_{SDIS}	Reference F	15	–	–	ns
Data In Hold Time from Clock Rising	t_{SDIH}	Reference G	10	–	–	ns
INTERFACE MODE SWITCH TIMING (SEE FIGURES 3 THROUGH 5)						
Sequence Minimum Hold Time	t_{SSH}	Reference H	58	64.5	72	µs
Serial Mode Exit Time	t_{SSEX}	Reference J	–	–	2	µs
Serial Mode Acknowledge Time	t_{SAT}	Reference K	59	65.5	73	µs
Serial Mode Acknowledge Pulse	t_{SAP}	Reference L; consistent fault status	921	1024	1127	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VBB Overvoltage Threshold	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis	$V_{BBOVHys}$		2	–	4	V
VBB Undervoltage Threshold	V_{BBUV}	V_{BB} falling	5.2	5.5	5.8	V
VBB Undervoltage Hysteresis	$V_{BBUVHys}$		500	760	–	mV
VBB Power-On Reset Threshold	V_{BBPOR}	V_{BB} falling	–	2.8	3.0	V
VBB Power-On Reset Hysteresis	$V_{BBPORHys}$		50	100	–	mV
VREG Undervoltage Threshold – High	V_{REGUVH}	V_{REG} falling	4.6	4.8	4.95	V
VREG Undervoltage Hysteresis–High	$V_{REGUVHHys}$		250	370	–	mV
VREG Undervoltage Threshold – Low	V_{REGUVL}	V_{REG} falling	3.2	3.35	3.5	V
VREG Undervoltage Hysteresis – Low	$V_{REGUVLHys}$		100	230	–	mV
High-Side Overcurrent Threshold	I_{OCH}	Sampled after t_{SCT}	1.4	2.05	2.65	A
High-Side Current Limit	I_{LIMH}	Active during t_{SCT}	3	5.5	8	A
Low-Side Overcurrent Sense Voltage	V_{OCL}	Sampled after t_{SCT}	210	250	290	mV
Overcurrent Fault Delay	t_{SCT}	Default fault delay	1500	2000	2700	ns
Open Load Current Threshold Error	E_{IOC}	V_{REF} = 2 V	–	–	±10	%
Hot Temperature Warning Threshold	T_{JWH}	Temperature increasing	125	135	145	°C
Hot Temperature Warning Hysteresis	T_{JWHHys}		–	15	–	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing	155	170	–	°C
Overtemperature Hysteresis	T_{JHys}	Recovery = $T_{JF} – T_{JHys}$	–	15	–	°C

[1] The term *functional* indicates operation is correct but parameters may not be within specification above or below the general limits (7 to 28 V). Outputs not operational above V_{BBOV} or below V_{REGUVL}.
[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[3] Assumes a 4 MHz clock.
[4] Current Trip Point Error is the difference between the actual current trip point and the target current trip point, referred to maximum full scale (100%) current: $E_{Trip} = 100 \times (I_{TripActual} – I_{TripTarget}) / I_{FullScale\%}$.

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Interface Timing Diagrams

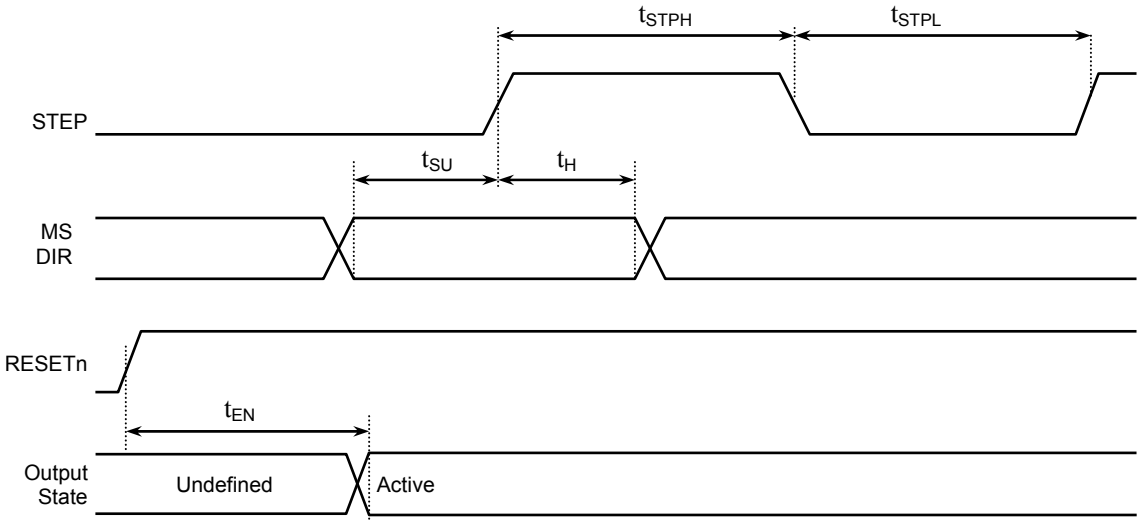

Figure 1. Control Input Timing

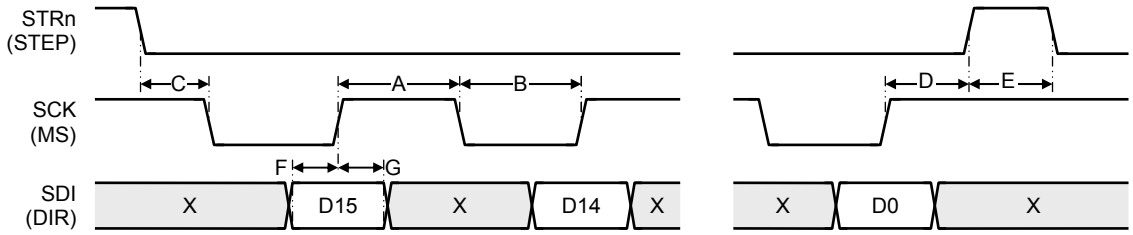

Figure 2. Serial Data Timing

X=don't care

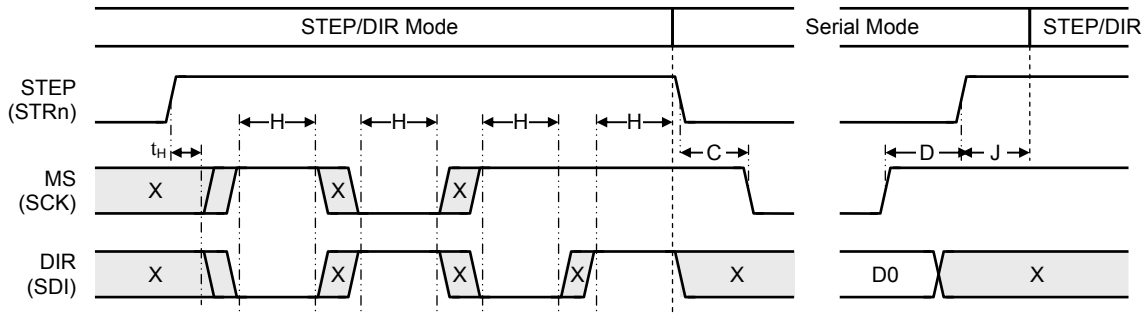

Figure 3. Interface Mode Change Timing

X=don't care

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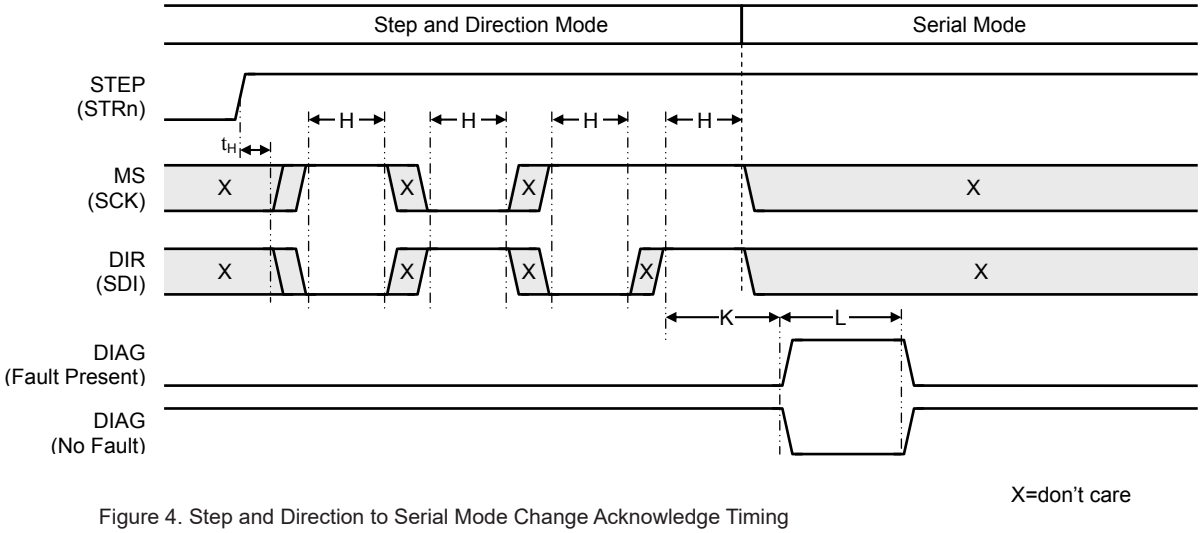

Figure 4. Step and Direction to Serial Mode Change Acknowledge Timing

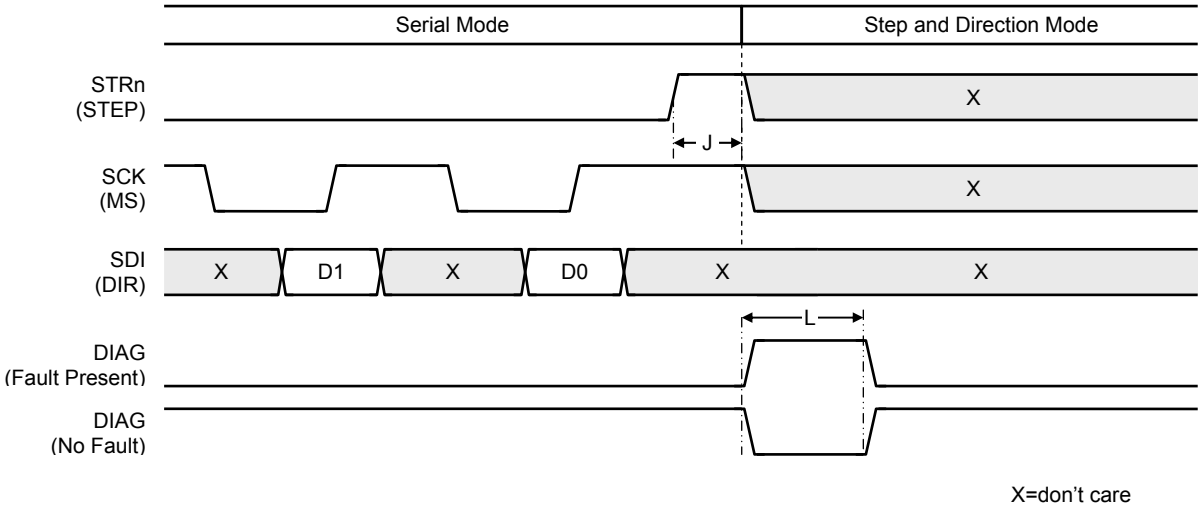

Figure 5. Serial to Step and Direction Mode Change Acknowledge Timing

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FUNCTIONAL DESCRIPTION

The A4992 is an automotive stepper motor driver suitable for high temperature applications such as headlamp bending and levelling, throttle control, and gas recirculation control. It is also suitable for other low current stepper applications such as air conditioning and venting. It provides a flexible microstepping motor driver controlled with simple step and direction inputs. It can also be switched into an optional serial interface mode, where it can be configured and driven via an SPI compatible serial interface.

The two DMOS full-bridges are capable of driving bipolar stepper motors in full-, half-, quarter-, eighth-, and sixteenth-step modes, at up to 28 V, with phase current up to ±1.4 A but limited by power dissipation and ambient temperature. For most applications typical phase current is up to ±750 mA. The current in each phase of the stepper motor is regulated by a fixed-frequency peak-detect PWM current control scheme operating in an adaptive mixed decay mode. This provides reduced audible motor noise and increased step accuracy for a wide range of motors and operating conditions.

The outputs are protected from short circuits and features for open load and stalled rotor detection are included. Chip level protection includes hot thermal warning, overtemperature shutdown, and overvoltage and undervoltage lockout.

Pin Functions

VBB Main motor supply and chip supply for internal regulators and charge pump. Both VBB pins should be connected together and each decoupled to ground with a low ESR electrolytic capacitor and a good ceramic capacitor.

CP1, CP2 Pump capacitor connection for charge pump. Connect a 100 nF (50 V) ceramic capacitor, between CP1 and CP2.

VCP Above supply voltage for high-side drive. A 100 nF (16 V) ceramic capacitor should be connected between VCP and VBB to provide the pump storage reservoir.

VREG Regulated supply for bridge gate drive. Should be decoupled to ground with a 470 nF (10V) ceramic capacitor.

AGND Analog reference ground. Quiet return for measurement and input references. Connect to PGND. See recommendations in Layout section.

PGND Digital and power ground. Connect to supply ground and AGND. See recommendations in Layout section.

OAP, OAM Motor connection for phase A. Positive motor phase current direction is defined as flowing from OAM to OAP.

OBP, OBM Motor connection for phase B. Positive motor phase current direction is defined as flowing from OBM to OBP.

SENSA Phase A current sense. Connect sense resistor between SENSA and PGND.

SENSB Phase B current sense. Connect sense resistor between SENSB and PGND.

REF Reference input to set absolute maximum current level for both phases. Defaults to internal reference when driven higher than 2.5 V.

STEP (STRn) Step logic input with internal pull-down resistor. Motor advances on rising edge. In serial mode, STEP pin takes on the functions of STRn, the serial data strobe and serial access enable input. When STRn is high any activity on MS (SCK function) or DIR (SDI function) is ignored.

DIR (SDI) Direction logic input with internal pull-down resistor. Direction changes on next STEP rising edge. When DIR is high the phase angle number is incremented by one on each rising edge of STEP. In serial mode, DIR takes on the function of SDI, the serial data input, accepting a 16-bit serial word input, with MSB first.

MS (SCK) Microstep resolution select input with internal pull-down resistor. In serial mode, MS takes on the function of SCK, the serial clock input. Data is latched in from DIR (SDI function) on the rising edge of SCK. There must be 16 rising edges per write and MS (SCK) must be held high when STEP (STRn) changes.

RESETn Resets faults when pulsed low. Forces low-power shutdown (sleep mode) when held low for more than the reset shutdown width, t_{RSD}. Can be pulled to VBB with 38 kΩ resistor.

DIAG Diagnostic open drain output, active low. Low indicates the presence of a fault. External pull-up resistor required.

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Driving a Stepper Motor

A two-phase stepper motor is made to rotate by sequencing the relative currents in each phase. In its simplest form each phase is simply fully energized in turn by applying a voltage to the winding. For more precise control of the motor torque across temperature and voltage ranges, current control is required. For efficiency this is usually accomplished using PWM techniques. In addition, current control also allows the relative current in each phase to be controlled providing more precise control over the motor movement and hence improvements in torque ripple and mechanical noise.

For bipolar stepper motors the current direction is significant so the voltage applied to each phase must be reversible. This requires the use of a full-bridge (also known as an H-bridge) which can switch each phase connection to supply or ground.

Phase Current Control

In the A4992, current to each phase of the two-phase bipolar stepper motor is controlled through a low impedance N-channel DMOS full bridge. This allows efficient and precise control of the phase current using fixed-frequency pulse width modulation (PWM) switching. The full-bridge configuration provides full control over the current direction during the PWM on-time and the current decay mode during the PWM off-time. The A4992 automatically controls the bridge decay mode to provide the optimum current control completely transparent to the user.

Each leg (high-side, low-side pair) of a bridge is protected from shoot-through by a fixed dead time. This is the time between switching off one FET and switching on the complementary FET. Cross-conduction is prevented by lockout logic in each driver pair.

The phase currents and in particular the relative phase currents are defined by the on-board phase current table, which is shown here in table 3. This table defines the two phase currents at each microstep position. For each of the two phases, the current is measured using a sense resistor, R_{Sx}, with voltage feedback to the respective SENSx pin. The sense voltage is amplified by a fixed gain and compared to the output of the digital-to-analog converter (DAC) for that phase. The target current level is then defined by the voltage from the DAC.

The maximum phase current, I_{SMAX}, is defined by the sense resistor and the reference input as:

$$I_{SMAX} = V_{REF} / (16 \times R_{Sx})$$

where V_{REF} is the voltage at the REF pin and R_{Sx} is value of the sense resistor for that phase.

The actual current delivered to each phase at each step angle is determined by the value of I_{SMAX} and the contents of the phase current table. For each phase, the value in the phase current table is passed to the DAC, which uses I_{SMAX} as the reference 100% level (code 63) and reduces the current target depending on the DAC code. The output from the DAC is used as the input to the current comparators.

The current comparison is ignored at the start of the PWM on-time for a duration referred to as the *blank time*. The blank time is necessary to prevent any capacitive switching currents from causing a peak current detection.

The PWM on-time starts at the beginning of each PWM period. The current rises in the phase winding until the sense voltage reaches the threshold voltage for the required current level. At this point the PWM off-time starts and the bridge is switched into fast decay. The sense voltage continues to be monitored. When the sense voltage drops below the threshold voltage the bridge is switched into slow decay for the remainder of the PWM period. This mixed decay technique automatically adapts the current control to a wide range of motors and operating conditions in order to minimize motor torque ripple and motor noise. It also provides the lowest motor power dissipation and the highest motor efficiency across a wide range of voltage and temperature conditions.

Step Angle and Direction Control

The relative phase currents are defined by the on-board phase current table (see table 3). This table contains 64 lines and is addressed by the step angle number, where step angle 0 corresponds to 0° or 360°. The step angle number is generated internally by the step sequencer, which is controlled either by the STEP and DIR inputs or by the step change value from the serial input. The step angle number determines the motor position within the 360° electrical cycle and a sequence of step angle numbers determines the motor movement. Note that there are four full mechanical steps per 360° electrical cycle.

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Each line of the phase current table has a 6-bit value, per phase, to set the DAC level for each phase plus an additional bit, per phase, to determine the current direction in each phase. The step angle number sets the electrical angle of the stepper motor in sixteenth microsteps, approximately equivalent to electrical steps of 5.625°.

On first power-up or after a power-on reset, the step angle number is set to 8, equivalent to the electrical 45° position. This position is referred to as the *home* position. The maximum current in each phase, I_{SMAX}, is defined by the sense resistor and the voltage at the REF pin, as described in the Phase Current Control section, above. The phase currents for each entry in the phase current table are expressed as a percentage of this maximum phase current.

A pulse on the STEP input automatically increments the step angle number when DIR is high and decrements the step angle number when DIR is low. The magnitude of the resulting change in angle is determined by the selected microstep mode. When step and direction control mode is programmed, the microstep mode is determined solely by the state of the MS input at power-up or after a power-on reset. Half step is selected if MS is low, and quarter step is selected if MS is high. When serial mode is programmed, this allocation and three other pairs of step modes are available, allowing full and eighth steps on STEP input (refer to the Serial Interface section, below).

The serial interface can also be used to control the stepper motor directly. This facility enables full control of the stepper motor at any microstep resolution up to $^1/_{16}$ microstep, plus the ability to change microstep resolution during operation, from one microstep to the next. When using the serial interface to control the stepper motor, a step change value (6-bit) is input through the serial interface to increment or decrement the step angle number. The step change value is a two's complement (2's C) number, where a positive value increments the step angle number and a negative value decrements the step angle number. A single step change in the step angle number is equivalent to a single $^1/_{16}$ microstep. Therefore, for correct motor movement, the step change value should be restricted to no greater than 16 steps positive or negative.

In both control input modes, the resulting step angle number is used to determine the phase current value and current direction for each phase based on the phase current table. The decay mode is determined by the position in the phase current table and the intended direction of rotation of the motor.

Diagnostics

The A4992 integrates several diagnostic features to protect the driver and load, from both fault conditions and extreme operating environments. Some of these features automatically disable the current drive to protect the outputs and the load. Others only provide an indication of the likely fault status (see table 1).

A single open-drain diagnostic output pin, DIAG, provides multiple diagnostic signals. At power-up or after a power-on reset, the DIAG pin outputs a simple Fault flag, which is low if a fault is present. This Fault flag remains low while the fault is present or if one of the latched faults (short circuit or serial write) has been detected.

In addition to the Fault flag, which signals all faults, the DIAG output can be programmed through the serial interface to provide four specific diagnostic signals:

- Stall signal, which goes low only when a stall is detected.
- Open load signal, which goes low only when an open load is detected.
- Temperature signal, which goes low only when the chip temperature rises above either the Hot Temperature Warning or the Overtemperature thresholds.
- Supply voltage signal, which goes low only when:
  - V_{BB} goes above the VBB overvoltage threshold,
  - V_{BB} goes below the VBB undervoltage threshold, or
  - V_{REG} goes below the VREG undervoltage threshold.

Table 1. Fault Table

Diagnostic	Action	Latched
VBB Overvoltage	Disable outputs, set Fault flag	No
VBB Undervoltage	Set Fault flag	No
VREG Undervoltage	Disable outputs, set Fault flag	No
Power-On Reset	Power-down, full reset	No
Temperature Warning	Set Fault flag	No
Overtemperature	Disable outputs, set Fault flag	No
Bridge Short	Disable outputs, set Fault flag	Yes
Bridge Open	Set Fault flag	No
Stall Detect	Set Fault flag	No
Serial Write Fault	Set Fault flag	Yes

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System Diagnostics

At the system level the supply voltages and chip temperature are monitored.

Supply Voltage Monitors

The motor supply, V_{BB}, and the regulator output, V_{REG}, are monitored. The motor supply is monitored for overvoltage and undervoltage, and the regulator output for undervoltage, as follows:

- If the motor supply voltage, V_{BB}, goes above the VBB Overvoltage Threshold, the A4992 will disable the outputs and will indicate the fault. If the motor supply voltage then goes below that threshold, the outputs will be re-enabled and the Fault flag removed.
- If the motor supply voltage, V_{BB}, goes below the VBB Undervoltage Threshold, the A4992 will indicate the fault and reduce the VREG Undervoltage Threshold to the low level. When the motor supply voltage goes above the VBB Undervoltage Threshold the VREG Undervoltage Threshold will be increased to the high level and the Fault flag removed.
- If the motor supply voltage, V_{BB}, goes below the VBB power-on reset threshold, the A4992 will be completely disabled except to monitor the motor supply voltage level. When the motor supply voltage rises above the VBB Power-On Reset Threshold, a power-on reset will take place and all registers will be reset to the default state.
- If the output of the regulator, V_{REG}, goes below the VREG Undervoltage Threshold, the A4992 will disable the outputs and indicate the fault. When the regulator output rises above that threshold the outputs will be re-enabled and the Fault flag removed.

The VREG Undervoltage Threshold level is determined by the state of the VBB undervoltage monitor. If VBB falls causing a VBB undervoltage fault, then the VREG threshold is reduced to the low level, V_{REGUVL}. When VBB is above the VBB Undervoltage Threshold the VREG Undervoltage Threshold is set to the high level, V_{REGUVH}. This allows the A4992 to continue to drive a stepper motor with a motor supply (VBB) voltage as low as 3.8 V without disabling the outputs. By retaining the higher threshold when VBB is above the VBB Undervoltage Threshold, the A4992 also provides protection for its outputs from excessive power dissipation during a high voltage transient on VBB when an independent VREG undervoltage condition is present.

Note that the point at which the A4992 stops driving the motor will always be less than 3.8 V. The maximum value for the low level VREG undervoltage is 3.5 V and for the VREG drop out, V_{REGDO}, is 200 mV. This means that the VREG undervoltage will never occur until VBB falls below 3.7 V, giving a 100 mV margin for noise. Typically the VREG undervoltage will occur when V_{BB} drops below 3.45 V. The A4992 will continue with full PWM current control and all output fault detection right down to the point at which the VREG undervoltage occurs.

Figures 6 and 7 show how the undervoltage thresholds change when a typical cold crank transient occurs.

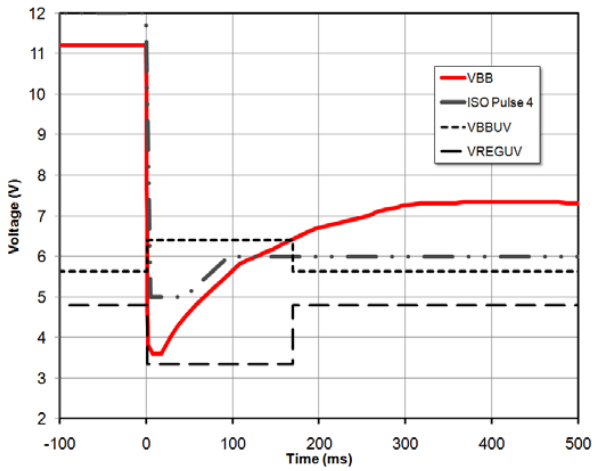

Figure 6. Response to an undervoltage transient

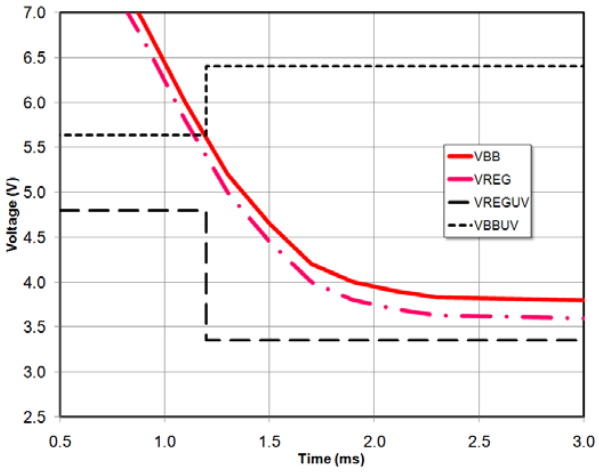

Figure 7. Expanded view of undervoltage transient response

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The standard ISO7637 pulse 4 is shown for reference in figure 6. The VBB transient shown is lower than the standard ISO pulse due to the forward voltage of a reverse polarity protection diode and switching transients.

Figure 7 provides more detail of the time around which the VBB undervoltage is detected, and shows the VREG voltage following below the VBB voltage by the maximum offset voltage of the VREG regulator. Typically this dropout will be less than the 200 mV shown.

When VBB drops below the falling VBB Undervoltage Threshold (at 1.2 ms and 5.6 V in figure 7), the VREG Undervoltage Threshold drops from high, 4.8 V (typ), to low, 3.35 V (typ). At the same time, the VBB Undervoltage Threshold increases by the VBB Threshold Hysteresis, 760 mV, (typ) and the Fault flag is active.

This state remains until VBB increases above the rising VBB undervoltage threshold (at 127 ms and 6.4 V in figure 6). At this point the VREG Undervoltage Threshold is increased back to the high threshold value of 4.8 V (typ) and the reverse hysteresis is applied to the VBB Undervoltage Threshold causing it to drop back to the falling level of 5.5 V (typ). The Fault flag goes inactive.

When a power-on reset occurs, or the A4992 is activated from sleep mode by taking RESETn high, then the VREG Undervoltage Threshold is initially set to the high level, V_{REGUVH}. (A power-on reset occurs either when power is first applied or when the motor supply voltage drops below the VBB Power-On Reset Threshold.) The VREG threshold will remain at the high level, irrespective of the state of VBB, until the VBB voltage has exceeded the VBB Undervoltage Threshold for the first time. After this has happened, the VREG Undervoltage Threshold is then determined by the state of the VBB undervoltage monitor output. When applying power, or when activating from sleep mode, the outputs should remain inactive for at least the Wake-Up from Reset time, t_{EN}, to allow the internal charge pump and regulator to reach their full operating state.

The VBB and VREG undervoltage monitor system is designed to allow the A4992 to continue operating safely during the extreme motor supply voltage drop caused by cold cranking with a weak battery when a reverse battery protection diode is also present. During low voltage transients the A4992 will continue to step a motor. However, current control will not achieve the same accuracy as specified with a motor supply voltage greater than 7 V. In fact a low motor supply voltage may not provide sufficient drive to allow the motor current to reach its normal operating level, especially if the motor is rotating and a back EMF is present. It is therefore recommended that, when a VBB undervoltage condition is indicated, the motor should be held stationary. This will help ensure that the motor does not slip and that the system retains some degree of control over the motor position, thus avoiding the need to recalibrate the motor position.

The output drive FETs of the A4992 remain protected from short circuits down to the VREG undervoltage level. However, the overcurrent thresholds cannot be ensured to meet the precision specified at higher supply voltage. In addition the open load detection may indicate a fault and the stall detection is not likely to correctly identify a motor stall condition when VBB is below the VBB undervoltage level.

Temperature Monitors

Two temperature thresholds are provided, a hot warning and an overtemperature shutdown.

- If the chip temperature rises above the Hot Temperature Warning Threshold the Fault flag will go low. No action will be taken by the A4992. When the temperature drops below the Hot Temperature Warning Threshold, the Fault flag will go high.
- If the chip temperature rises above the Overtemperature Shutdown threshold the Fault flag will go low and the A4992 will disable the outputs to try to prevent a further increase in the chip temperature. When the temperature drops below the overtemperature threshold the Fault flag will go high and the outputs will be re-enabled.

Bridge and Output Diagnostics

The A4992 includes monitors that can detect a short to supply or a short to ground at the motor phase connections. These conditions are detected by monitoring the current from the motor phase connections through the bridge to the motor supply and to ground. Low current comparators and timers are provided to help detect possible open load conditions.

Short to Supply

A short from any of the motor connections to the motor supply, VBB, is detected by monitoring the voltage across the low-side current sense resistor in each bridge. This gives a direct measurement of the current through the low-side of the bridge.

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When a low-side FET is in the on state, the voltage across the sense resistor, under normal operating conditions, should never be more than the maximum sense voltage, V_{SMAX}. In this state, an overcurrent is determined to exist when the voltage across the sense resistor exceeds V_{OCL}, typically $2 \times V_{SMAX}$. This overcurrent must be continuously present for at least the Overcurrent Fault Delay time, t_{SCT}, before the short fault is confirmed by driving the DIAG output low if the Fault flag is selected. The output is switched off and remains off until a fault reset occurs. The actual overcurrent that V_{OCL} represents is determined by the value of the sense resistor and is typically $2 \times I_{SMAX}$.

Short to Ground

A short from any of the motor connections to ground is detected by directly monitoring the current through each of the high-side FETs in each bridge. When a high-side FET is in the on state the maximum current is typically always less than 1.4 A. In this state, an overcurrent is determined to exist when the current through the active high-side FET exceeds the High-Side Overcurrent Threshold, I_{OCH}.

This overcurrent must be present for at least the Overcurrent Fault Delay time, t_{SCT}, before the short fault is confirmed by driving the DIAG output low if the Fault flag is selected. The output is switched off and remains off until a fault reset occurs.

Note that when a short to ground is present the current through the high-side FET is limited to the High-Side Current Limit, I_{LIMH}, during the Overcurrent Fault Delay time. This prevents large negative transients at the phase output pins when the outputs are switched off.

Shorted Load

A short across the load is indicated by concurrent short faults on both high side and low side.

Short Fault Blanking

All overcurrent conditions are ignored for the duration of the Overcurrent Fault Delay time, t_{SCT}. The short detection delay timer is started when an overcurrent first occurs. If the overcurrent is still present at the end of the short detection delay time then a short fault will be generated and latched. If the overcurrent goes away before the short detection delay time is complete, then the timer is reset and no fault is generated.

This prevents false short detection caused by supply and load transients. It also prevents false short detection from the current transients generated by the motor or wiring capacitance when a FET is first switched on.

Short Fault Reset and Retry

When a short circuit has been detected, all outputs for the faulty phase are disabled until: the next rising edge on the STEP input, or the RESETn input is pulsed low, or a serial write is completed. At the next step command, or after a fault reset, the Fault flag is cleared, the outputs are re-enabled, and the voltage across the FET is resampled.

While the fault persists the A4992 will continue this cycle, enabling the outputs for a short period then disabling the outputs. This allows the A4992 to handle a continuous short circuit without damage. If, while stepping rapidly, a short circuit appears and no action is taken, the repeated short circuit current pulses will eventually cause the temperature of the A4992 to rise and an overtemperature fault will occur.

Open Load Detection

Possible open load conditions are detected by monitoring the phase current when the phase DAC values are greater than 31. The open load current threshold, I_{OL}, is defined by the OL bit in the diagnostic Configuration register as a percentage of the maximum (100%) phase current, I_{SMAX}.

The open load current monitor is only active after a Blank Time from the start of a PWM cycle. An open load can only be detected if the DAC value for the phase is greater than 31 and the current has not exceeded the open load current threshold for more than 15 PWM cycles. The A4992 continues to drive the bridge outputs under an open load condition and clears the Fault flag as soon as the phase current exceeds the open load current threshold or the DAC value is less than 32.

Stall Detection

For all motors it is possible to determine the mechanical state of the motor by monitoring the back EMF generated in the motor phase winding. A stalled motor condition is when the phase currents are being sequenced to step the motor but the motor remains stationary. This can be due to a mechanical blockage such as an end stop or the step sequence exceeding the motor capability for the attached load.

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A PWM monitor feature is included in the A4992 to assist in detecting the stall condition of the stepper motor. This feature uses the indirect effect of the back EMF on the current rise quadrant to determine the point at which a stall occurs.

When a motor is running normally at speed, the back EMF, generated by the magnetic poles in the motor passing the phase windings, acts against the supply voltage and reduces the rise rate of the phase current, as shown in figure 8. The PWM current control does not activate until the current reaches the set trip level for the microstep position. When a motor is stopped, as in a stall condition, the back EMF is reduced. This allows the current to rise to the limit faster and the PWM current control to activate sooner. Assuming a constant step rate and motor load this results in an increase in the quantity of PWM cycles for each step of the motor. The A4992 uses this difference to detect a motor changing from continuous stepping to being stalled.

Two PWM counters, one for each phase, accumulate the count of PWM cycles when the phase current is stepped from zero to full current. At the end of each phase current rise, the counter for that phase is compared to the counter for the previous current rise in the opposite phase (see figure 9). If the difference is greater than the PWM count difference in the Configuration register, then the ST fault signal will go low.

This stall detection scheme assumes two factors:

- The motor must be stepping fast enough for the back EMF to reduce the phase current slew rate. Stall detection reliability improves as the current slew rate reduces.
- The motor is not being stepped in full step.

Although stall detection cannot be guaranteed using this detection method, good stall detection reliability can be achieved by careful selection of motor speed, count difference, and by conforming to the above factors.

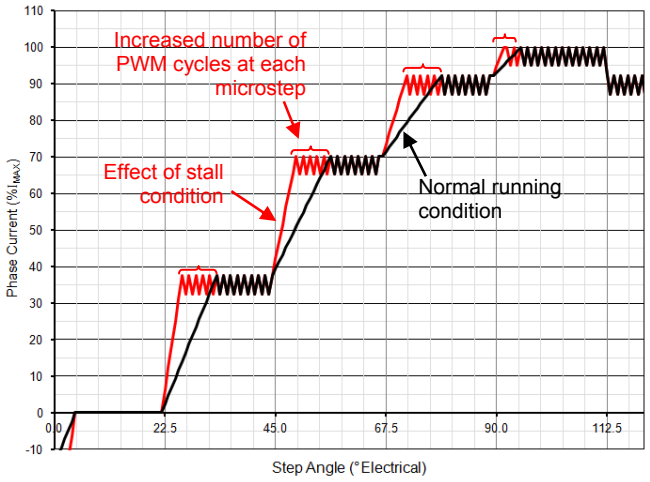

Figure 8. Effect of stall condition on current rise

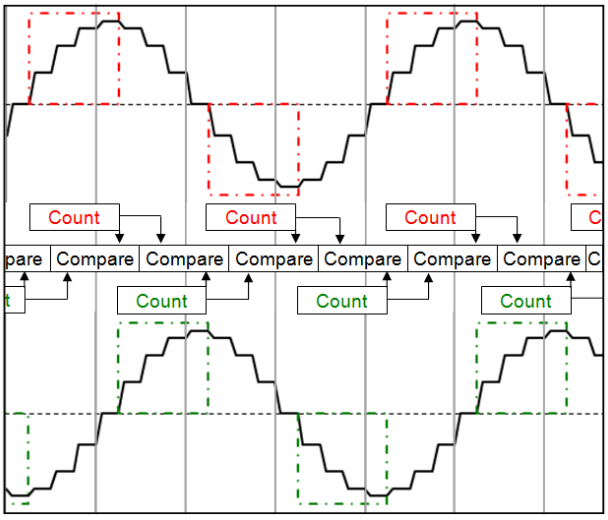

Figure 9. Stall detect by PWM count compare

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SERIAL INTERFACE

A three-wire synchronous serial interface, compatible with SPI, can be used to control all features of the A4992.

The A4992 powers-up in the default step and direction control mode. The serial mode is only available following a specific sequence on the DIR and MS pins when STEP is high (see figure 3). The sequence starts when STEP is high and MS is held high and DIR is held low for longer than the Sequence Minimum Hold Time, t_{SSH}. MS must then be held low and DIR high for longer than t_{SSH}, followed by holding MS high and DIR low for longer than t_{SSH}. The final step is to hold DIR high for t_{SSH}, at which time the A4992 will enter the serial control mode. If STEP is taken low at any time during the sequence then the sequence is reset and the sequence of MS and DIR must be repeated.

When the sequence is accepted by the A4992, the DIAG output will change state for the Serial Mode Acknowledge Pulse duration, $t_{SAP,}$ to indicate that the switch was successful. For example if a fault is present when switching between modes, DIAG will be low during the sequence and will first go high, to acknowledge the mode change, then go low after t_{SAP}. If no fault is present DIAG will be high during the sequence and will first go low to acknowledge the mode change, then go high after t_{SAP}.

When in serial control mode the function of the STEP, DIR, and MS pins change. STEP assumes the function of STRn, the serial data strobe input, DIR functions as SDI, the serial data input, and MS as SCK, the serial clock.

The A4992 will remain in the serial mode as long as the SER bit remains set to 1. If a serial transfer occurs when SER is 0, then the A4992 will revert to the step and direction control mode after the Serial Mode Exit Time, t_{SSEX}, following the rising edge of STRn. The STRn, SDI, and SCK inputs will then revert to their default functions, STEP, DIR, and MS, respectively. The DIAG output will change state for t_{SAP} to indicate that the switch was successful.

Note that the DIAG output is inverted to acknowledge a state change. This means that, if the DIAG output is in the default fault output mode, and a fault occurs or is removed during the time the DIAG pin is inverted, then it will change state part way through the acknowledge pulse time. If this occurs, and it is not clear that the mode has changed, then the sequence must be reset before entering the sequence to change from the step and direction mode to the serial mode. A serial write can then be made to reset back to step and direction mode.

The A4992 can be operated without the serial interface, by using the default settings and the STEP and DIR inputs. Application-specific configurations are only possible, however, by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the motor directly.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in the Serial Data Timing diagram (figure 2). Data is received on SDI and clocked

Table 2. Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Configuration Register																
Config	0	SER	–	TSC	OL	CD4	CD3	CD2	CD1	CD0	MS1	MS0	HLR	TBK	FRQ1	FRQ0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Run Register																
Run	1	SER	–	DG2	DG1	DG0	SR	DIS	–	–	SC5	SC4	SC3	SC2	SC1	SC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*Power-on reset value shown below each input register bit.

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through a shift register on the rising edge of the clock signal input on SCK. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data. If fewer than, or greater than 16 rising edges of the SCK are received before STRn goes high then the sequence is considered invalid and a serial write fault condition is set. This fault condition can be cleared by a subsequent valid serial write and by a power-on-reset or by a RESETn low pulse.

Configuration and Run Registers

The serial data word is 16 bits, input MSB first, and the first bit selects which register is written.

- The first register, selected when the MSB is 0, is the Configuration register, containing system and diagnostic parameters.
- The second register, selected when the MSB is 1, is the Run register, containing motor drive settings used to control the motor movement and phase current.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Config	0	SER	–	TSC	OL	CD4	CD3	CD2	CD1	CD0	MS1	MS0	HLR	TBK	FRQ1	FRQ0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

SER Selects serial or step and direction mode following serial transfer

SER	Control Mode Select	Default
0	Switch to step and direction mode	
1	Remain in serial mode	D

TSC Overcurrent fault delay, assumes 4 MHz clock

TSC	Detect Delay Time	Default
0	2 µs	D
1	4 µs	

OL Open load current threshold as a percentage of maximum current defined by I_{SMAX}

OL	Open Load Current	Default
0	20%	D
1	30%	

CD[4..0] PWM count difference for ST detection
0 = Stall detect disabled
Default to 0.

MS[1..0] Microstep modes for MS input control

MS1	MS0	Microstep Modes		Default
		MS = Low	MS = High	
0	0	Half	Quarter	D
0	1	Full	Half	
1	0	Full	Quarter	
1	1	Half	Eighth	

HLR Selects slow decay recirculation path

HLR	Recirculation Path	Default
0	High side	D
1	Low side	

TBK Blank Time, assumes 4 MHz clock

TBK	Blank Time	Default
0	3.5 µs	D
1	1.5 µs	

FRQ[1..0] Frequency, assumes 4 MHz clock

FRQ 1	FRQ 0	Period / Frequency	Default
0	0	60 µs / 16.7 kHz	
0	1	46 µs / 21.7 kHz	D
1	0	40 µs / 25.0 kHz	
1	1	32 µs / 31.3 kHz	

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Run	1	SER	–	DG2	DG1	DG0	SR	DIS	–	–	SC5	SC4	SC3	SC2	SC1	SC0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SER Selects serial or step and direction mode following serial transfer

SER	Control Mode Select	Default
0	Switch to step and direction mode	D
1	Remain in serial mode	

DG[2..0] Selects signal routed to DIAG output

DG2	DG1	DG0	Signal on DIAG pin (low true)	Default
0	0	0	All Faults	D
0	0	1	VBB and VREG undervoltage, and VBB overvoltage	
0	1	0	Open load	
0	1	1	Temperature warning, and overtemperature	
1	X	X	Stall	

SR Synchronous rectification

SR	Synchronous rectification	Default
0	Synchronous	D
1	Diode recirculation	

DIS Phase current disable

DIS	Phase Outputs	Default
0	Output bridges enabled	D
1	Output bridges disabled	

SC[5..0] Step change number
2's complement format
Positive value increases step angle number
Negative value decreases step angle number

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APPLICATIONS INFORMATION

Motor Movement Control

The A4992 provides two independent methods to control the movement of a stepper motor. The simpler is the step and direction method, which only requires two control signals to control the stepper motor in either direction. The other method is through the serial interface, which provides more flexible control capability. Both methods can be used together (although it is not common), provided the timing restrictions of the STEP input in relation to the STRn input are preserved.

Phase Table and Phase Diagram

The key to understanding both of the available control methods lies in understanding the on-board phase current table, shown here as table 3. This table contains the relative phase current magnitude and direction for each of the two motor phases at each microstep position. The maximum resolution of the A4992 is $^1/_{16}$ microstep. That is 16 microsteps per full step. There are 4 full steps per electrical cycle, so the phase current table has 64 microstep entries. The entries are numbered from 0 to 63. This number represents the phase angle within the full 360° electrical cycle and is called the step angle number. This is illustrated in figure 10.

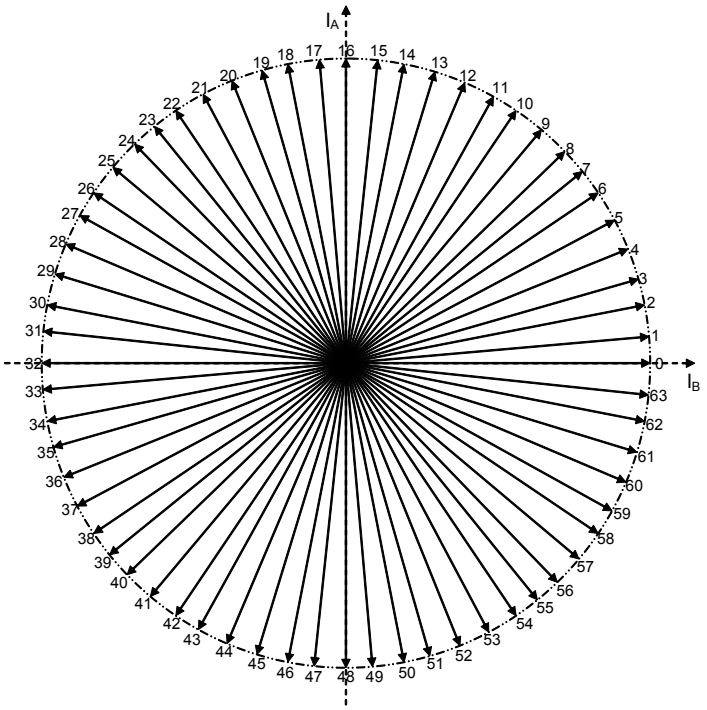

Figure 10. A4992 Phase Current table as a phase diagram; values shown are referred to as the step angle number

Figure 10 shows the contents of the phase current table as a phase diagram. The phase B current, I_B, from the phase current table, is plotted on horizontal axis and the phase A current, I_A, is plotted on the vertical axis. The resultant motor current at each microstep is shown as numbered radial arrows. The number shown corresponds to the $^1/_{16}$ microstep step angle number in the phase current table.

Figure 11 shows an example of calculating the resultant motor current magnitude and angle for step number 28. The target is to have the magnitude of the resultant motor current be 100% at all microstep positions. The relative phase currents from the phase current table are:

$$I_A = 37.50\%$$

$$I_B = -92.19\%$$

Assuming a full scale (100%) current of 1A means that the two phase currents are:

$$I_A = 0.3750 \text{ A}$$

$$I_B = -0.9219 \text{ A}$$

The magnitude of the resultant will be the square root of the sum of the squares of these two currents:

$$|I_{28}| = \sqrt{I_A^2 + I_B^2} = \sqrt{0.1406 + 0.8499} = 0.9953 \text{ (A)}$$

So the resultant current magnitude is 99.53% of full scale. This is within 0.5% of the target (100%) and is well within the ±5% accuracy of the A4992.

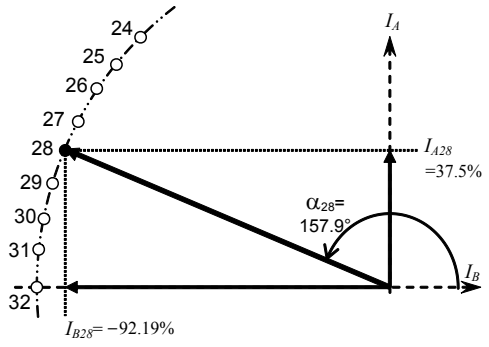

Figure 11. Calculation of resultant motor current

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Table 3. Phase Current Table

Step Angle Number					Phase Current (% of I_{SMAX})		Step Angle	Phase		DAC		Step Angle Number					Phase Current (% of I_{SMAX})		Step Angle	Phase		DAC	
Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B	Full	1/2	1/4	1/8	1/16	A	B		A	B	A	B
	0	0	0	0	0.00	100.00	0.0	0	0	0	63		4	8	16	32	0.00	–100.00	180.0	0	1	0	63
				1	9.38	100.00	5.4	0	0	5	63					33	–9.38	–100.00	185.4	1	1	5	63
			1	2	18.75	98.44	10.8	0	0	11	62				17	34	–18.75	–98.44	190.8	1	1	11	62
				3	29.69	95.31	17.3	0	0	18	60					35	–29.69	–95.31	197.3	1	1	18	60
		1	2	4	37.50	92.19	22.1	0	0	23	58			9	18	36	–37.50	–92.19	202.1	1	1	23	58
				5	46.88	87.50	28.2	0	0	29	55					37	–46.88	–87.50	208.2	1	1	29	55
			3	6	56.25	82.81	34.2	0	0	35	52				19	38	–56.25	–82.81	214.2	1	1	35	52
				7	64.06	76.56	39.9	0	0	40	48					39	–64.06	–76.56	219.9	1	1	40	48
0	1	2	4	8	70.31	70.31	45.0	0	0	44	44	2	5	10	20	40	–70.31	–70.31	225.0	1	1	44	44
				9	76.56	64.06	50.1	0	0	48	40					41	–76.56	–64.06	230.1	1	1	48	40
			5	10	82.81	56.25	55.8	0	0	52	35				21	42	–82.81	–56.25	235.8	1	1	52	35
				11	87.50	46.88	61.8	0	0	55	29					43	–87.50	–46.88	241.8	1	1	55	29
		3	6	12	92.19	37.50	67.9	0	0	58	23			11	22	44	–92.19	–37.50	247.9	1	1	58	23
				13	95.31	29.69	72.7	0	0	60	18					45	–95.31	–29.69	252.7	1	1	60	18
			7	14	98.44	18.75	79.2	0	0	62	11				23	46	–98.44	–18.75	259.2	1	1	62	11
				15	100.00	9.38	84.6	0	0	63	5					47	–100.00	–9.38	264.6	1	1	63	5
	2	4	8	16	100.00	0.00	90.0	0	0	63	0		6	12	24	48	–100.00	0.00	270.0	1	1	63	0
				17	100.00	–9.38	95.4	0	1	63	5					49	–100.00	9.38	275.4	1	0	63	5
			9	18	98.44	–18.75	100.8	0	1	62	11				25	50	–98.44	18.75	280.8	1	0	62	11
				19	95.31	–29.69	107.3	0	1	60	18					51	–95.31	29.69	287.3	1	0	60	18
		5	10	20	92.19	–37.50	112.1	0	1	58	23			13	26	52	–92.19	37.50	292.1	1	0	58	23
				21	87.50	–46.88	118.2	0	1	55	29					53	–87.50	46.88	298.2	1	0	55	29
			11	22	82.81	–56.25	124.2	0	1	52	35				27	54	–82.81	56.25	304.2	1	0	52	35
				23	76.56	–64.06	129.9	0	1	48	40					55	–76.56	64.06	309.9	1	0	48	40
1	3	6	12	24	70.31	–70.31	135.0	0	1	44	44	3	7	14	28	56	–70.31	70.31	315.0	1	0	44	44
				25	64.06	–76.56	140.1	0	1	40	48					57	–64.06	76.56	320.1	1	0	40	48
			13	26	56.25	–82.81	145.8	0	1	35	52				29	58	–56.25	82.81	325.8	1	0	35	52
				27	46.88	–87.50	151.8	0	1	29	55					59	–46.88	87.50	331.8	1	0	29	55
		7	14	28	37.50	–92.19	157.9	0	1	23	58			15	30	60	–37.50	92.19	337.9	1	0	23	58
				29	29.69	–95.31	162.7	0	1	18	60					61	–29.69	95.31	342.7	1	0	18	60
			15	30	18.75	–98.44	169.2	0	1	11	62				31	62	–18.75	98.44	349.2	1	0	11	62
				31	9.38	–100.00	174.6	0	1	5	63					63	–9.38	100.00	354.6	1	0	5	63
	4	8	16	32	0.00	–100.00	180.0	0	1	0	63		0	0	0	0	0.00	100.00	0.0	0	0	0	63

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The reference angle, zero degrees (0°), within the full electrical cycle (360°), is defined as the angle where I_B is at +100% and I_A is zero. Each full step is represented by 90° in the electrical cycle so each one-sixteenth microstep is: 90°/16 steps = 5.625°. The target angle of each microstep position with the electrical cycle is determined by the product of the Step angle number and the angle for a single microstep. So for the example of figure 11:

$$\alpha_{28(TARGET)} = 28 \times 5.625° = 157.5°$$

The actual angle is calculated using basic trigonometry as:

$$\alpha_{28(ACTUAL)} = 180 + \tan^{-1}\left(\frac{I_{A28}}{I_{B28}}\right)$$

$$= 180 + (-22.1) = 157.9°$$

So the angle error is only 0.4°. Equivalent to about 0.1% error in 360° and well within the current accuracy of the A4992.

Note that each phase current in the A4992 is defined by a 6-bit DAC. This means that the smallest resolution of the DAC is 100 / 64 = 1.56% of the full scale, so the A4992 cannot produce a resultant motor current of exactly 100% at each microstep. Nor can it produce an exact microstep angle. However, as can be seen from the calculations above, the results for both are well within the specified accuracy of the A4992 current control. The resultant motor current angle and magnitude are also more than precise enough for all but the highest precision stepper motors.

With the phase current table, control of a stepper motor is simply a matter of increasing or decreasing the Step angle number to move around the phase diagram of figure 10. This can be in predefined multiples using the STEP input, or it can be variable using the serial interface.

Using Step and Direction Control

The STEP input moves the motor at the microstep resolution defined by the MS0 and MS1 bits and the logic level of the MS input. The DIR input defines the motor direction. These inputs define the output of a translator which determines the required step angle number in the phase current table.

The MS input allows two microstep resolutions to be selected. The default combination, reset at power-on, is half step when MS is low, and quarter step when MS is high. The two resolution combinations can be changed using the MS0 and MS1 bits in the Configuration register through the serial interface. The combinations available are as shown in table 4.

Note that the microstep selection is only used with the STEP input. It has no effect when the motor is fully controlled through the serial interface. $^1/_{16}$ microstepping is only possible using the serial interface.

In eighth-step mode the translator simply increments or decrements the step angle number by two on each rising edge of the STEP input depending on the logic state of the DIR input. In the other three microstep resolution modes the translator outputs specific step angle numbers as defined in the phase current table.

Full step uses four of the entries in the phase current table. These are 8, 24, 40, and 56 as shown in figure 12. Note that the four positions selected for full step are not the points at which only one current is active, as would be the case in a simple on-off full step driver. There are two advantages in using these positions rather than the single full current positions. With both phases active, the power dissipation is shared between two drivers. This slightly improves the ability to dissipate the heat generated and reduces the stress on each driver. The second reason is that the holding torque is slightly improved because the forces holding the motor are mainly rotational rather than mainly radial.

Table 4. Microstep Mode Selection (Serial Mode)

MS1	MS0	Microstep Mode	
		MS = Low	MS = High
0	0	Half Step	Quarter Step
0	1	Full Step	Half Step
1	0	Full Step	Quarter Step
1	1	Half Step	Eighth Step

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Half step uses eight of the entries in the phase current table. These are 0, 8, 16, 24, 32, 40, 48, and 56 as shown in figure 13.

Quarter step uses sixteen of the entries in the phase current table. These are 0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, and 60 as shown in figure 14.

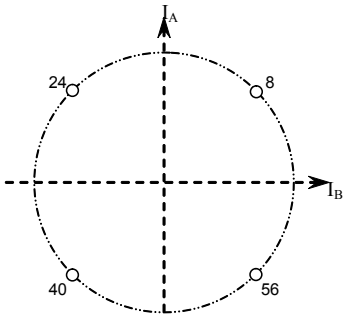

Figure 12. Full-step phase diagram using STEP input

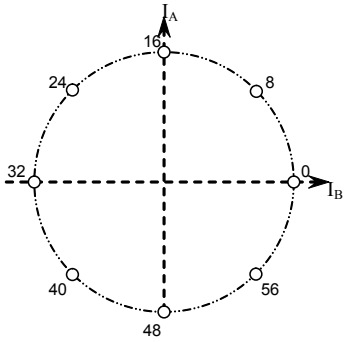

Figure 13. Half-step phase diagram using STEP input

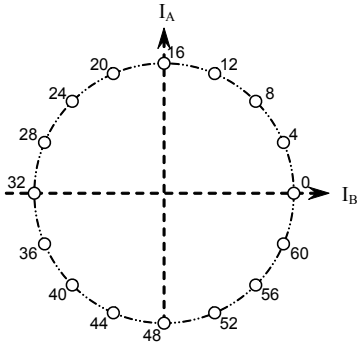

Figure 14. Quarter-step phase diagram using STEP input

In half step and in quarter step, the single-phase active positions are used to preserve symmetry. However, if the motor is required to stop with a significant holding torque for any length of time it is recommended that the 45° positions be used; those are step angle numbers 8, 24, 40, and 56, as used with full-step resolution.

Table 5 summarizes the step angle numbers used for the four resolutions available when using the STEP input to control the output of the A4992.

The microstep select inputs can be changed between each rising edge of the STEP input. The only restriction is that the MS logic input must comply with the set-up and hold timing constraints. When the microstep resolution changes, the A4992 moves to the next available step angle number on the next rising edge of the STEP input. For example, if the microstep mode is eighth and the present step angle is 58 then with the direction forwards (increasing step angle), changing to quarter step will cause the phase number to go to 60 on the next rising edge of the STEP input. If the microstep mode is changed to half step, then the phase number will go to 0 on the next rising edge of the STEP input. If the microstep mode is changed to full step, then the phase number will go to 8 on the next rising edge of the STEP input.

Control Through the Serial Interface

The A4992 provides the ability to directly control the motor movement using only the serial interface by directly increasing or decreasing the step angle number. Note that the maximum value of the step angle number is 63 and the minimum number is 0. Therefore, any increase or reduction in the microstep number is performed using modulo 64 arithmetic. This means that increasing a step angle number of 63 by 1 will produce a step angle number of 0. Increasing by two from 63 will produce 1 and so on. Similarly, in the reverse direction, reducing a step angle number

Table 5. Step Angle Number Allocation

Mode	Step Angle
Full Step	8, 24, 40, 56
Half Step	0, 8, 16, 24, 32, 40, 48,56
Quarter Step	0, 4, 8, 12, 16, 20, 24, 28, 32, 36, 40, 44, 48, 52, 56, 60
Eighth Step	0, 2, 4, 6, 8, 10, 12, 14, 16 18, 20, 22, 24, 26, 28, 32, 32, 34, 36, 38, 40, 42, 44, 46, 48, 50, 52, 54, 56, 58, 60, 62

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of 0 by 1 will produce a step angle number of 63. Decreasing by two from 0 will produce 62 and so on.

The least significant six bits of the Run register, bits 0 to 5, are the step change number, SC[5..0]. This number is a two's complement number that is added to the step angle number causing it to increase or decrease. Two's complement is the natural integer number system for most microcontrollers. This allows standard arithmetic operators to be used, within the microcontroller, to determine the size of the next step increment. Table 6 shows the binary equivalent of each decimal number between 16 and +16.

Each increase in the step angle number represents a forward movement of one eighth microstep. Each decrease in the step angle number represents a reverse movement of one eighth microstep.

To move the motor one full step, the step angle number must be increased or decreased by 16. To move the motor one half step, the step angle number must be increased or decreased by 8. For quarter step the increase or decrease is 4 and for eighth step, 2.

So, for example, to continuously move the motor forwards in quarter-step increments, the number 4 (000100) is repeatedly written to SC[5..0] through the serial interface Run register (see figure 15). To move the motor backwards in quarter step increments, the number -4 (111100) is repeatedly written to SC[5..0] (see figure 16). The remaining bits in the Run register should be set for the required configuration and sent with the step change number each time.

Table 6. Two's Complements

Decimal	2's Complement	Decimal	2's Complement
0	000000	–	–
1	000001	–1	111111
2	000010	–2	111110
3	000011	–3	111101
4	000100	–4	111100
5	000101	–5	111011
6	000110	–6	111010
7	000111	–7	111001
8	001000	–8	111000
9	001001	–9	110111
10	001010	–10	110110
11	001011	–11	110101
12	001100	–12	110100
13	001101	–13	110011
14	001110	–14	110010
15	001111	–15	110001
16	010000	–16	110000

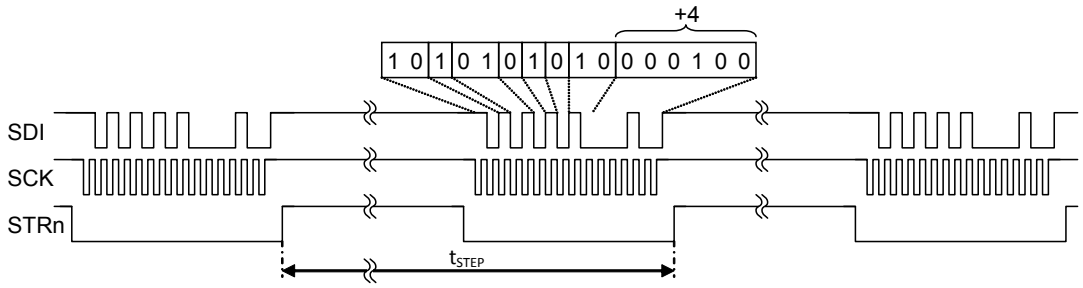

Figure 8. Serial interface sequence for quarter step in forward direction

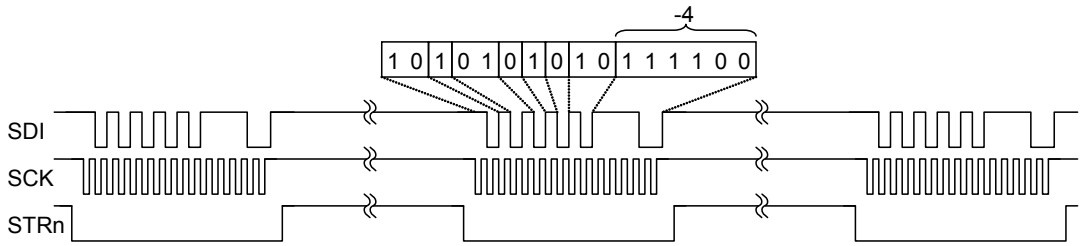

Figure 9. Serial interface sequence for quarter step in reverse direction

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The step rate is controlled by the timing of the serial interface. It is the inverse of the step time, t_{STEP}, shown in figure 15. The motor step only takes place when the STRn goes from low to high when writing to the Run register. The motor step rate is therefore determined by the timing of the rising edge of the STRn input. The clock rate of the serial interface, defined by the frequency of the SCK input, has no effect on the step rate.

Layout

The printed circuit board (PCB) should use a higher weight copper thickness than a standard small signal or digital board. This helps to reduce the impedance of the copper traces when conducting high currents. PCB traces carrying switching currents should be as wide and short as possible to reduce the inductance of the trace. This will help reduce any voltage transients caused by current switching during PWM current control.

For optimum thermal performance, the exposed thermal pad on the underside of the A4992 should be soldered directly onto the board. A solid ground plane should be added to the opposite side of the board and multiple vias through the board placed in the area under the thermal pad.

Decoupling

All supplies should be decoupled with an electrolytic capacitor in parallel with a ceramic capacitor. The ceramic capacitor should have a value of 100 nF and should be placed as close as possible to the associated supply and ground pins of the A4992. The electrolytic capacitor connected to VBB should be rated to at least 1.5 times the maximum voltage and selected to support the maximum ripple current provided to the motor. The value of the capacitor is unimportant but should be the lowest value with the necessary ripple current capability.

The pump capacitor between CP1 and CP2, the pump storage capacitor between VCP and VBB, and the compensation capacitor between VREG and ground should be connected as close as possible to the respective pins of the A4992.

Grounding

A star ground system, with the common star point located close to the A4992 is recommended. On the 20-lead TSSOP package, the reference ground, AGND (pin 6), and the power ground, PGND (pin 9), must be connected together externally. The copper ground plane located under the exposed thermal pad is typically used as the star ground point.

Current Sense Resistor

To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistors (R_{Sx}) should have an independent ground return to the star ground point. This path should be as short as possible. For low-value sense resistors the IR drop in the PCB trace to the sense resistor can be significant and should be taken into account. Surface mount chip resistors are recommended to minimize contact resistance and parasitic inductance. The value, R_S, of the sense resistors is given by:

$$R_S = \frac{V_{REF}}{16 \times I_{SMAX}}$$

There is no restriction on the value of R_S or V_{REF}, other than the range of V_{REF} over which the output current precision is guaranteed. However, it is recommended that the value of V_{REF} be kept as high as possible to improve the current accuracy. Table 7 provides increasing values of I_{SMAX} for suggested values of V_{REF} and standard E96 values of R_S.

Table 7. Suggested Values

I_{SMAX} (mA)	R_S (mΩ)	V_{REF} (V)
100	499	0.8
200	499	1.6
300	417	2.0
405	309	2.0
501	249	2.0
610	205	2.0
702	178	2.0
812	154	2.0
912	137	2.0
1008	124	2.0

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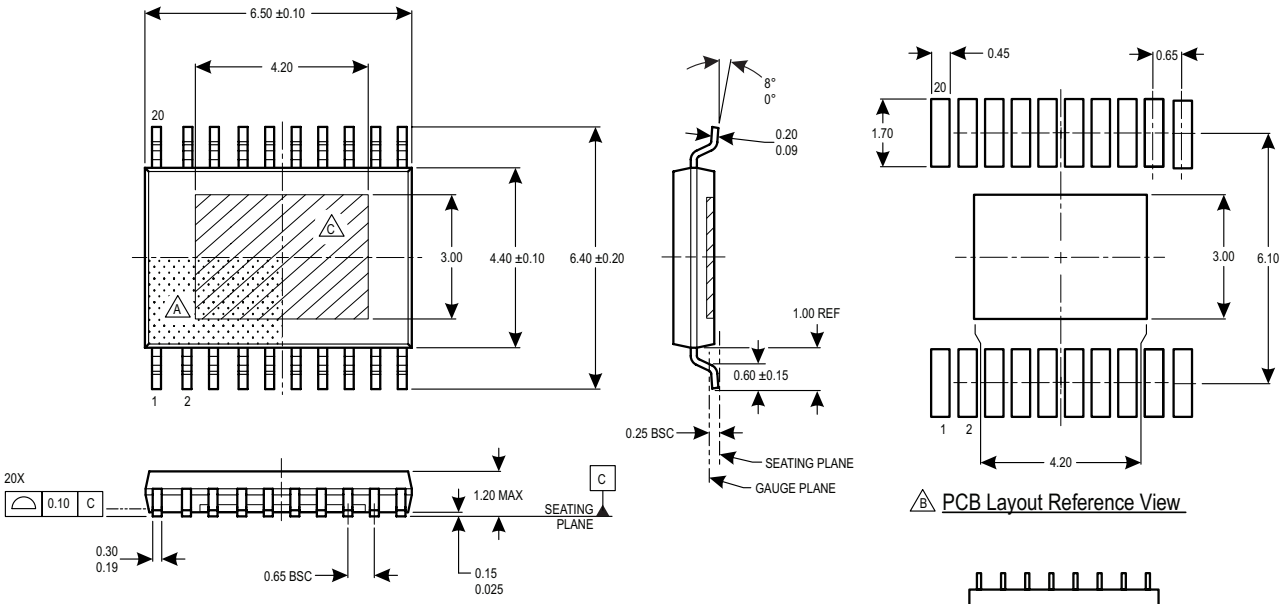
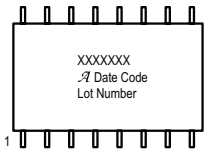
Package LP, 20-Pin TSSOP With Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
1	April 22, 2014	Revised T_{tJ} spec. in Abs. Max. Ratings table
2	April 10, 2020	Minor editorial updates
3	April 5, 2022	Updated package drawing (page 28)

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