

74ABT16543

16-bit latched transceiver with dual enable; 3-state

Rev. 04 — 26 May 2005

Product data sheet

1. General description

The 74ABT16543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16543 16-bit registered transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch enable ($\overline{\text{nLEAB}}$, $\overline{\text{nLEBA}}$) and output enable ($\overline{\text{nOEAB}}$, $\overline{\text{nOEBA}}$) inputs are provided for each register to permit independent control of data transfer in either direction. The outputs are guaranteed to sink 64 mA.

2. Features

- Two 8-bit octal transceivers with D-type latch
- Live insertion and extraction permitted
- Power-up 3-state
- Power-up reset
- Multiple V_{CC} and GND pins minimize switching noise
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64 mA and –32 mA
- Latch-up protection exceeds 500 mA per JEDEC Std 78
- ESD protection:
 - ◆ MIL STD 883 method 3015: exceeds 2000 V
 - ◆ Machine model: exceeds 200 V

3. Quick reference data

Table 1: Quick reference data

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $GND = 0\text{ V}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PLH}	propagation delay nAx to nBx	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	-	2.5	-	ns
t_{PHL}	propagation delay nAx to nBx	$C_L = 50\text{ pF}$; $V_{CC} = 5\text{ V}$	-	2.2	-	ns
C_I	input capacitance	$V_I = 0\text{ V}$ or V_{CC}	-	3	-	pF
$C_{I/O}$	I/O capacitance	$V_O = 0\text{ V}$ or V_{CC} ; 3-state	-	7	-	pF
I_{CC}	quiescent supply current	$V_{CC} = 5.5\text{ V}$; $V_I = GND$ or V_{CC}				
		outputs 3-state	-	0.55	-	mA
		outputs LOW-state	-	9	-	mA

PHILIPS

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16543BB	−40 °C to +85 °C	QFP52	plastic quad flat package; 52 leads (lead length 1.6 mm); body width 10 × 10 × 2 mm	SOT379-2

5. Functional diagram

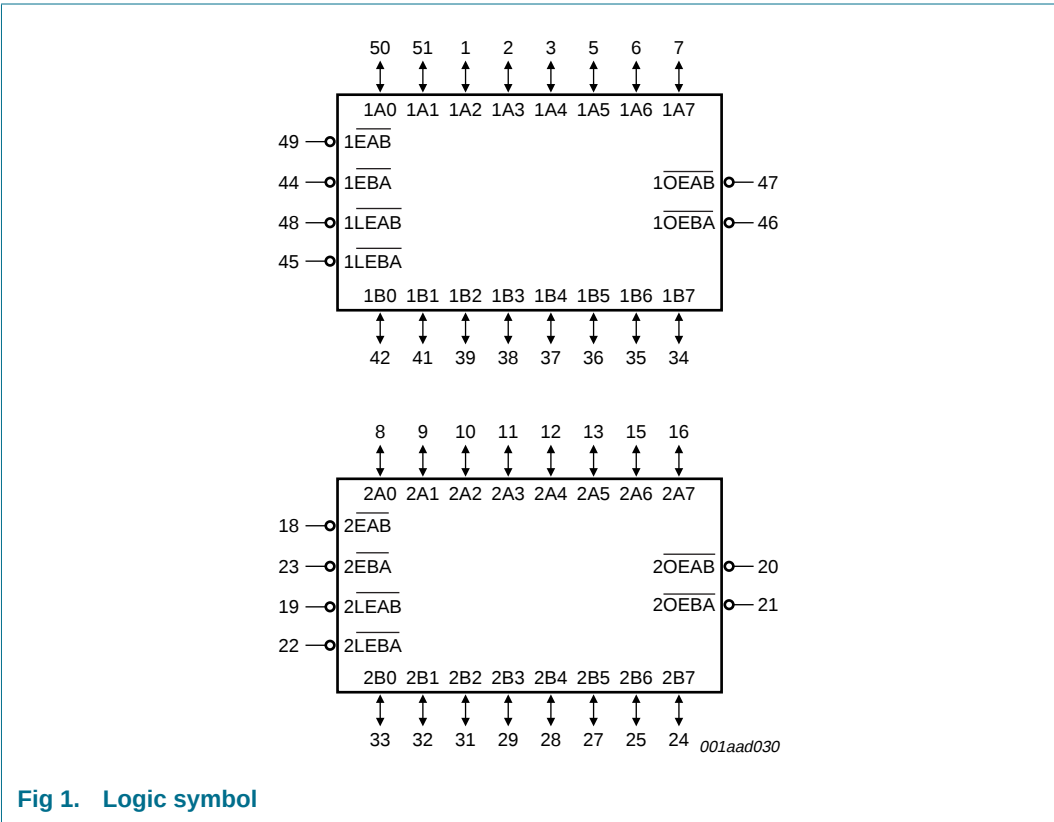
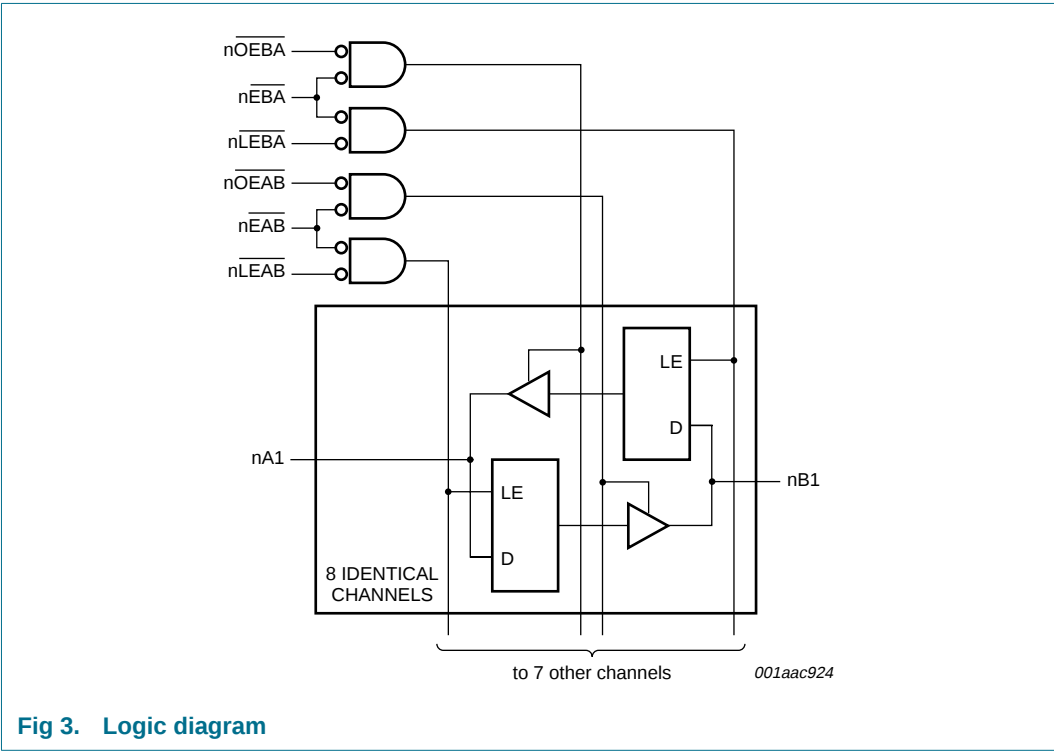
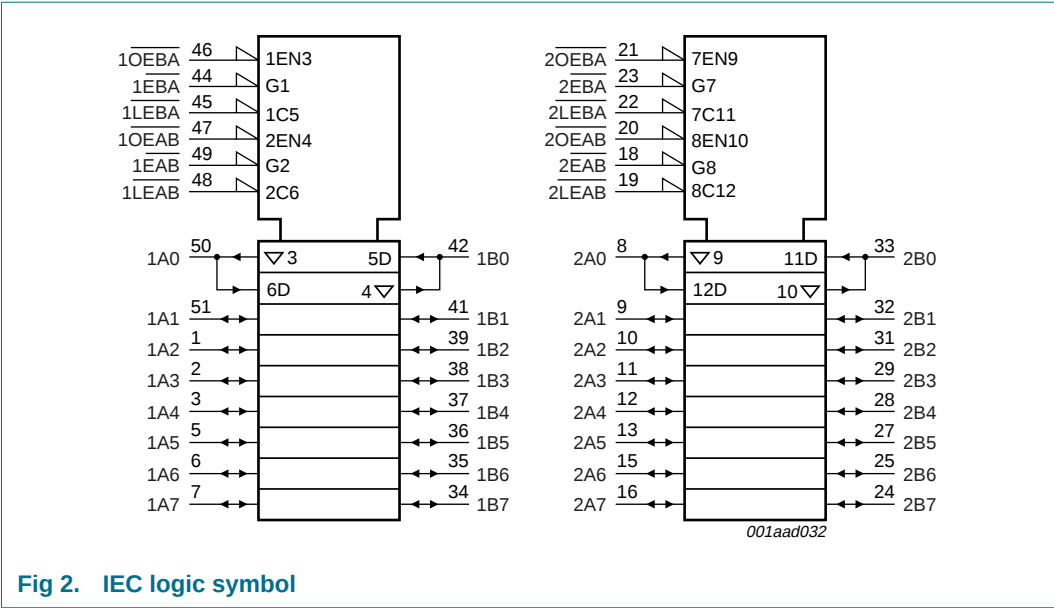
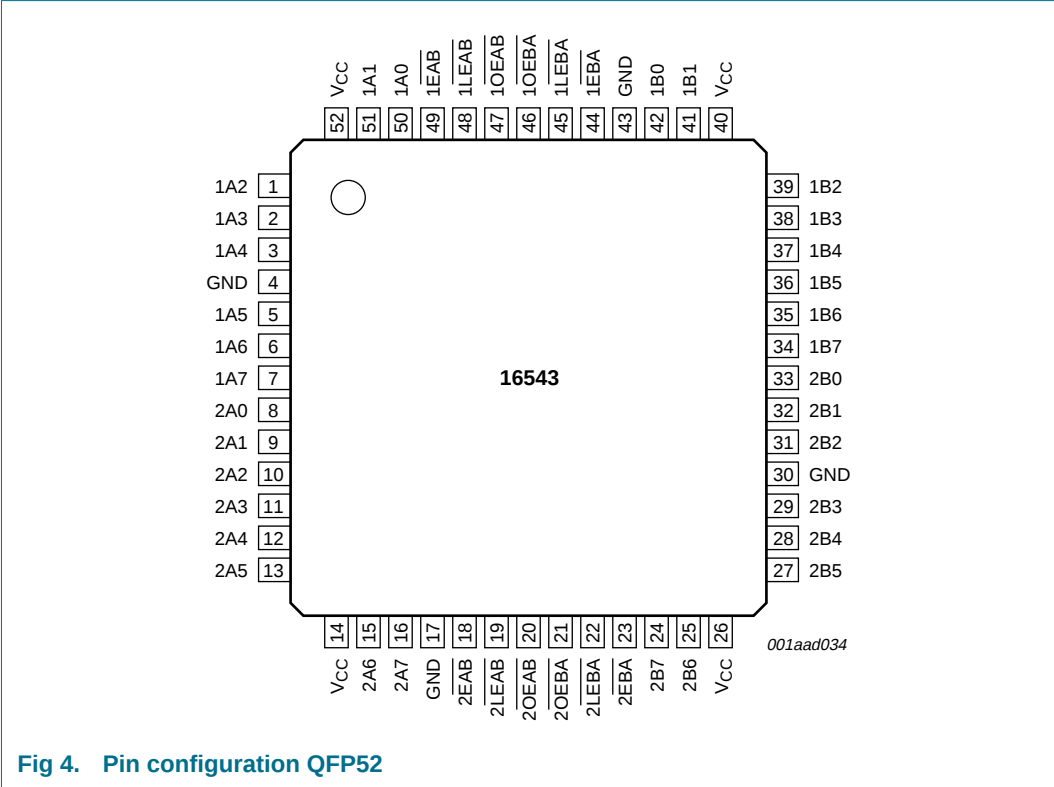


Fig 1. Logic symbol



6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
1A2	1	1 data input or output 2; A-side
1A3	2	1 data input or output 3; A-side
1A4	3	1 data input or output 4; A-side
GND	4	ground (0 V)
1A5	5	1 data input or output 5; A-side
1A6	6	1 data input or output 6; A-side
1A7	7	1 data input or output 7; A-side
2A0	8	2 data input or output 0; A-side
2A1	9	2 data input or output 1; A-side
2A2	10	2 data input or output 2; A-side
2A3	11	2 data input or output 3; A-side
2A4	12	2 data input or output 4; A-side
2A5	13	2 data input or output 5; A-side
V _{CC}	14	supply voltage
2A6	15	2 data input or output 6; A-side

Table 3: Pin description ...continued

Symbol	Pin	Description
2A7	16	2 data input or output 7; A-side
GND	17	ground (0 V)
$\overline{2EAB}$	18	A-to-B output enable input (active LOW)
$\overline{2LEAB}$	19	A-to-B latch enable input (active LOW)
$\overline{2OEAB}$	20	A-to-B enable input (active LOW)
$\overline{2OEBA}$	21	B-to-A output enable input (active LOW)
$\overline{2LEBA}$	22	B-to-A latch enable input (active LOW)
$\overline{2EBA}$	23	B-to-A enable input (active LOW)
2B7	24	2 data input or output 7; B-side
2B6	25	2 data input or output 6; B-side
V _{CC}	26	supply voltage
2B5	27	2 data input or output 5; B-side
2B4	28	2 data input or output 4; B-side
2B3	29	2 data input or output 3; B-side
GND	30	ground (0 V)
2B2	31	2 data input or output 2; B-side
2B1	32	2 data input or output 1; B-side
2B0	33	2 data input or output 0; B-side
1B7	34	1 data input or output 7; B-side
1B6	35	1 data input or output 6; B-side
1B5	36	1 data input or output 5; B-side
1B4	37	1 data input or output 4; B-side
1B3	38	1 data input or output 3; B-side
1B2	39	1 data input or output 2; B-side
V _{CC}	40	positive supply voltage
1B1	41	1 data input or output 1; B-side
1B0	42	1 data input or output 0; B-side
GND	43	ground (0 V)
$\overline{1EBA}$	44	B-to-A output enable input (active LOW)
$\overline{1LEBA}$	45	B-to-A latch enable input (active LOW)
$\overline{1OEBA}$	46	B-to-A enable input (active LOW)
$\overline{1OEAB}$	47	A-to-B output enable input (active LOW)
$\overline{1LEAB}$	48	A-to-B latch enable input (active LOW)
$\overline{1EAB}$	49	A-to-B enable input (active LOW)
1A0	50	1 data input or output 0; A-side
1A1	51	1 data input or output 1; A-side
V _{CC}	52	supply voltage

7. Functional description

7.1 Function table

Table 4: Function table ^[1]

Input				Output	Status
$\overline{nOEAB}$ or $\overline{nOEBA}$	$\overline{nEAB}$ or $\overline{nEBA}$	$\overline{nLEAB}$ or $\overline{nLEBA}$	nAx or nBx	nBx or nAx	
H	X	X	X	Z	disabled
X	H	X	X	Z	disabled
L	↑	L	h	Z	disabled + latch
L	↑	L	l	Z	disabled + latch
L	L	↑	h	H	latch + display
L	L	↑	l	L	latch + display
L	L	L	H	H	transparent
L	L	L	L	L	transparent
L	L	H	X	NC	hold

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH transition of $\overline{nLEAB}$, $\overline{nLEBA}$, $\overline{nEAB}$ or $\overline{nEBA}$;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH transition of $\overline{nLEAB}$, $\overline{nLEBA}$, $\overline{nEAB}$ or $\overline{nEBA}$;
X = don't care;
Z = high-impedance off state;
↑ = LOW-to-HIGH transition;
NC = no change.

7.2 Description

The 74ABT16543 contains two sets of eight D-type latches, with separate control pins for each set. Using data flow from A to B as an example, when the A-to-B enable ($\overline{nEAB}$) input and the A-to-B latch enable ($\overline{nLEAB}$) input are LOW the A-to-B path is transparent.

A subsequent LOW-to-HIGH transition of the $\overline{nLEAB}$ signal puts the A data into the latches where it is stored and the B outputs no longer change with the A inputs. With $\overline{nEAB}$ and $\overline{nOEAB}$ both LOW, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{nEBA}$, $\overline{nLEBA}$, and $\overline{nOEBA}$ inputs.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		[1] -1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+5.5	V
I_{IK}	input diode current	$V_I < 0$ V	-	-18	mA
I_{OK}	output diode current	$V_O < 0$ V	-	-50	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_j	junction temperature		[2] -	+150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-	-	-32	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IK}	input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-	-	-1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; V _I = V _{IL} or V _{IH}				
		I _{OH} = -3 mA	2.5	2.9	-	V
		I _{OH} = -32 mA	2.0	2.4	-	V
		V _{CC} = 5.0 V; V _I = V _{IL} or V _{IH}				
		I _{OH} = -3 mA	3.0	3.4	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; V _I = V _{IL} or V _{IH} ; I _{OL} = 64 mA	-	0.36	0.55	V
V _{RST}	power-up output voltage	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	[1]	-	0.13	0.55 V
I _{LI}	input leakage current of control pins	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	±0.01	±1.0	µA
I _{OFF}	power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	-	±2.0	±100	µA
I _{PU} , I _{PD}	power-up or power-down down 3-state output current	V _{CC} = 2.1 V; V _O = 0.0 V or V _{CC} ; V _I = GND or V _{CC} ; V _{noEAB} and V _{noEBA} = don't care	[2]	-	±1.0	±50 µA
I _{OZ}	3-state output current	V _{CC} = 5.5 V; V _I = V _{IL} or V _{IH}				
		outputs HIGH-state at V _O = 5.5 V	-	1.0	10	µA
		outputs LOW-state at V _O = 0.0 V	-	-1.0	-10	µA
I _{CEX}	output HIGH leakage current	V _{CC} = 5.5 V; V _O = 5.5 V; V _I = GND or V _{CC}	-	1.0	50	µA
I _O	output current	V _{CC} = 5.5 V; V _O = 2.5 V	[3]	-50	-100	-200 mA
C _I	input capacitance	V _I = 0 V or V _{CC}	-	3	-	pF
C _{I/O}	I/O capacitance	V _O = 0 V or V _{CC} ; 3-state	-	7	-	pF
I _{CC}	quiescent supply current	V _{CC} = 5.5 V; V _I = GND or V _{CC}				
		outputs HIGH-state	-	0.55	2	mA
		outputs LOW-state	-	9	19	mA
		outputs 3-state	-	0.55	2	mA
ΔI _{CC}	additional supply current per input pin	V _{CC} = 5.5 V; one input at 3.4 V; other inputs at V _{CC} or GND	[4]	-	5.0	50 µA
T_{amb} = -40 °C to +85 °C						
V _{IK}	input clamp voltage	V _{CC} = 4.5 V; I _{IK} = -18 mA	-	-	-1.2	V
V _{OH}	HIGH-level output voltage	V _{CC} = 4.5 V; V _I = V _{IL} or V _{IH}				
		I _{OH} = -3 mA	2.5	-	-	V
		I _{OH} = -32 mA	2.0	-	-	V
		V _{CC} = 5.0 V; V _I = V _{IL} or V _{IH}				
		I _{OH} = -3 mA	3.0	-	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 4.5 V; V _I = V _{IL} or V _{IH} ; I _{OL} = 64 mA			0.55	V
V _{RST}	power-up output voltage	V _{CC} = 5.5 V; I _O = 1 mA; V _I = GND or V _{CC}	[1]	-	-	0.55 V
I _{LI}	input leakage current of control pins	V _{CC} = 5.5 V; V _I = GND or 5.5 V	-	-	±1.0	µA
I _{OFF}	power-off leakage current	V _{CC} = 0.0 V; V _O or V _I ≤ 4.5 V	-	-	±100	µA

Table 7: Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PU}, I_{PD}	power-up or power-down down 3-state output current	$V_{CC} = 2.1\text{ V}$; $V_O = 0.0\text{ V}$ or V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; V_{nOEAB} and $V_{nOEBA} = \text{don't care}$	[2] -	-	± 50	μA
I_{OZ}	3-state output current	$V_{CC} = 5.5\text{ V}$; $V_I = V_{IL}$ or V_{IH}				
		outputs HIGH-state at $V_O = 5.5\text{ V}$	-	-	10	μA
		outputs LOW-state at $V_O = 0.0\text{ V}$	-	-	-10	μA
I_{CEX}	output HIGH leakage current	$V_{CC} = 5.5\text{ V}$; $V_O = 5.5\text{ V}$; $V_I = \text{GND}$ or V_{CC}	-	-	50	μA
I_O	output current	$V_{CC} = 5.5\text{ V}$; $V_O = 2.5\text{ V}$	[3] -50	-	-200	mA
I_{CC}	quiescent supply current	$V_{CC} = 5.5\text{ V}$; $V_I = \text{GND}$ or V_{CC}				
		outputs HIGH-state	-	-	2	mA
		outputs LOW-state	-	-	19	mA
		outputs 3-state	-	-	2	mA
ΔI_{CC}	additional supply current per input pin	$V_{CC} = 5.5\text{ V}$; one input at 3.4 V; other inputs at V_{CC} or GND	[4] -	-	50	μA

[1] For valid test results, data must not be loaded into the latches after applying the power.

[2] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms; From $V_{CC} = 2.1\text{ V}$ to $V_{CC} = 5\text{ V} \pm 10\%$ a transition time of up to 100 μs is permitted.

[3] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[4] This is the increase in supply current for each input at 3.4 V.

11. Dynamic characteristics

Table 8: Dynamic characteristicsGND = 0 V; for test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C; V_{CC} = 5.0 V						
t_{PLH}	propagation delay					
	nAx to nBx, nBx to nAx	see Figure 6	1.0	2.5	3.3	ns
	nLEBA to nAx, nLEAB to nBx	see Figure 5	1.0	3.1	4.3	ns
t_{PHL}	propagation delay					
	nAx to nBx, nBx to nAx	see Figure 6	1.0	2.2	4.4	ns
	nLEBA to nAx, nLEAB to nBx	see Figure 5	1.2	3.0	4.8	ns
t_{PZH}	output enable time	see Figure 7				
	nOEBA to nAx, nOEAB to nBx		1.0	3.3	4.3	ns
	nEBA to nAx, nEAB to nBx		1.0	3.4	4.9	ns
t_{PZL}	output enable time	see Figure 8				
	nOEBA to nAx, nOEAB to nBx		1.1	3.3	5.9	ns
	nEBA to nAx, nEAB to nBx		1.2	3.4	6.5	ns
t_{PHZ}	output disable time	see Figure 7				
	nOEBA to nAx, nOEAB to nBx		1.9	3.5	5.0	ns
	nEBA to nAx, nEAB to nBx		2.0	3.4	5.6	ns

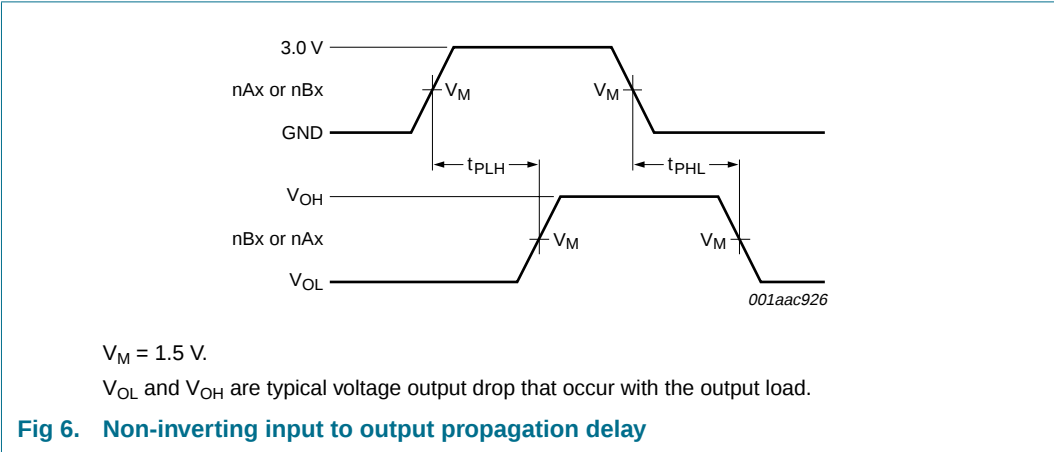
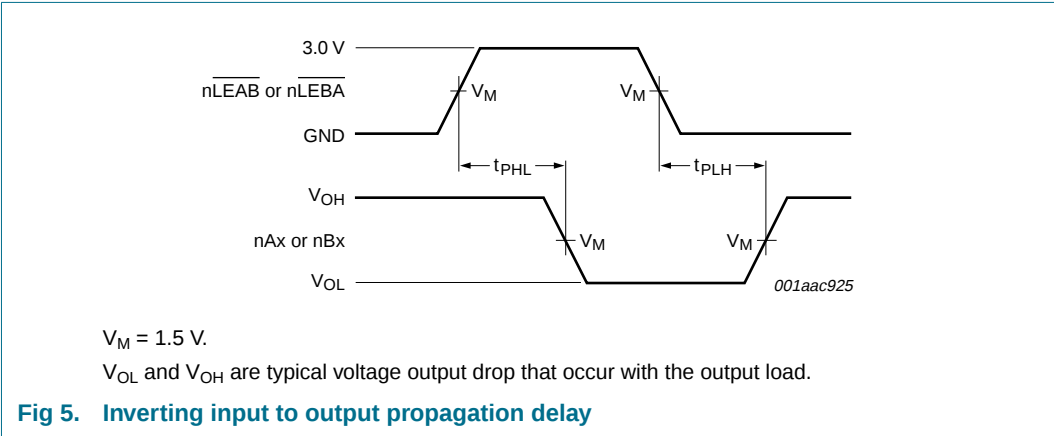
Table 8: Dynamic characteristics ...continuedGND = 0 V; for test circuit see [Figure 10](#).

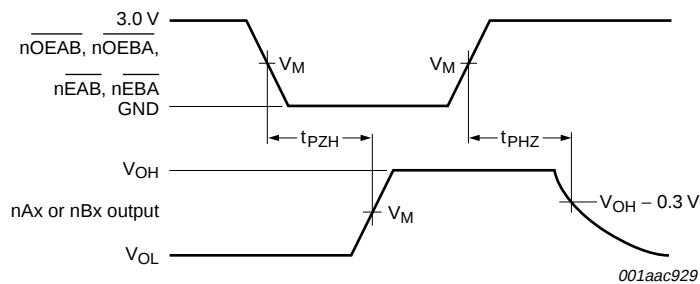
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t _{PLZ}	output disable time	see Figure 8				
	nOEBA to nAx, nOEAB to nBx		1.6	2.6	4.2	ns
	nEBA to nAx, nEAB to nBx		1.7	2.6	5.1	ns
t _{su(H)}	set-up time HIGH	see Figure 9				
	nAx to nLEAB, nBx to nLEBA		1.5	0.4	-	ns
	nAx to nEAB, nBx to nEBA		1.5	0.2	-	ns
t _{su(L)}	set-up time LOW	see Figure 9				
	nAx to nLEAB, nBx to nLEBA		+3.5	-0.1	-	ns
	nAx to nEAB, nBx to nEBA		+3.5	-0.3	-	ns
t _{h(H)}	hold time HIGH	see Figure 9				
	nAx to nLEAB, nBx to nLEBA		1.5	0.2	-	ns
	nAx to nEAB, nBx to nEBA		1.5	0.3	-	ns
t _{h(L)}	hold time LOW	see Figure 9				
	nAx to nLEAB, nBx to nLEBA		+2.0	-0.3	-	ns
	nAx to nEAB, nBx to nEBA		+2.0	-0.2	-	ns
t _{WL}	pulse width LOW	see Figure 9	4.0	3.1	-	ns
T_{amb} = -40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V						
t _{PLH}	propagation delay					
	nAx to nBx, nBx to nAx	see Figure 6	1.0	-	3.8	ns
	nLEBA to nAx, nLEAB to nBx	see Figure 5	1.0	-	5.2	ns
t _{PHL}	propagation delay					
	nAx to nBx, nBx to nAx	see Figure 6	1.0	-	5.1	ns
	nLEBA to nAx, nLEAB to nBx	see Figure 5	1.2	-	5.6	ns
t _{PZH}	output enable time	see Figure 7				
	nOEBA to nAx, nOEAB to nBx		1.0	-	5.2	ns
	nEBA to nAx, nEAB to nBx		1.0	-	6.2	ns
t _{PZL}	output enable time	see Figure 8				
	nOEBA to nAx, nOEAB to nBx		1.1	-	7.0	ns
	nEBA to nAx, nEAB to nBx		1.2	-	7.8	ns
t _{PHZ}	output disable time	see Figure 7				
	nOEBA to nAx, nOEAB to nBx		1.9	-	5.7	ns
	nEBA to nAx, nEAB to nBx		2.0	-	6.6	ns
t _{PLZ}	output disable time	see Figure 8				
	nOEBA to nAx, nOEAB to nBx		1.6	-	4.6	ns
	nEBA to nAx, nEAB to nBx		1.7	-	5.4	ns
t _{su(H)}	set-up time HIGH	see Figure 9				
	nAx to nLEAB, nBx to nLEBA		1.5	-	-	ns
	nAx to nEAB, nBx to nEBA		1.5	-	-	ns

Table 8: Dynamic characteristics ...continued
GND = 0 V; for test circuit see Figure 10.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(L)}$	set-up time LOW	see Figure 9				
	nAx to $\overline{nLEAB}$, nBx to $\overline{nLEBA}$		3.5	-	-	ns
	nAx to $\overline{nEAB}$, nBx to $\overline{nEBA}$		3.5	-	-	ns
$t_{h(H)}$	hold time HIGH	see Figure 9				
	nAx to $\overline{nLEAB}$, nBx to $\overline{nLEBA}$		1.5	-	-	ns
	nAx to $\overline{nEAB}$, nBx to $\overline{nEBA}$		1.5	-	-	ns
$t_{h(L)}$	hold time LOW	see Figure 9				
	nAx to $\overline{nLEAB}$, nBx to $\overline{nLEBA}$		2.0	-	-	ns
	nAx to $\overline{nEAB}$, nBx to $\overline{nEBA}$		2.0	-	-	ns
t_{WL}	pulse width LOW	see Figure 9	4.0	-	-	ns

12. Waveforms

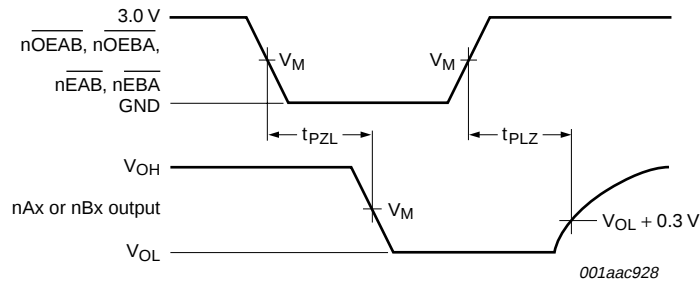




$V_M = 1.5 \text{ V}$.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

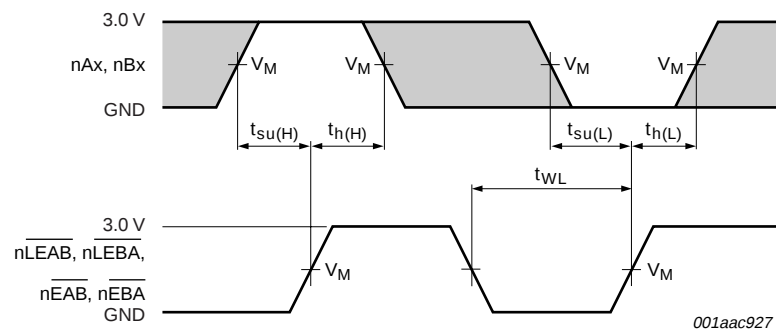
Fig 7. 3-state output enable time to HIGH-level and output disable time from HIGH-level state



$V_M = 1.5 \text{ V}$.

V_{OL} and V_{OH} are typical voltage output drop that occur with the output load.

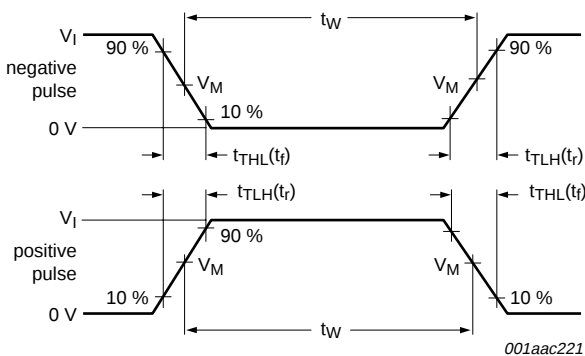
Fig 8. 3-state output enable time to LOW-level and output disable time from LOW-level state



$V_M = 1.5 \text{ V}$.

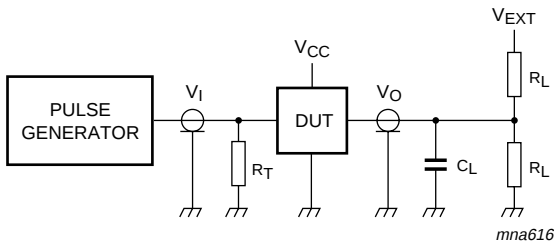
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. Data set-up and hold times and latch enable pulse width



$V_M = 1.5\text{ V}$.

a. Input pulse definition



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistor.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = Test voltage for switching times.

b. Test circuit

Fig 10. Load circuitry for switching times

Table 9: Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	$\leq 2.5\text{ ns}$	50 pF	500 Ω	open	7.0 V	open

13. Package outline

QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2 mm

SOT379-2

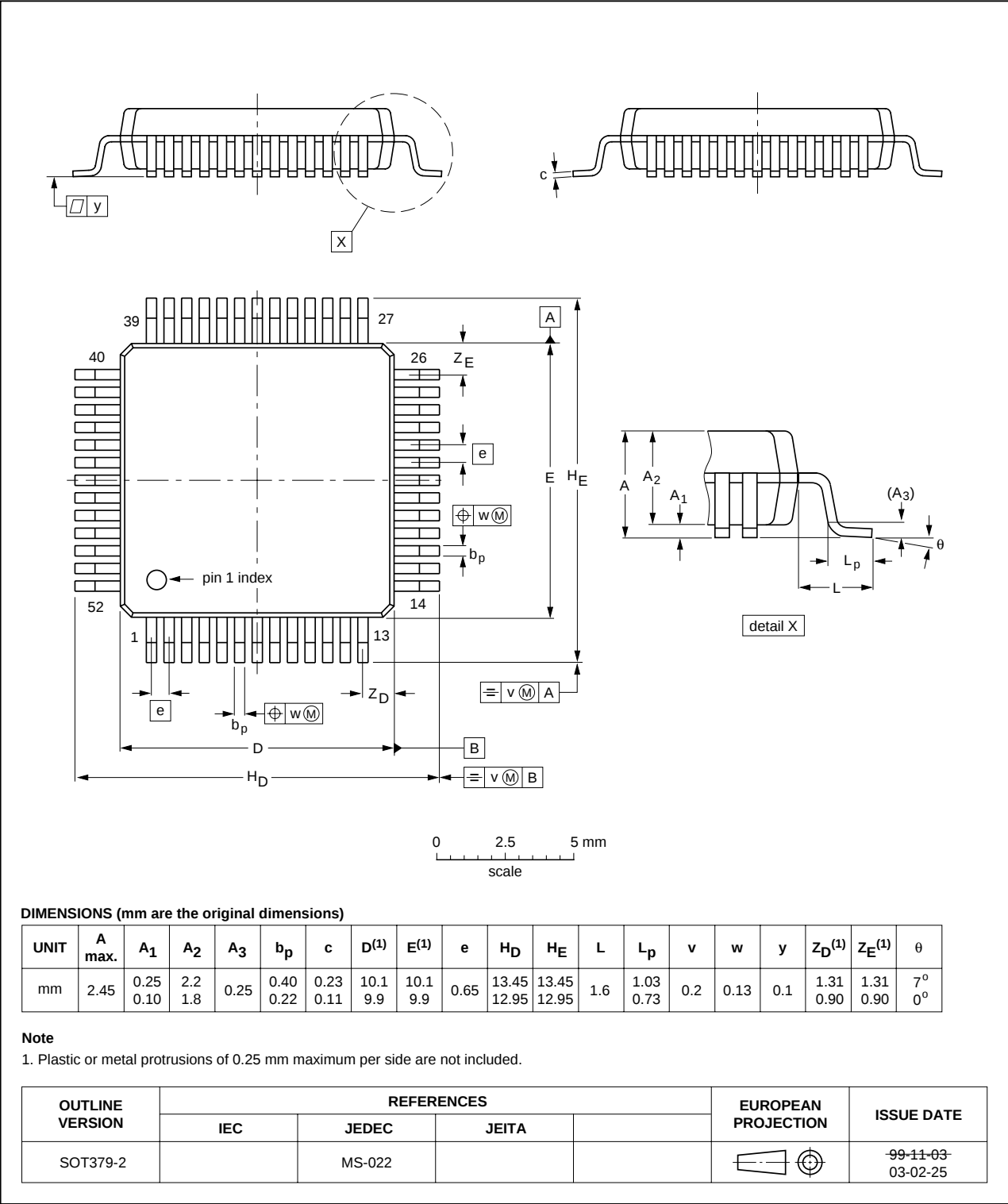


Fig 11. Package outline SOT379-2 (QFP52)

14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74ABT16543_4	20050526	Product data sheet	-	9397 750 15046	74ABT16543_3
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. Section 2 “Features”: Changed JEDEC Std 17 to JEDEC Std 78 - QFP52 package information added to and (T)SSOP56 packages removed from Section 4 “Ordering information”, Section 5 “Functional diagram”, Section 6 “Pinning information” and Section 13 “Package outline”					
74ABT16543_3	20020403	Product data sheet	-	9397 750 09692	-

15. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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