

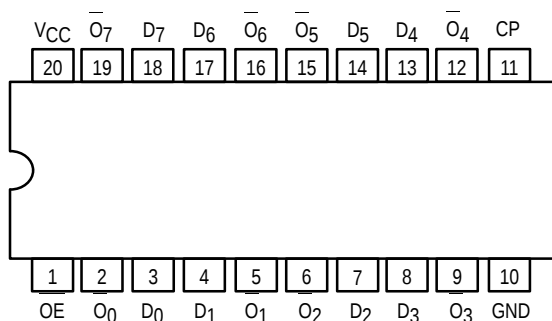


OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

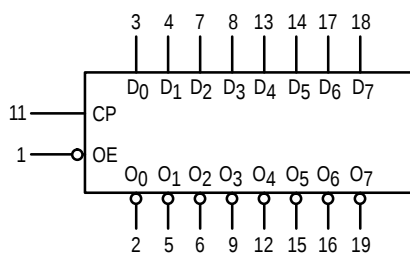
The MC54/74F534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The F534 is the same as the F374 except that the outputs are inverted.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus Oriented Applications

CONNECTION DIAGRAM



LOGIC SYMBOL

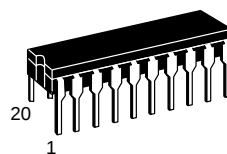


V_{CC} = PIN 20
GND = PIN 10

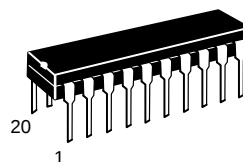
MC54/74F534

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

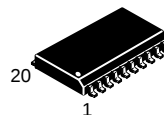
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

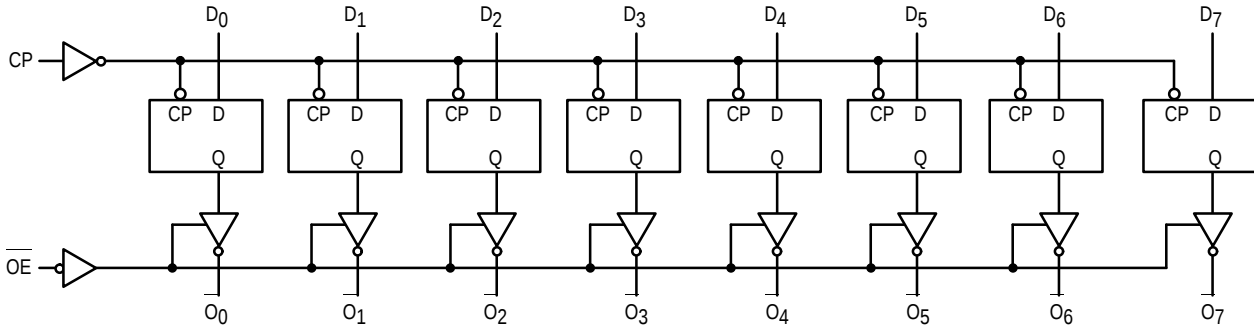
MC54FXXXJ	Ceramic
MC74FXXXN	Plastic
MC74FXXXDW	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I _{OH}	Output Current — High	54, 74			-3.0	mA
I _{OL}	Output Current — Low	54, 74			24	mA

MC54/74F534

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

FUNCTIONAL DESCRIPTION

The F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the

LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V _{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V _{IK}	Input Clamp Diode Voltage				-1.2	V	I _{IN} = -18 mA	V _{CC} = MIN
V _{OH}	Output HIGH Voltage	54, 74	2.4	3.3		V	I _{OH} = -3.0 mA	V _{CC} = 4.5 V
		74	2.7	3.3		V	I _{OH} = -3.0 mA	V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage			0.35	0.5	V	I _{OL} = 24 mA	V _{CC} = MIN
I _{OZH}	Output OFF Current — HIGH				50	μA	V _{OUT} = 2.7 V	V _{CC} = MAX
I _{OZL}	Output OFF Current — LOW				-50	μA	V _{OUT} = 0.5 V	V _{CC} = MAX
I _{IH}	Input HIGH Current				20	μA	V _{IN} = 2.7 V	V _{CC} = MAX
					100		V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.6	mA	V _{IN} = 0.5 V	V _{CC} = MAX
I _{OS}	Output Short Circuit Current (Note 2)		-60		-150	mA	V _{OUT} = 0 V	V _{CC} = MAX
I _{CCZ}	Power Supply Current			55	86	mA	D _A = Gnd OE = 4.5 V	V _{CC} = MAX

NOTES:

1. For conditions such as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

MC54/74F534

AC CHARACTERISTICS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF			T _A = -55 to +125°C V _{CC} = 5.0 V ±10% C _L = 50 pF		T _A = 0 to +70°C V _{CC} = 5.0 V ±10% C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100			60		70		MHz
t _{PLH} t _{PHL}	Propagation Delay CP to O _n	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11	4.0 4.0	10 10	ns
t _{PZH} t _{PZL}	Output Enable Time	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14 10	2.0 2.0	12.5 8.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	2.0 2.0	8.0 6.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	54/74F			54F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = -55 to +125°C V _{CC} = 5.0 V ±10%		T _A = 0 to +70°C V _{CC} = 5.0 V ±10%		
		Min	Typ	Max	Min	Max	Min	Max	
t _S (H) t _S (L)	Setup Time, HIGH or LOW D _N to CP	2.0 2.0			2.5 2.0		2.0 2.0		ns
t _H (H) t _H (L)	Hold Time, HIGH or LOW D _N to CP	2.0 2.0			2.0 2.5		2.0 2.0		
t _W (H) t _W (L)	CP Pulse Width HIGH or LOW	7.0 6.0			7.0 6.0		7.0 6.0		ns

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