

# TS1109 Data Sheet

## TS1109 Bidirectional Current-Sense Amplifier with Buffered Bipolar Output

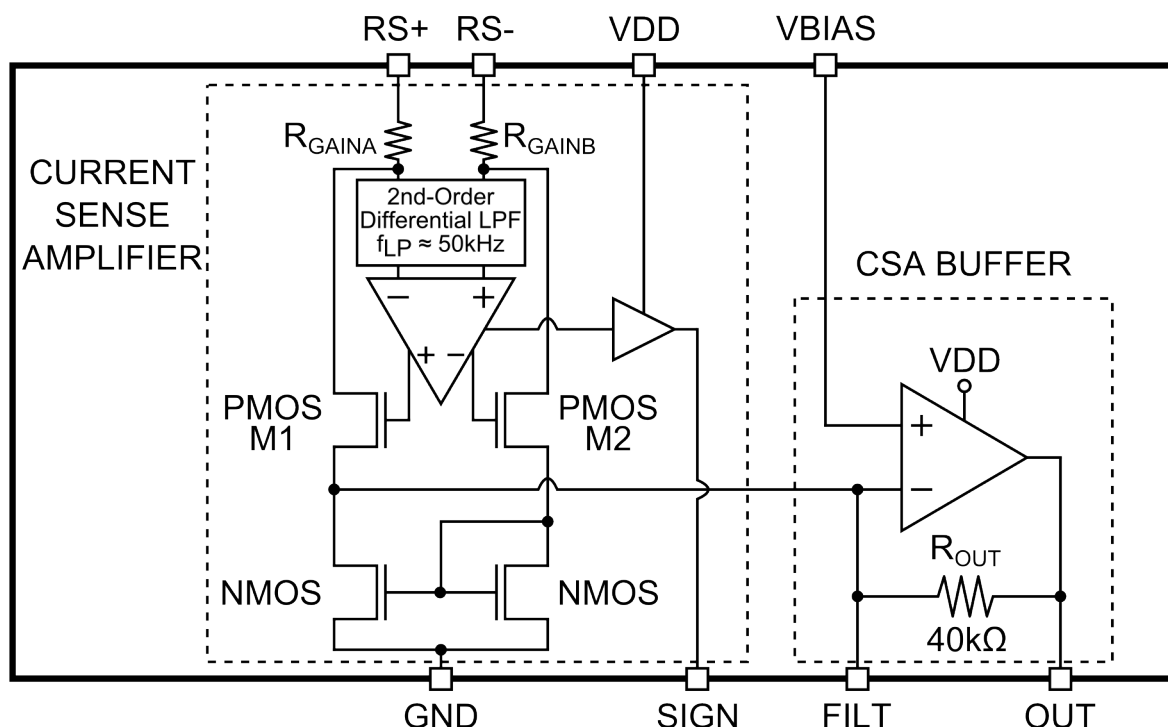
The TS1109 incorporates a bidirectional current-sense amplifier plus a buffered bipolar output with an adjustable bias. The internal configuration of the TS1109 high-side current-sense amplifier is a variation of the TS1101 bidirectional current-sense amplifier, consuming  $0.68 \mu\text{A}(\text{typ})$  and  $1.2 \mu\text{A}(\text{max})$ . The current-sense amplifier's buffered output consumes only  $0.76 \mu\text{A}(\text{typ})$  and  $1.3 \mu\text{A}(\text{max})$  of supply current. With an input offset voltage of  $150 \mu\text{V}(\text{max})$  and a gain error of  $1\%(\text{max})$ , the TS1109 is optimized for high precision current measurements

### Applications

- Power Management Systems
- Portable/Battery-Powered Systems
- Smart Chargers
- Battery Monitoring
- Overcurrent and Undercurrent Detection
- Remote Sensing
- Industrial Controls

### KEY FEATURES

- Low Supply Current
  - Current Sense Amplifier:  $0.68 \mu\text{A}$
  - $I_{\text{VDD}}$ :  $0.76 \mu\text{A}$
- High Side Bidirectional Current Sense Amplifier
- Wide CSA Input Common Mode Range:  $+2 \text{ V}$  to  $+27 \text{ V}$
- Low CSA Input Offset Voltage:  $150 \mu\text{V}(\text{max})$
- Low Gain Error:  $1\%(\text{max})$
- Two Gain Options Available:
  - Gain =  $20 \text{ V/V}$  : TS1109-20
  - Gain =  $200 \text{ V/V}$  : TS1109-200
- 8-Pin TDFN Packaging ( $3 \text{ mm} \times 3 \text{ mm}$ )



## 1. Ordering Information

**Table 1.1. Ordering Part Numbers**

| Ordering Part Number                                                                                  | Description                                                        | Gain V/V |
|-------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------|----------|
| TS1109-20IDT833                                                                                       | Bidirectional current sense amplifier with buffered bipolar output | 20       |
| TS1109-200 IDT833                                                                                     | Bidirectional current sense amplifier with buffered bipolar output | 200      |
| <b>Note:</b> Adding the suffix “T” to the part number (e.g. TS1109-200IDT833T) denotes tape and reel. |                                                                    |          |

## 2. System Overview

### 2.1 Functional Block Diagram

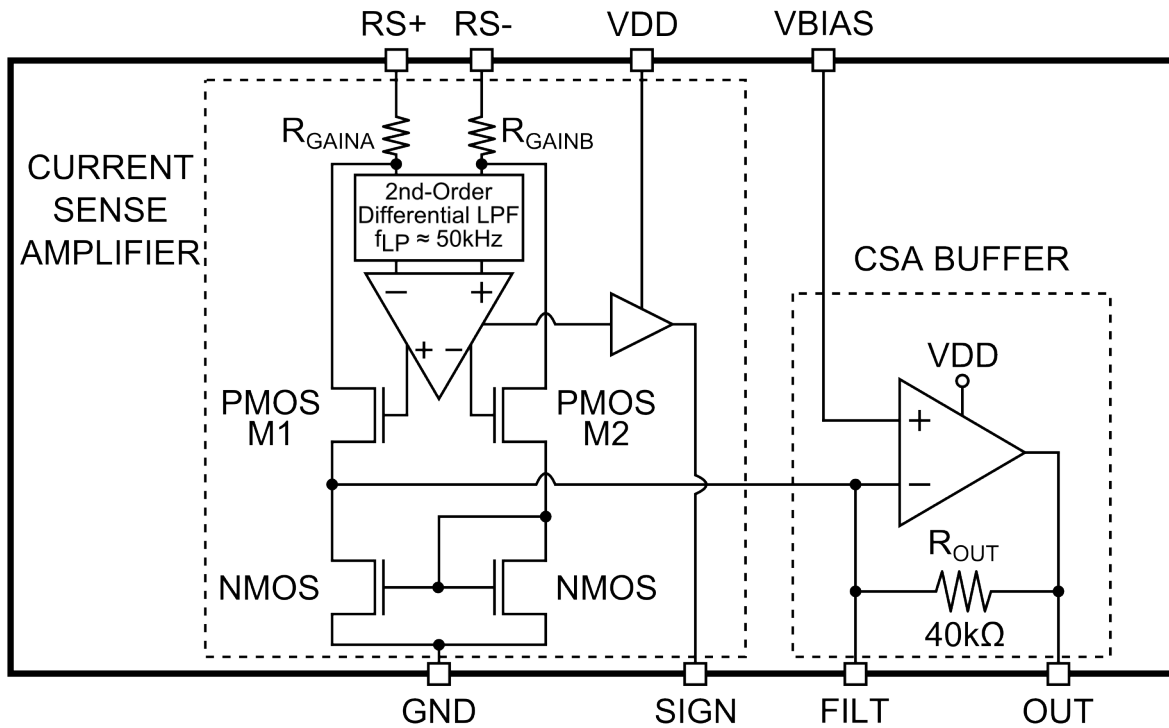


Figure 2.1. TS1109 Bidirectional Bipolar Buffered Current Sense Amplifier Block Diagram

## 2.2 Current Sense Amplifier + Output Buffer

The internal configuration of the TS1109 bidirectional current-sense amplifier is a variation of the TS1101 bidirectional current-sense amplifier. The TS1109 current-sense amplifier is configured for fully differential input/output operation.

Referring to the block diagram, the inputs of the TS1109's differential input/output amplifier are connected to RS+ and RS– across an external  $R_{SENSE}$  resistor that is used to measure current. At the non-inverting input of the current-sense amplifier, the applied voltage difference in voltage between RS+ and RS– is  $I_{LOAD} \times R_{SENSE}$ . Since the RS– terminal is the non-inverting input of the internal op-amp, the current-sense op-amp action drives PMOS[1/2] to drive current across  $R_{GAIN[A/B]}$  to equalize voltage at its inputs.

Thus, since the M1 PMOS source is connected to the inverting input of the internal op-amp and since the voltage drop across  $R_{GAINA}$  is the same as the external  $V_{SENSE}$ , the M1 PMOS' drain-source current is equal to:

$$I_{DS(M1)} = \frac{V_{SENSE}}{R_{GAINA}}$$

$$I_{DS(M1)} = \frac{I_{LOAD} \times R_{SENSE}}{R_{GAINA}}$$

The drain terminal of the M1 PMOS is connected to the transimpedance amplifier's gain resistor,  $R_{OUT}$ , via the inverting terminal. The non-inverting terminal of the transimpedance amplifier is internally connected to VBIAS, therefore the output voltage of the TS1109 at the OUT terminal is:

$$V_{OUT} = V_{BIAS} - I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAINA}}$$

When the voltage at the RS– terminal is greater than the voltage at the RS+ terminal, the external  $V_{SENSE}$  voltage drop is impressed upon  $R_{GAINB}$ . The voltage drop across  $R_{GAINB}$  is then converted into a current by the M2 PMOS. The M2 PMOS drain-source current is the input current for the NMOS current mirror which is matched with a 1-to-1 ratio. The transimpedance amplifier sources the M2 PMOS drain-source current for the NMOS current mirror. Therefore, the output voltage of the TS1109 at the OUT terminal is:

$$V_{OUT} = V_{BIAS} + I_{LOAD} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAINB}}$$

When M1 is conducting current ( $V_{RS+} > V_{RS-}$ ), the TS1109's internal amplifier holds M2 OFF. When M2 is conducting current ( $V_{RS-} > V_{RS+}$ ), the internal amplifier holds M1 OFF. In either case, the disabled PMOS does not contribute to the resultant output voltage.

The current-sense amplifier's gain accuracy is therefore the ratio match of  $R_{OUT}$  to  $R_{GAIN[A/B]}$ . For each of the two gain options available, The following table lists the values for  $R_{GAIN[A/B]}$ .

**Table 2.1. Internal Gain Setting Resistors (Typical Values)**

| GAIN (V/V) | $R_{GAIN[A/B]}$ (Ω) | $R_{OUT}$ (Ω) | Part Number |
|------------|---------------------|---------------|-------------|
| 20         | 2 k                 | 40 k          | TS1109-20   |
| 200        | 200                 | 40 k          | TS1109-200  |

The TS1109 allows access to the inverting terminal of the transimpedance amplifier by the FILT pin, whereby a series RC filter may be connected to reduce noise at the OUT terminal. The recommended RC filter is 4 kΩ and 0.47 μF connected in series from FILT to GND to suppress the noise. Any capacitance at the OUT terminal should be minimized for stable operation of the buffer.

## 2.3 Sign Output

The TS1109 SIGN output indicates the load current's direction. The SIGN output is a logic HIGH when M1 is conducting current ( $V_{RS+} > V_{RS-}$ ). Alternatively, the SIGN output is a logic LOW when M2 is conducting current ( $V_{RS-} > V_{RS+}$ ). The SIGN comparator's transfer characteristic is illustrated in the figure below. Unlike other current-sense amplifiers that implement an OUT/SIGN arrangement, the TS1109 exhibits no "dead zone" at  $I_{LOAD}$  switchover.

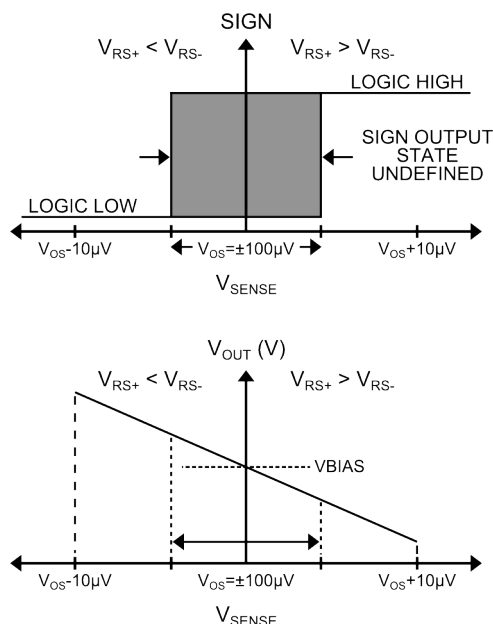


Figure 2.2. TS1109 Sign Output Transfer Characteristic

## 2.4 Selecting a Sense Resistor

Selecting the optimal value for the external  $R_{SENSE}$  is based on the following criteria and for each commentary follows:

1.  $R_{SENSE}$  Voltage Loss
2.  $V_{OUT}$  Swing vs. Desired  $V_{SENSE}$  and Applied Supply Voltage at VDD
3. Total  $I_{LOAD}$  Accuracy
4. Circuit Efficiency and Power Dissipation
5.  $R_{SENSE}$  Kelvin Connections

### 2.4.1 RSENSE Voltage Loss

For lowest IR power dissipation in  $R_{SENSE}$ , the smallest usable resistor value for  $R_{SENSE}$  should be selected.

## 2.4.2 VOUT Swing vs. Desired VSENSE and Applied Supply Voltage at VDD

Although the Current Sense Amplifier draws its power from the voltage at its RS+ and RS– terminals, the signal voltage at the OUT terminal is provided by a buffer, and is therefore bounded by the buffer's output range. As shown in the Electrical Characteristics table, the CSA Buffer has a maximum and minimum output voltage of:

$$V_{OUT(max)} = VDD_{(min)} - 0.2V$$

$$V_{OUT(min)} = 0.2V$$

Therefore, the full-scale sense voltage should be chosen so that the OUT voltage is neither greater nor less than the maximum and minimum output voltage defined above. To satisfy this requirement, the positive full-scale sense voltage,  $V_{SENSE(pos\_max)}$ , should be chosen so that:

$$V_{SENSE(pos\_max)} < \frac{VBIAS - V_{OUT(min)}}{GAIN}$$

Likewise, the negative full-scale sense voltage,  $V_{SENSE(neg\_min)}$ , should be chosen so that:

$$V_{SENSE(neg\_min)} < \frac{V_{OUT(max)} - VBIAS}{GAIN}$$

For best performance,  $R_{SENSE}$  should be chosen so that the full-scale  $V_{SENSE}$  is less than  $\pm 75$  mV.

## 2.4.3 Total Load Current Accuracy

In the TS1109's linear region where  $V_{OUT(min)} < V_{OUT} < V_{OUT(max)}$ , there are two specifications related to the circuit's accuracy: a) the TS1109 CSA's input offset voltage ( $V_{OS(max)} = 150 \mu V$ ), b) the TS1109 CSA's gain error ( $GE_{(max)} = 1\%$ ). An expression for the TS1109's total error is given by:

$$V_{OUT} = VBIAS - [GAIN \times (1 \pm GE) \times V_{SENSE}] \pm (GAIN \times V_{OS})$$

A large value for  $R_{SENSE}$  permits the use of smaller load currents to be measured more accurately because the effects of offset voltages are less significant when compared to larger  $V_{SENSE}$  voltages. Due care though should be exercised as previously mentioned with large values of  $R_{SENSE}$ .

## 2.4.4 Circuit Efficiency and Power Dissipation

IR losses in  $R_{SENSE}$  can be large especially at high load currents. It is important to select the smallest, usable  $R_{SENSE}$  value to minimize power dissipation and to keep the physical size of  $R_{SENSE}$  small. If the external  $R_{SENSE}$  is allowed to dissipate significant power, then its inherent temperature coefficient may alter its design center value, thereby reducing load current measurement accuracy. Precisely because the TS1109 CSA's input stage was designed to exhibit a very low input offset voltage, small  $R_{SENSE}$  values can be used to reduce power dissipation and minimize local hot spots on the pcb.

## 2.4.5 RSENSE Kelvin Connections

For optimal  $V_{SENSE}$  accuracy in the presence of large load currents, parasitic pcb track resistance should be minimized. Kelvin-sense pcb connections between  $R_{SENSE}$  and the TS1109's RS+ and RS– terminals are strongly recommended. The drawing below illustrates the connections between the current-sense amplifier and the current-sense resistor. The pcb layout should be balanced and symmetrical to minimize wiring-induced errors. In addition, the pcb layout for  $R_{SENSE}$  should include good thermal management techniques for optimal  $R_{SENSE}$  power dissipation.

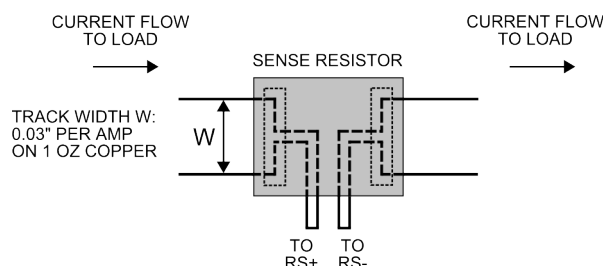


Figure 2.3. Making PCB Connections to  $R_{SENSE}$

### 2.4.6 RSENSE Composition

Current-shunt resistors are available in metal film, metal strip, and wire-wound constructions. Wire-wound current-shunt resistors are constructed with wire spirally wound onto a core. As a result, these types of current shunt resistors exhibit the largest self-inductance. In applications where the load current contains high-frequency transients, metal film or metal strip current sense resistors are recommended.

### 2.4.7 Internal Noise Filter

In power management and motor control applications, current-sense amplifiers are required to measure load currents accurately in the presence of both externally-generated differential and common-mode noise. An example of differential-mode noise that can appear at the inputs of a current-sense amplifier is high-frequency ripple. High-frequency ripple (whether injected into the circuit inductively or capacitively) can produce a differential-mode voltage drop across the external current-shunt resistor,  $R_{SENSE}$ . An example of externally-generated, common-mode noise is the high-frequency output ripple of a switching regulator that can result in common-mode noise injection into both inputs of a current-sense amplifier.

Even though the load current signal bandwidth is dc, the input stage of any current-sense amplifier can rectify unwanted, out-of-band noise that can result in an apparent error voltage at its output. Against common-mode injection noise, the current-sense amplifier's internal common-mode rejection ratio is 130 dB (typ).

To counter the effects of externally-injected noise, the TS1109 incorporates a 50 kHz (typ), 2nd-order differential low-pass filter as shown in the TS1109's block diagram, thereby eliminating the need for an external low-pass filter, which can generate errors in the offset voltage and the gain error.

### 2.4.8 PC Board Layout and Power-Supply Bypassing

For optimal circuit performance, the TS1109 should be in very close proximity to the external current-sense resistor, and the pcb tracks from  $R_{SENSE}$  to the  $RS+$  and the  $RS-$  input terminals of the TS1109 should be short and symmetric. Also recommended are surface mount resistors and capacitors, as well as a ground plane.

### 3. Electrical Characteristics

**Table 3.1. Recommended Operating Conditions<sup>1</sup>**

| Parameter                                                                                                                                                | Symbol          | Conditions                            | Min | Typ | Max  | Units |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------------------|-----|-----|------|-------|
| System Specifications                                                                                                                                    |                 |                                       |     |     |      |       |
| Operating Voltage Range                                                                                                                                  | VDD             |                                       | 1.7 | —   | 5.25 | V     |
| Common-Mode Input Range                                                                                                                                  | V <sub>CM</sub> | V <sub>RS+</sub> , Guaranteed by CMRR | 2   | —   | 27   | V     |
| <b>Note:</b><br>1. All devices 100% production tested at T <sub>A</sub> = +25 °C. Limits over Temperature are guaranteed by design and characterization. |                 |                                       |     |     |      |       |

**Table 3.2. DC Characteristics<sup>1</sup>**

| Parameter                               | Symbol                              | Conditions                       | Min | Typ  | Max       | Units |
|-----------------------------------------|-------------------------------------|----------------------------------|-----|------|-----------|-------|
| System Specifications                   |                                     |                                  |     |      |           |       |
| No Load Input Supply Current            | I <sub>RS+</sub> + I <sub>RS−</sub> | See Note 2                       | —   | 0.68 | 1.2       | μA    |
|                                         | I <sub>VDD</sub>                    |                                  | —   | 0.76 | 1.3       | μA    |
| Current Sense Amplifier                 |                                     |                                  |     |      |           |       |
| Common Mode Rejection Ratio             | CMRR                                | 2 V < V <sub>RS+</sub> < 27 V    | 120 | 130  | —         | dB    |
| Input Offset Voltage (See Note 3)       | V <sub>OS</sub>                     | T <sub>A</sub> = +25 °C          | —   | ±100 | ±150      | μV    |
|                                         |                                     | −40 °C < T <sub>A</sub> < +85 °C | —   | —    | ±200      | μV    |
| V <sub>OS</sub> Hysteresis (See Note 4) | V <sub>HYS</sub>                    | T <sub>A</sub> = +25 °C          | —   | 10   | —         | μV    |
| Gain                                    | G                                   | TS1109-20                        | —   | 20   | —         | V/V   |
|                                         |                                     | TS1109-200                       | —   | 200  | —         |       |
| Positive Gain Error (See Note 5)        | GE+                                 | T <sub>A</sub> = +25 °C          | —   | ±0.1 | ±0.6      | %     |
|                                         |                                     | −40 °C < T <sub>A</sub> < +85 °C | —   | —    | ±1        | %     |
| Negative Gain Error (See Note 5)        | GE−                                 | T <sub>A</sub> = +25 °C          | —   | ±0.6 | ±1        | %     |
|                                         |                                     | −40 °C < T <sub>A</sub> < +85 °C | —   | —    | ±1.4      | %     |
| Gain Match (See Note 5)                 | GM                                  | T <sub>A</sub> = +25 °C          | —   | ±0.6 | ±1        | %     |
|                                         |                                     | −40 °C < T <sub>A</sub> < +85 °C | —   | —    | ±1.4      | %     |
| Transfer Resistance                     | R <sub>OUT</sub>                    | From FILT to OUT                 | 28  | 40   | 52.8      | kΩ    |
| CSA Buffer                              |                                     |                                  |     |      |           |       |
| Input Bias Current                      | I <sub>Buffer_BIAS</sub>            | −40 °C < T <sub>A</sub> < +85 °C | —   | 0.3  | —         | nA    |
| Input referred DC Offset                | V <sub>Buffer_OS</sub>              |                                  | —   | —    | ±2.5      | mV    |
| Offset Drift                            | TCV <sub>Buffer_OS</sub>            | −40 °C < T <sub>A</sub> < +85 °C | —   | 0.6  | —         | μV/°C |
| Input Common Mode Range                 | V <sub>Buffer_CM</sub>              | −40C < T <sub>A</sub> < +85 °C   | 0.2 | —    | VDD − 0.2 | V     |
| Output Range                            | V <sub>OUT(min,max)</sub>           | I <sub>OUT</sub> = ±150 μA       | 0.2 | —    | VDD − 0.2 | V     |
| Sign Comparator Parameters              |                                     |                                  |     |      |           |       |

| Parameter           | Symbol                | Conditions                                                             | Min                   | Typ | Max | Units |
|---------------------|-----------------------|------------------------------------------------------------------------|-----------------------|-----|-----|-------|
| Output Low Voltage  | $V_{\text{SIGN\_OL}}$ | $V_{\text{DD}} = 1.8 \text{ V}$ , $I_{\text{SINK}} = 35 \mu\text{A}$   | —                     | —   | 0.2 | V     |
| Output High Voltage | $V_{\text{SIGN\_OH}}$ | $V_{\text{DD}} = 1.8 \text{ V}$ , $I_{\text{SOURCE}} = 35 \mu\text{A}$ | $V_{\text{DD}} - 0.2$ | —   | —   | V     |

**Note:**

1.  $R_{\text{S+}} = R_{\text{S-}} = 3.6 \text{ V}$ ,  $V_{\text{SENSE}} = (V_{\text{RS+}} - V_{\text{RS-}}) = 0 \text{ V}$ ,  $V_{\text{DD}} = 3 \text{ V}$ ,  $V_{\text{BIAS}} = 1.5 \text{ V}$ ,  $F_{\text{ILT}}$  connected to  $4 \text{ kW}$  and  $470 \text{ nF}$  in series to GND.  $T_{\text{A}} = T_{\text{J}} = -40 \text{ }^{\circ}\text{C}$  to  $+85 \text{ }^{\circ}\text{C}$  unless otherwise noted. Typical values are at  $T_{\text{A}} = +25 \text{ }^{\circ}\text{C}$ .
2. Extrapolated to  $V_{\text{OUT}} = V_{\text{FILT}}$ .  $I_{\text{RS+}} + I_{\text{RS-}}$  is the total current into the  $R_{\text{S+}}$  and the  $R_{\text{S-}}$  pins.
3. Input offset voltage  $V_{\text{OS}}$  is extrapolated from a  $V_{\text{OUT}(+)}$  measurement with  $V_{\text{SENSE}}$  set to  $+1 \text{ mV}$  and a  $V_{\text{OUT}(-)}$  measurement with  $V_{\text{SENSE}}$  set to  $-1 \text{ mV}$ ; Average  $V_{\text{OS}} = (V_{\text{OUT}(-)} - V_{\text{OUT}(+)}) / (2 \times \text{GAIN})$ .
4. Amplitude of  $V_{\text{SENSE}}$  lower or higher than  $V_{\text{OS}}$  required to cause the comparator to switch output states.
5. Gain error is calculated by applying two values for  $V_{\text{SENSE}}$  and then calculating the error of the actual slope vs. the ideal transfer characteristic: For  $\text{GAIN} = 20 \text{ V/V}$ , the applied  $V_{\text{SENSE}}$  for  $\text{GE} \pm$  is  $\pm 25 \text{ mV}$  and  $\pm 60 \text{ mV}$ . For  $\text{GAIN} = 200 \text{ V/V}$ , the applied  $V_{\text{SENSE}}$  for  $\text{GE} \pm$  is  $\pm 2.5 \text{ mV}$  and  $\pm 6 \text{ mV}$ .

**Table 3.3. AC Characteristics**

| Parameter              | Symbol                | Conditions                                       | Min           | Typ | Max  | Units |
|------------------------|-----------------------|--------------------------------------------------|---------------|-----|------|-------|
| <b>CSA Buffer</b>      |                       |                                                  |               |     |      |       |
| Output Settling time   | $t_{\text{OUT\_S}}$   | 1% Final value, $V_{\text{OUT}} = 1.3 \text{ V}$ | Gain = 20 V/V | —   | 1.35 | msec  |
| <b>Sign Comparator</b> |                       |                                                  |               |     |      |       |
| Propagation Delay      | $t_{\text{SIGN\_PD}}$ | $V_{\text{SENSE}} = \pm 1 \text{ mV}$            |               | —   | 3    | msec  |
|                        |                       | $V_{\text{SENSE}} = \pm 10 \text{ mV}$           |               | 0.4 | —    | msec  |

**Table 3.4. Thermal Conditions**

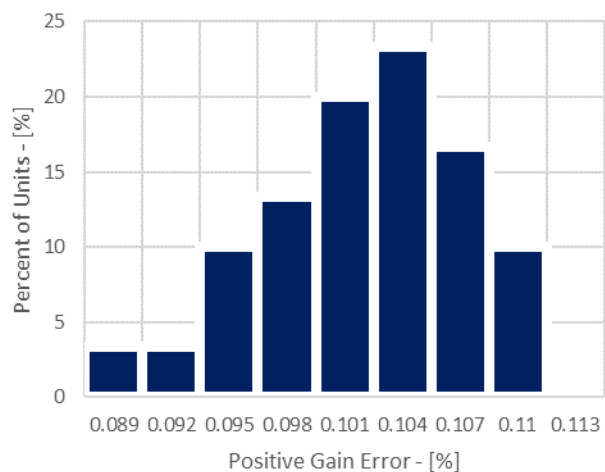
| Parameter                   | Symbol          | Conditions | Min | Typ | Max | Units              |
|-----------------------------|-----------------|------------|-----|-----|-----|--------------------|
| Operating Temperature Range | $T_{\text{OP}}$ |            | -40 | —   | +85 | $^{\circ}\text{C}$ |

**Table 3.5. Absolute Maximum Limits**

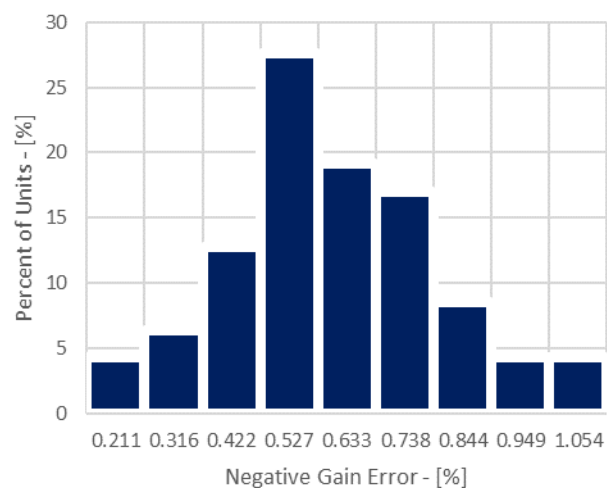
| Parameter                          | Symbol              | Conditions | Min  | Typ | Max        | Units |
|------------------------------------|---------------------|------------|------|-----|------------|-------|
| RS+ Voltage                        | $V_{RS+}$           |            | −0.3 | —   | 27         | V     |
| RS− Voltage                        | $V_{RS-}$           |            | −0.3 | —   | 27         | V     |
| Supply Voltage                     | VDD                 |            | −0.3 | —   | 6          | V     |
| OUT Voltage                        | $V_{OUT}$           |            | −0.3 | —   | 6          | V     |
| SIGN Voltage                       | $V_{SIGN}$          |            | −0.3 | —   | 6          | V     |
| FILT Voltage                       | $V_{FILT}$          |            | −0.3 | —   | 6          | V     |
| VBIAS Voltage                      | $V_{VBIAS}$         |            | −0.3 | —   | VDD + 0.3  | V     |
| RS+ to RS− Voltage                 | $V_{RS+} - V_{RS-}$ |            | —    | —   | 27         | V     |
| Short Circuit Duration: OUT to GND |                     |            | —    | —   | Continuous |       |
| Continuous Input Current (Any Pin) |                     |            | −20  | —   | 20         | mA    |
| Junction Temperature               |                     |            | —    | —   | 150        | °C    |
| Storage Temperature Range          |                     |            | −65  | —   | 150        | °C    |
| Lead Temperature (Soldering, 10 s) |                     |            | —    | —   | 300        | °C    |
| Soldering Temperature (Reflow)     |                     |            | —    | —   | 260        | °C    |
| <b>ESD Tolerance</b>               |                     |            |      |     |            |       |
| Human Body Model                   |                     |            | —    | —   | 2000       | V     |
| Machine Model                      |                     |            | —    | —   | 200        | V     |

For the following graphs,  $V_{RS+} = V_{RS-} = 3.6\text{ V}$ ;  $V_{DD} = 3\text{ V}$ ;  $V_{BIAS} = 1.5\text{ V}$ , and  $T_A = +25\text{ °C}$  unless otherwise noted.

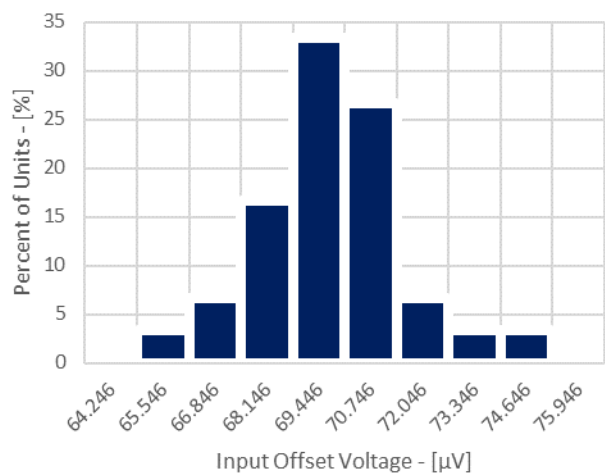
Positive Gain Error Histogram



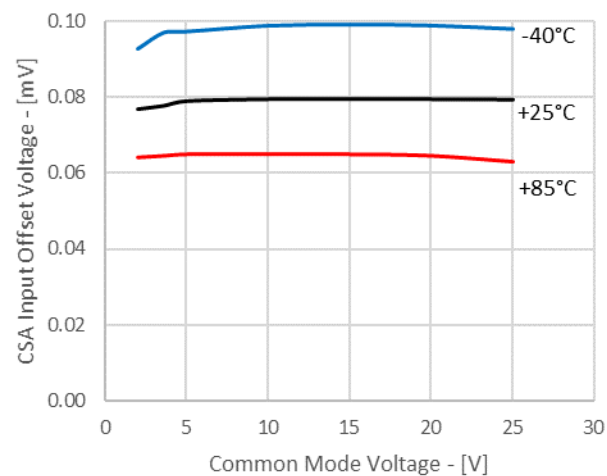
Negative Gain Error Histogram



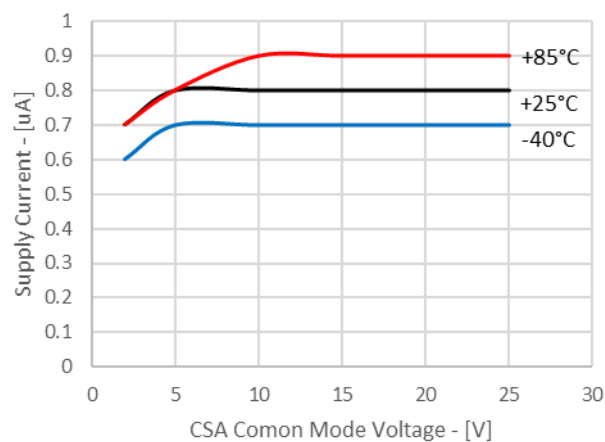
CSA Input Offset Voltage Histogram



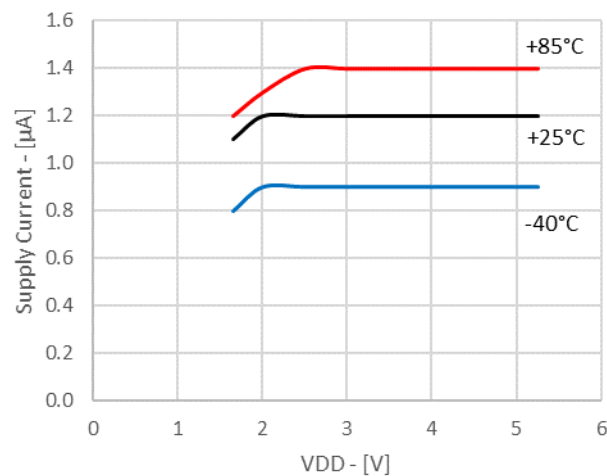
CSA Input Offset vs Common Mode Voltage



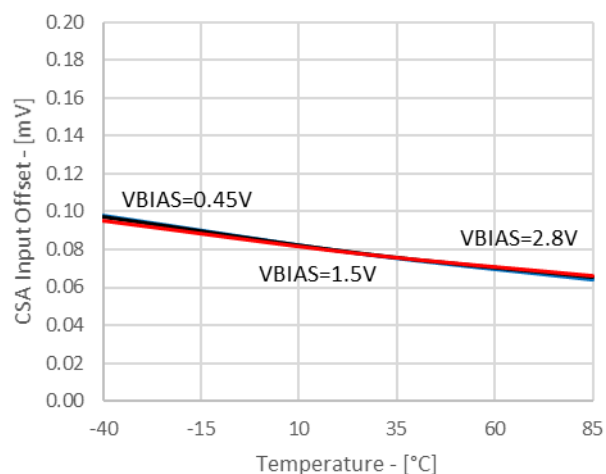
CSA Supply Current vs Common Mode Voltage



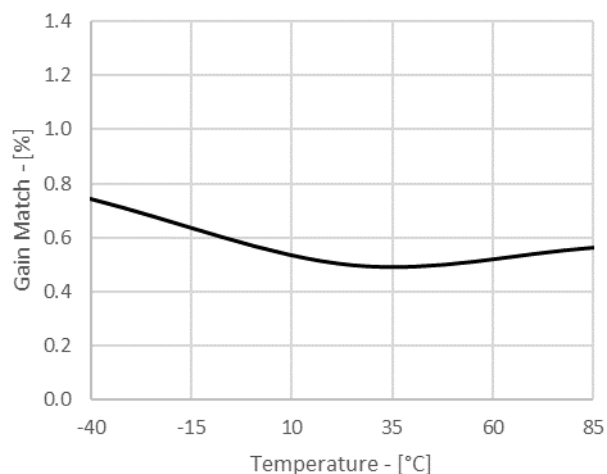
Supply Current vs VDD



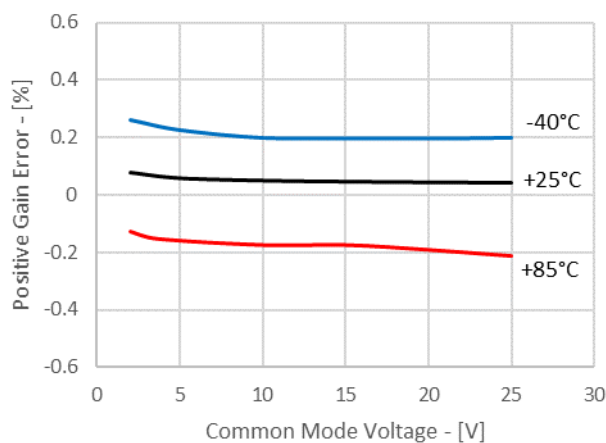
CSA Input Offset vs Temperature



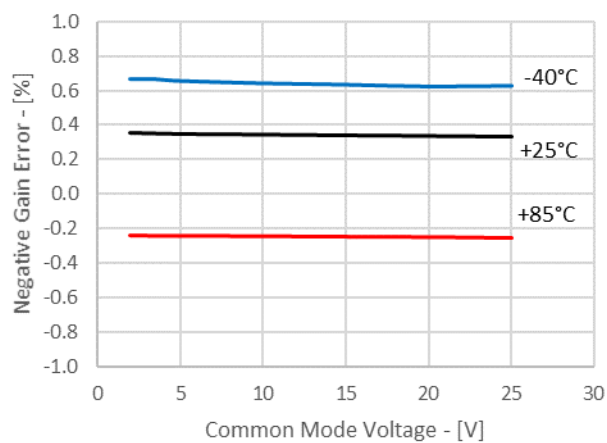
Gain Match vs Temperature



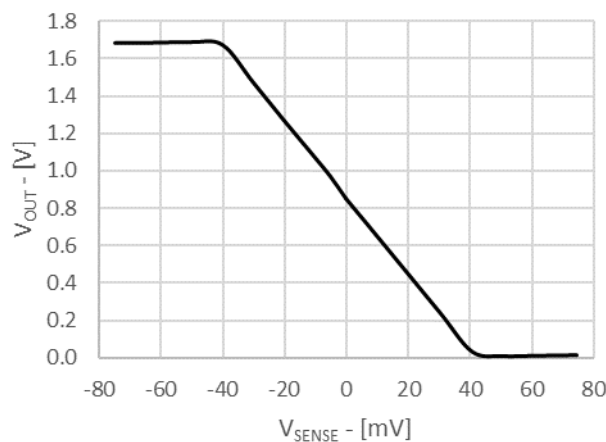
Positive Gain Error vs Common Mode Voltage



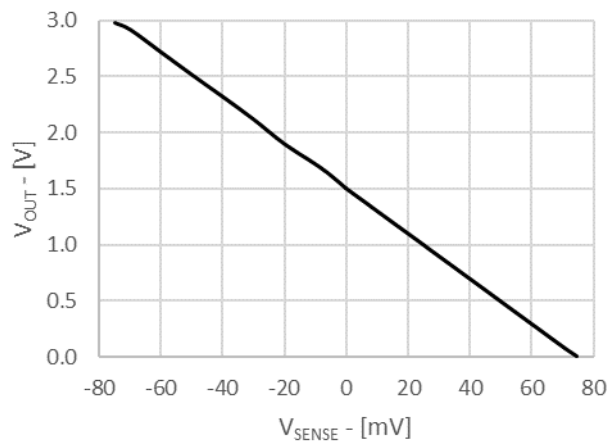
Negative Gain Error vs Common Mode Voltage

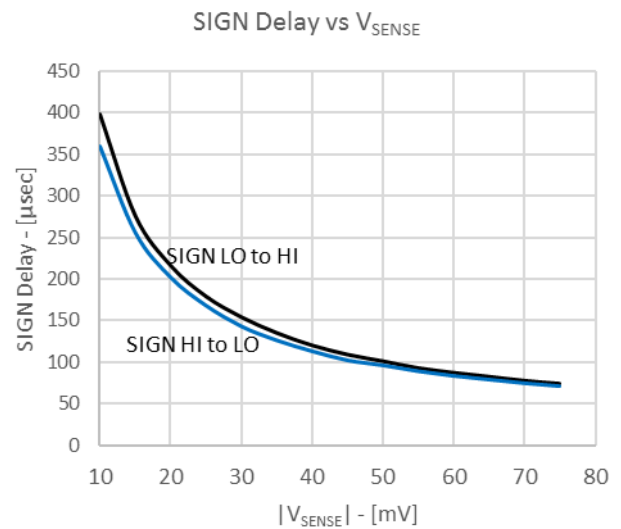
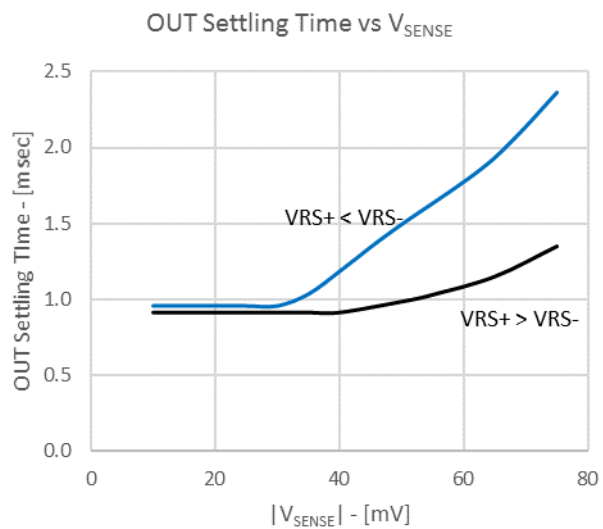
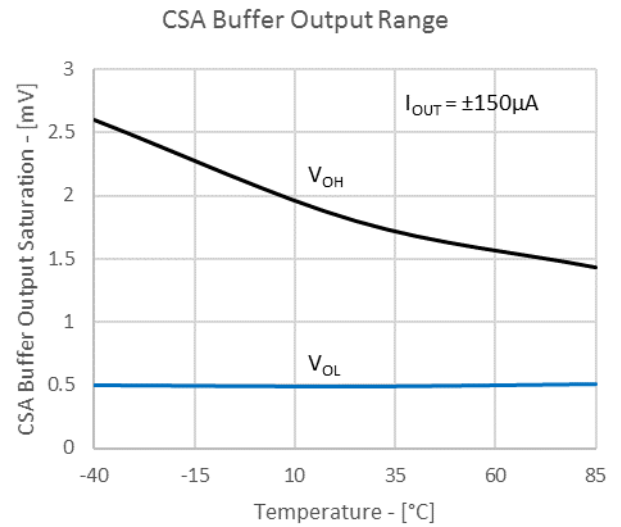
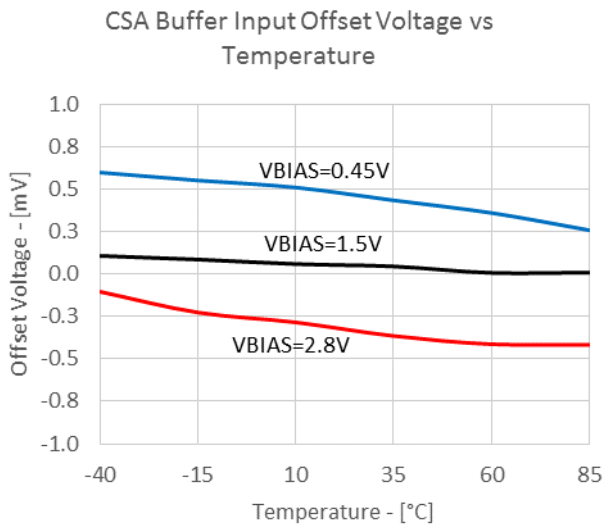
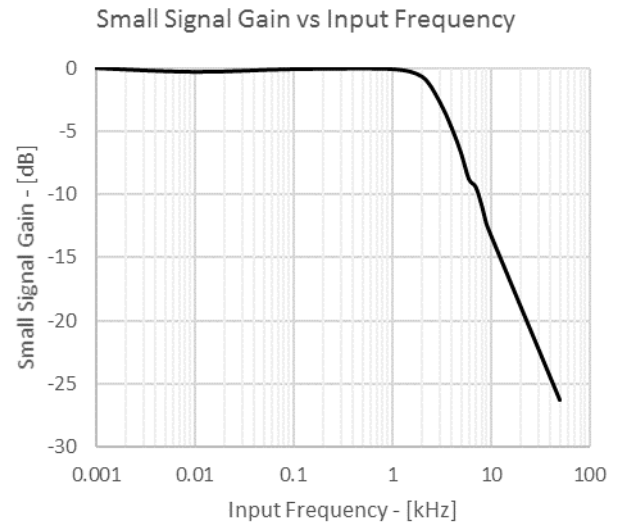
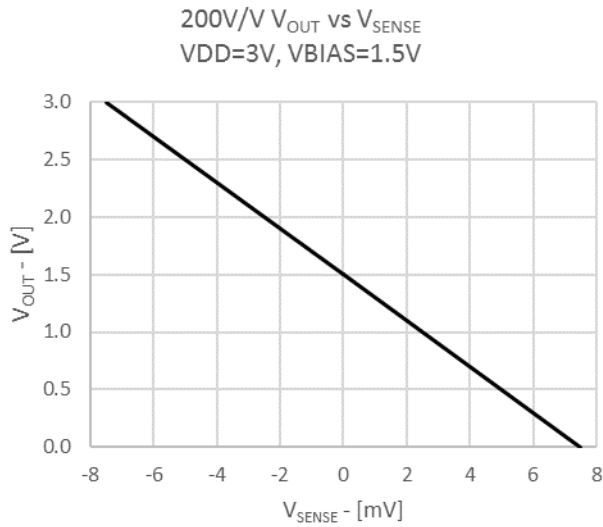


20V/V  $V_{OUT}$  vs  $V_{SENSE}$   
VDD=1.7V, VBIAS=0.85V

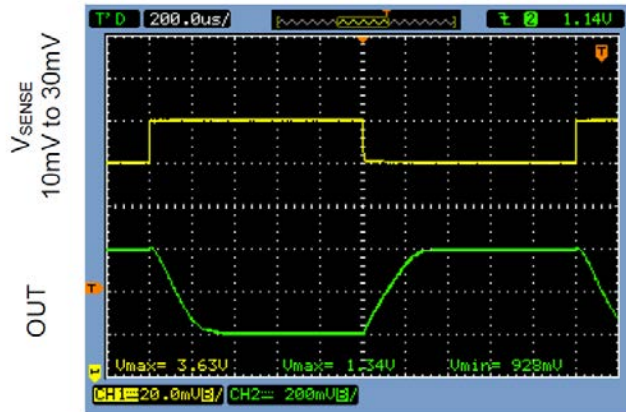


20V/V  $V_{OUT}$  vs  $V_{SENSE}$   
VDD=3V, VBIAS=1.5V

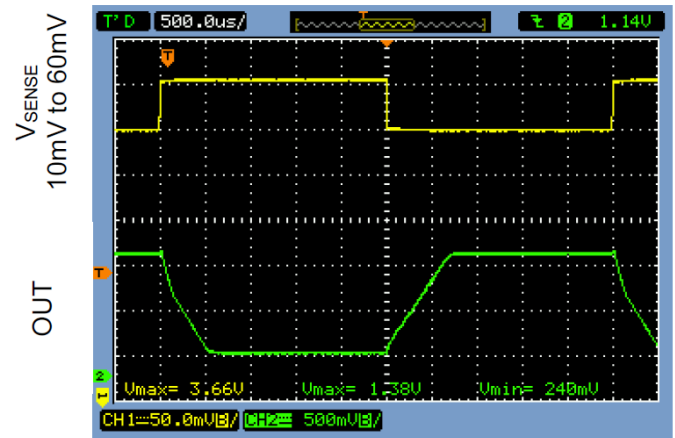




Small Signal Pulse Response



Large Signal Pulse Response



#### 4. Typical Application Circuit

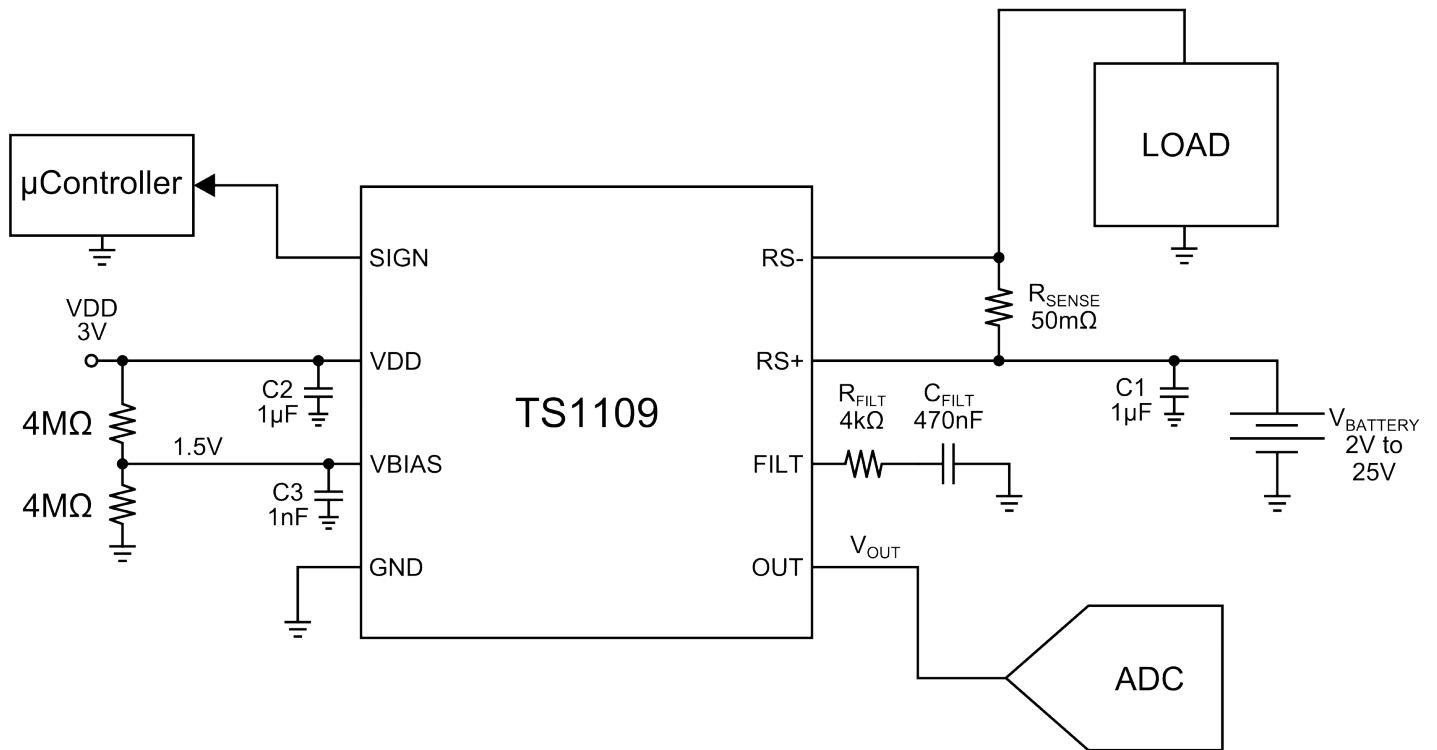
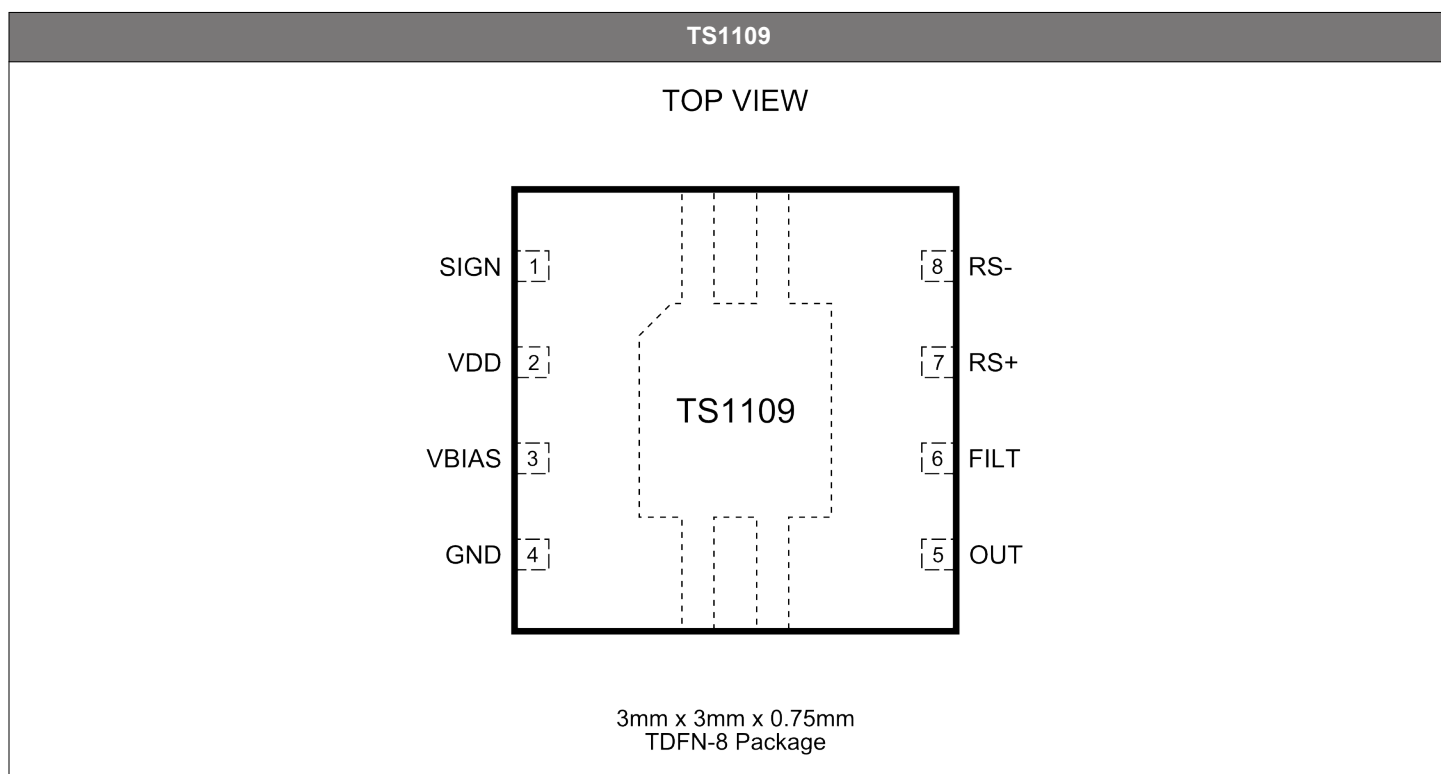


Figure 4.1. TS1109 Typical Application Circuit

## 5. Pin Descriptions



**Table 5.1. Pin Descriptions**

| Pin         | Label | Function                                                                                                             |
|-------------|-------|----------------------------------------------------------------------------------------------------------------------|
| 1           | SIGN  | Sign output. SIGN is HIGH for $V_{RS+} > V_{RS-}$ and LOW for $V_{RS-} > V_{RS+}$ .                                  |
| 2           | VDD   | External power supply pin. Connect this to the system's VDD supply.                                                  |
| 3           | VBIAS | Bias voltage for CSA output. When VREF is activated, leave open.                                                     |
| 4           | GND   | Ground. Connect to analog ground.                                                                                    |
| 5           | OUT   | CSA buffered output. Connect to CIN-.                                                                                |
| 6           | FILT  | Inverting terminal of CSA Buffer. Connect a series RC Filter of 4 k $\Omega$ and 0.47 $\mu$ F, otherwise leave open. |
| 7           | RS+   | External Sense Resistor Power-Side Connection.                                                                       |
| 8           | RS-   | External Sense Resistor Load-Side Connection.                                                                        |
| Exposed Pad | EPAD  | Exposed backside paddle. For best electrical and thermal performance, solder to analog ground.                       |

## 6. Packaging

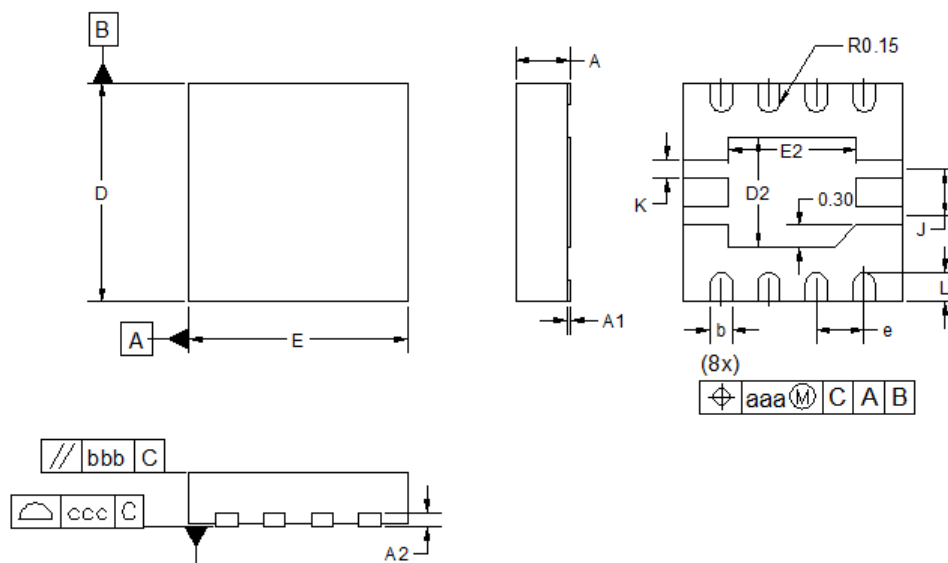


Figure 6.1. TS1109 3x3 mm 8-TDFN Package Diagram

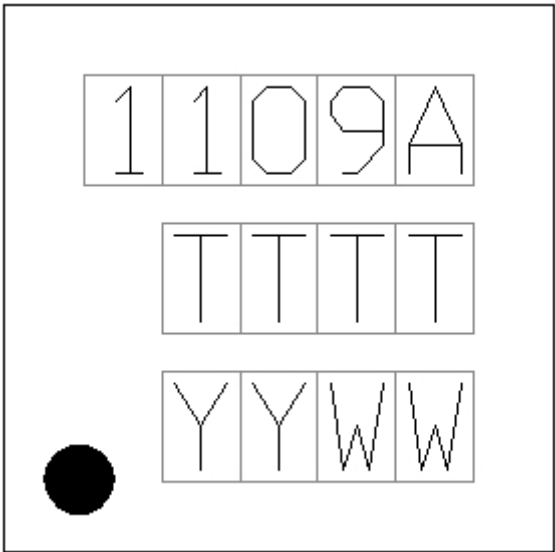
Table 6.1. Package Dimensions

| Dimension | Min      | Nom  | Max  |
|-----------|----------|------|------|
| A         | 0.70     | 0.75 | 0.80 |
| A1        | 0.00     | 0.02 | 0.05 |
| A2        | 0.20 REF |      |      |
| b         | 0.25     | 0.30 | 0.35 |
| D         | 3.00 BSC |      |      |
| D2        | 1.49     | 1.50 | 1.51 |
| e         | 0.65 BSC |      |      |
| E         | 3.00 BSC |      |      |
| E2        | 1.65     | 1.75 | 1.85 |
| L         | 0.30     | 0.40 | 0.50 |
| K         | 0.20     | 0.25 | 0.30 |
| J         | 0.65 REF |      |      |
| aaa       | 0.10     |      |      |
| bbb       | 0.05     |      |      |
| ccc       | 0.05     |      |      |

**Note:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. This drawing conforms to the JEDEC Solid State Outline MO-229.

## 7. Top Marking

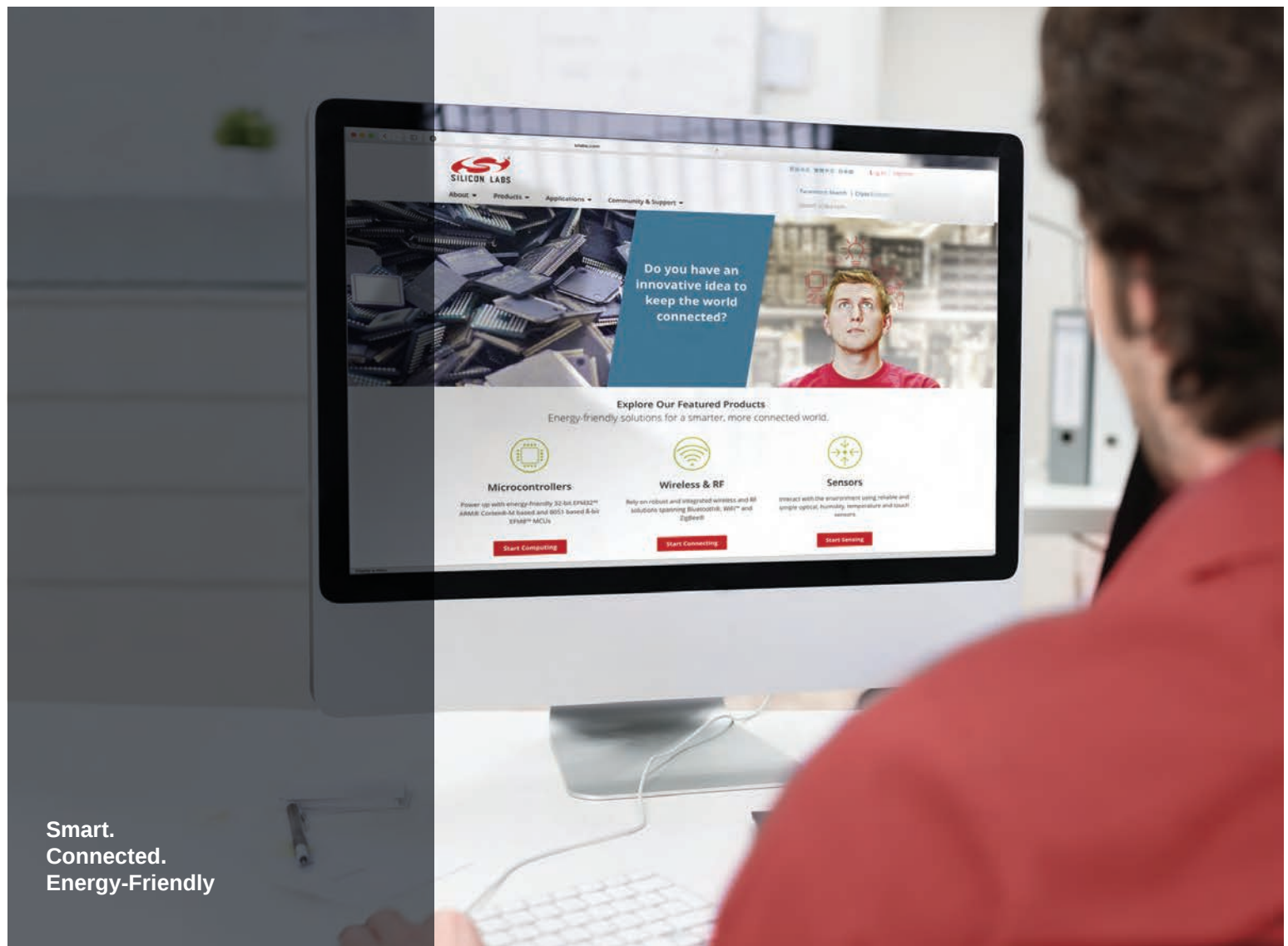


**Figure 7.1. Top Marking**

**Table 7.1. Top Marking Explanation**

| Mark Method         | Laser                                         |                                 |
|---------------------|-----------------------------------------------|---------------------------------|
| Pin 1 Mark:         | Circle = 0.50 mm Diameter (lower left corner) |                                 |
| Font Size:          | 0.50 mm (20 mils)                             |                                 |
| Line 1 Mark Format: | Product ID                                    | Note: A = 20 gain, B = 200 gain |
| Line 2 Mark Format: | TTTT – Mfg Code                               | Manufacturing code              |
| Line 3 Mark Format: | YY = Year; WW = Work Week                     | Year and week of assembly       |

|                                                                        |           |
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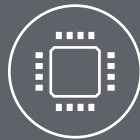


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