

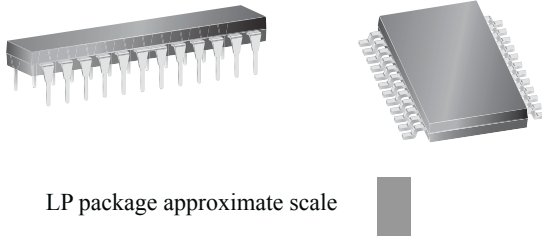
DMOS Dual Full-Bridge Microstepping PWM Motor Driver

Features and Benefits

- ± 1.5 A, 50 V continuous output rating
- Low $R_{DS(on)}$ DMOS output drivers
- Short-to-ground protection
- Shorted load protection
- Optimized microstepping via six bit linear DACs
- Programmable mixed, fast, and slow current decay modes
- 4 MHz internal oscillator for digital timing
- Serial interface controls chip functions
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection
- Inputs compatible with 5 or 3.3 V control signals
- Sleep and Idle modes

Packages

24 pin batwing DIP (suffix B) and 24 pin TSSOP with exposed thermal pad (suffix LP)



LP package approximate scale

Description

Designed for pulse width modulated (PWM) current control of bipolar microstepped stepper motors, the A3992 is capable of continuous output currents to ± 1.5 A and operating voltages to 50 V. Internal fixed off-time PWM current control timing circuitry can be programmed via the serial interface to operate in slow, fast, or mixed decay modes.

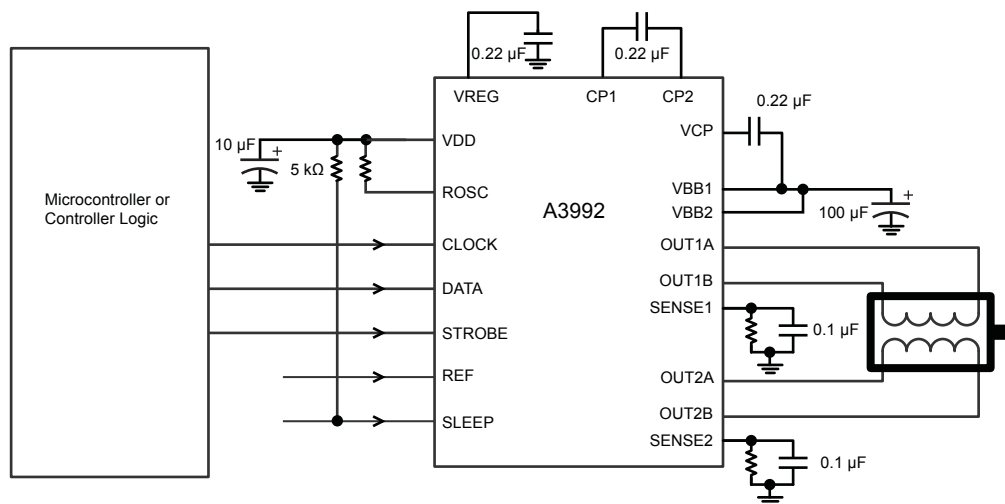
The desired load current level is set via the serial port with two six bit linear DACs in conjunction with a reference voltage. The six bits of control allow maximum flexibility in torque control for a variety of step methods, from microstepping to full step drive. Load current is set in 1.56% increments of the maximum value.

Synchronous rectification circuitry allows the load current to flow through the low $R_{DS(on)}$ of the DMOS output driver during current decay. This feature eliminates the need for external clamp diodes in most applications, saving cost and external component count, while minimizing power dissipation.

Internal circuit protection includes short-to-ground, shorted load, thermal shutdown with hysteresis, and crossover current protection. Special power up sequencing is not required.

The A3992 is supplied in a thin profile (1.2 mm maximum height) 24 pin TSSOP (suffix LP) with exposed thermal pad and a 24 pin plastic DIP with dual copper batwing tabs (suffix B). The exposed thermal pad on the LP is at ground potential and needs no electrical isolation. Both packages are lead (Pb) free with 100% matte tin leadframe plating.

Typical Application



Selection Guide

| Part Number | Packing | Package |
|--------------|------------------------|---------------------------------------|
| A3992SB-T | 15 pieces/tube | 24 pin batwing DIP |
| A3992SLPTR-T | Tape, 4000 pieces/reel | 24 pin TSSOP with exposed thermal pad |

Absolute Maximum Ratings

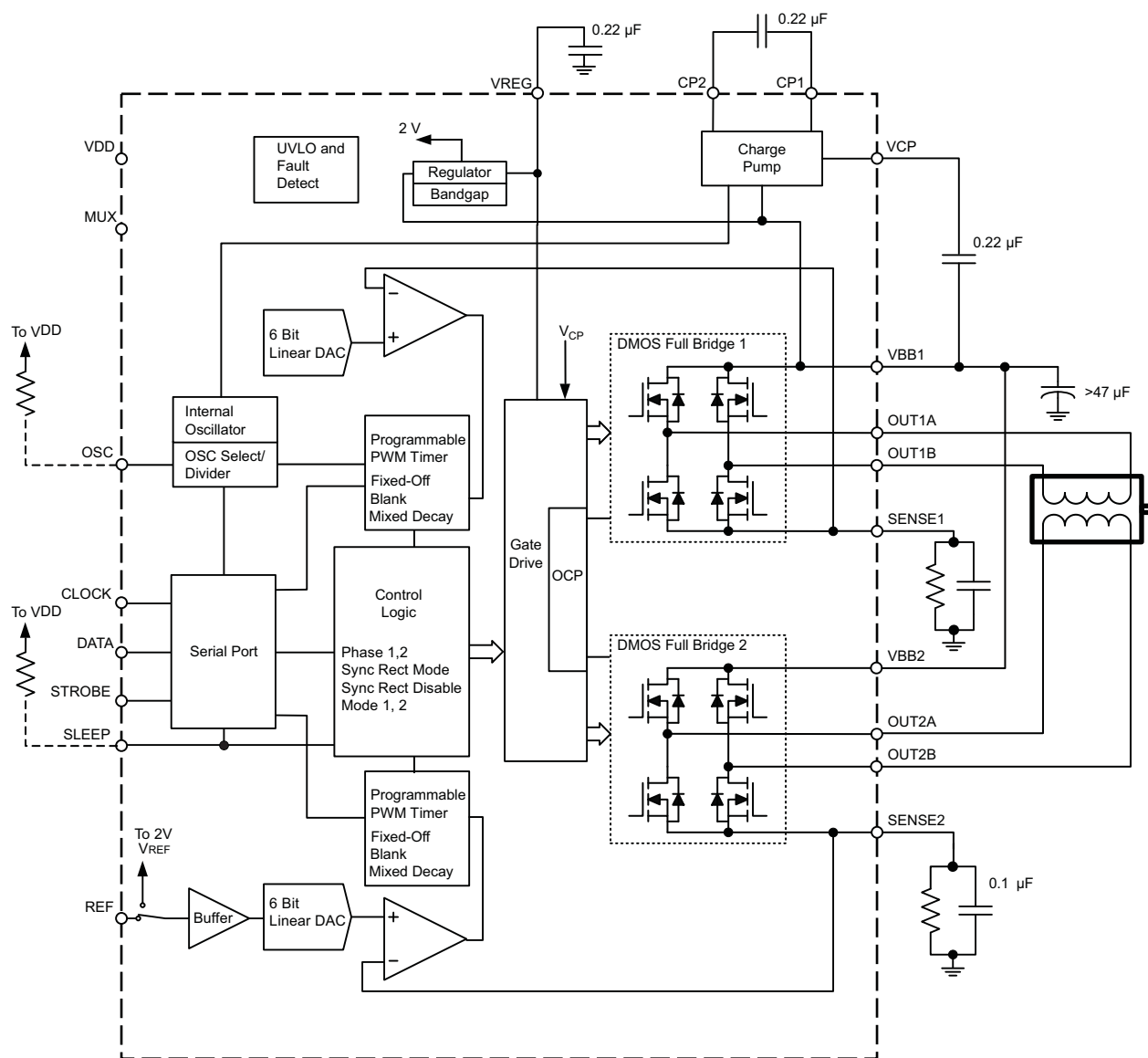
| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|--------------|--|------------|-------|
| Load Supply Voltage | V_{BB} | | 50 | V |
| Output Current | I_{OUT} | Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C. | ±1.5 | A |
| Logic Supply Voltage | V_{DD} | | 7.0 | V |
| Logic Input Voltage Range | V_{IN} | | −0.3 to 7 | V |
| VBBx to OUTx Voltage | | | 50 | V |
| OUTx to SENSEx Voltage | | | 50 | V |
| REF Reference Voltage | V_{REF} | | 3 | V |
| SENSE Voltage (DC) | V_{SENSE} | | 500 | mV |
| Operating Ambient Temperature | T_A | Range S | −20 to 85 | °C |
| Maximum Junction Temperature | $T_{J(max)}$ | | 150 | °C |
| Storage Temperature | T_{stg} | | −55 to 150 | °C |

Thermal Characteristics*

| Characteristic | Symbol | Notes | Rating | Units |
|----------------------------|-----------------|--|--------|-------|
| Package Thermal Resistance | $R_{\theta JA}$ | B package on 4-layer PCB | 26 | °C/W |
| | | B package on 2-layer PCB with 3.15 in. ² 2 oz. copper each side | 36 | °C/W |
| | | LP package on 4-layer PCB | 28 | °C/W |
| | | LP package on 2-layer PCB with 3.8 in. ² 2 oz. copper each side | 32 | °C/W |

*Additional thermal data available on the Allegro website.

Functional Block Diagram



ELECTRICAL CHARACTERISTICS¹ valid at $T_A = 25^\circ\text{C}$, $V_{BB} = 50\text{ V}$, $f_{\text{PWM}} < 50\text{ kHz}$, unless otherwise noted

| Characteristic | Symbol | Test Conditions | Min. | Typ. ² | Max. | Units |
|---|--------------------------------------|---|-------|-------------------|-------|-------|
| Output Drivers | | | | | | |
| Load Supply Voltage Range | V _{BB} | Operating, I _{OUT} = ±1.5 A | 15 | – | 50 | V |
| | | During Sleep mode | 0 | – | 50 | V |
| Output Leakage Current | I _{DSS} | V _{OUT} = V _{BB} | – | <1.0 | 50 | µA |
| | | V _{OUT} = 0 V | – | <–1.0 | –50 | µA |
| Output On Resistance | R _{DS(on)} | Source driver, I _{OUT} = -1.5 A | – | 0.54 | 0.6 | Ω |
| | | Sink driver, I _{OUT} = 1.5 A | – | 0.54 | 0.6 | Ω |
| Body Diode Forward Voltage | V _F | Source diode, I _F = -1.5 A | – | – | 1.2 | V |
| | | Sink diode, I _F = 1.5 A | – | – | 1.2 | V |
| Motor Supply Current | I _{BB} | f _{PWM} < 50 kHz | – | – | 8 | mA |
| | | Operating, outputs disabled | – | – | 6 | mA |
| | | Sleep or Idle mode | – | – | 20 | µA |
| Logic Supply Current | I _{DD} | f _{PWM} < 50 kHz | – | – | 12 | mA |
| | | Outputs off | – | – | 10 | mA |
| | | Idle mode (Word 1, D18 = 0) | – | – | 1.5 | mA |
| | | Sleep mode | – | – | 100 | µA |
| Control Logic | | | | | | |
| Logic Supply Voltage Range | V _{DD} | Operating | 4.5 | 5 | 5.5 | V |
| Logic Input Voltage | V _{IN(1)} | | 2.0 | – | – | V |
| | V _{IN(0)} | | – | – | 0.8 | V |
| Logic Input Current | I _{IN(1)} | V _{IN} = 2.0 V | – | <1.0 | 20 | µA |
| | I _{IN(0)} | V _{IN} = 0.8 V | – | <–2.0 | –20 | µA |
| Input Hysteresis | | | 0.20 | – | 0.40 | V |
| Minimum sleep pulse width | t _S | | > 2 | – | – | µs |
| OSC input frequency | f _{OSC(in)} | Divide by 1 (Word 2, D13=0, D14=1) | 2.5 | – | 6 | MHz |
| OSC input duty cycle | | | 40 | – | 60 | % |
| Internal Oscillator | f _{OSC} | OSC shorted to GND | 3 | 4 | 5 | MHz |
| | | R _{OSC} = 51 kΩ | 3.4 | 4 | 4.6 | MHz |
| DAC Accuracy | V _{DAC} | Measured relative to REF buffer output | – | ±0.5 | – | LSB |
| Reference Input Voltage Range | | | .5 | – | 2.6 | V |
| Reference Buffer Offset | V _{OS} | | – | ±10 | – | mV |
| Reference Divider Ratio | V _{REF} /V _{SENSE} | Word 0, D18 = 0, D17 = 1, V _{REF} = 0.5 to 2.6 V | 7.4 | 8 | 8.8 | – |
| | | Word 0, D18 = 1, D17 = 1, V _{REF} =0.5 to 2.6 V | 3.6 | 4 | 4.4 | – |
| Reference Input Current | I _{REF} | V _{REF} = 2.0 V | –0.5 | – | 0.5 | µA |
| Internal Reference Voltage | V _{REFINT} | | 1.940 | 2.0 | 2.060 | V |
| Comparator Input Offset Volt. | V _{IO} | V _{REF} = 0 V | –5 | 0 | 5 | mV |
| G _M Error ³ | V _{ERR} | Internal V _{REF} , Range = 8, DAC = 63 | –6 | 0 | 6 | % |
| | | Internal V _{REF} , Range = 8, DAC = 31 | –9 | 0 | 9 | % |
| | | Internal V _{REF} , Range = 4, DAC = 63 | –6 | 0 | 6 | % |
| | | Internal V _{REF} , Range = 4, DAC = 15 | –10 | 0 | 10 | % |
| Propagation Delay Times | t _{pd} | 50% to 90%; PWM change to source on | 500 | 800 | 1000 | ns |
| | | 50% to 90%; PWM change to source off | 35 | – | 250 | ns |
| | | 50% to 90%; PWM change to sink on | 500 | 800 | 1000 | ns |
| | | 50% to 90%; PWM change to sink off | 35 | – | 250 | ns |
| Crossover Dead Time | t _{DT} | | 300 | 650 | 900 | ns |
| UVLO Enable Threshold | V _{UVLO} | V _{DD} rising | 3.9 | 4.2 | 4.45 | V |
| UVLO Hysteresis | V _{UVLOHYS} | | 0.05 | 0.10 | – | V |
| Protection Circuitry | | | | | | |
| Overcurrent Protection Threshold ⁴ | I _{OCPST} | | 2 | – | – | A |
| Overcurrent Blanking | t _{OCP} | | 1 | – | 3 | µs |
| Thermal Shutdown Temperature | T _J | | – | 165 | – | °C |
| Thermal Shutdown Hysteresis | T _{JHYS} | | – | 15 | – | °C |

¹Negative current is defined as coming out of (sourcing) the specified device pin.

²Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

³ $V_{\text{ERR}} = [(V_{\text{REF}}/\text{Range}) - V_{\text{SENSE}}]/(V_{\text{REF}}/\text{Range})$.

⁴OCP is tested at $T_A = 25^\circ\text{C}$ in a restricted range and guaranteed by characterization.



Serial Interface Description

The A3992 is controlled via a 3 wire serial port. The programmable functions allow maximum flexibility in configuring the PWM to the motor drive requirements. The serial data is written as two 19 bit words, 1 bit to select which word (referred to here as *Word 0* and *Word 1*) and 18 bits of data. The serial port is defined in the following tables and text descriptions.

Word 0 Bit Assignments

Word 0 is selected by setting D0 = 0. Assignments are summarized in the following table, and described in detail in the remainder of this section.

| Word 0 Bit Assignments | |
|------------------------|----------------------|
| Bit | Function |
| D0 | Word Select = 0 |
| D1 | Bridge 1, DAC, LSB |
| D2 | Bridge 1, DAC, Bit2 |
| D3 | Bridge 1, DAC, Bit3 |
| D4 | Bridge 1, DAC, Bit4 |
| D5 | Bridge 1, DAC, Bit 5 |
| D6 | Bridge 1, DAC, MSB |
| D7 | Bridge 2, DAC, LSB |
| D8 | Bridge 2, DAC, Bit2 |
| D9 | Bridge 2, DAC, Bit3 |
| D10 | Bridge 2, DAC, Bit4 |
| D11 | Bridge 2, DAC, Bit 5 |
| D12 | Bridge 2, DAC, MSB |
| D13 | Bridge 1 Phase |
| D14 | Bridge 2 Phase |
| D15 | Bridge 1 Mode |
| D16 | Bridge 2 Mode |
| D17 | Reference Select |
| D18 | Range Select |

D1 – D6 Bridge 1, Linear DAC. 6 bit word to set desired current level for bridge 1. Setting all bits to zero disables Full Bridge 1, all drivers off. (See Current Regulation in the Functional Description section.)

D7 – 12 Bridge 2 Linear DAC. 6 bit word to set the desired current level for bridge 2. Setting all bits to zero disables Full Bridge 2, all drivers off. (See Current Regulation in the Functional Description section.)

D13 Bridge 1 Phase. This bit controls the direction of current for motor phase 1 as defined below:

| D13 | OUT1A | OUT1B |
|-----|-------|-------|
| 0 | L | H |
| 1 | H | L |

D14 Bridge 2 Phase. This bit controls the direction of current for motor phase 2 as defined below:

| D14 | OUT2A | OUT2B |
|-----|-------|-------|
| 0 | L | H |
| 1 | H | L |

D15 Bridge 1 Mode. This bit determines the decay for Full Bridge 1 as defined below:

| D15 | Mode |
|-----|-------------|
| 0 | Mixed Decay |
| 1 | Slow Decay |

D16 Bridge 2 Mode. This bit determines the decay for Full Bridge 2 as defined below:

| D16 | Mode |
|-----|-------------|
| 0 | Mixed Decay |
| 1 | Slow Decay |

D17 Ref Select. This bit determines the reference input for the two 6 bit linear DACs. Logic low selects internal 2 V reference voltage, logic high selects external reference input on the REF pin.

D18 G_m Range Select. D18 determines if the scaling factor used is 4 or 8:

| D18 | Divider | Load Current |
|-----|---------|---|
| 0 | ÷ 8 | $I_{TRIP} = V_{DAC}/(R_{SENSE} \times 8)$ |
| 1 | ÷ 4 | $I_{TRIP} = V_{DAC}/(R_{SENSE} \times 4)$ |

Word 1 Bit Assignments

Word 1 is selected by setting D0 = 1. Assignments are summarized in the following table, and described in detail in the remainder of this section.

| Word 1 Bit Assignments | |
|------------------------|-----------------------|
| Bit | Function |
| D0 | Word Select = 1 |
| D1 | Blank Time LSB |
| D2 | Blank Time MSB |
| D3 | Off Time LSB |
| D4 | Off Time Bit1 |
| D5 | Off Time Bit2 |
| D6 | Off Time Bit3 |
| D7 | Off Time MSB |
| D8 | Fast Decay Time LSB |
| D9 | Fast Decay Time Bit1 |
| D10 | Fast Decay Time Bit2 |
| D11 | Fast Decay Time MSB |
| D12 | C0 Oscillator Control |
| D13 | C1 Oscillator Control |
| D14 | SR Control Bit 1 |
| D15 | SR Control Bit 2 |
| D16 | Reserved for testing |
| D17 | Reserved for testing |
| D18 | Idle Mode |

D1 – D2 Blank Time. 2 bits to set the blank time scaling factor for the current sense comparator:

| D2 | D1 | Time |
|----|----|---------------------|
| 0 | 0 | $4 \times P_{OSC}$ |
| 0 | 1 | $6 \times P_{OSC}$ |
| 1 | 0 | $8 \times P_{OSC}$ |
| 1 | 1 | $12 \times P_{OSC}$ |

When a source driver turns on, a current spike occurs due to the reverse recovery currents of the clamp diodes and/or switching transients related to distributed capacitance in the load. To prevent this current spike

from erroneously resetting the source enable latch, the sense comparator is blanked. The blank timer runs after the off time counter to provide the programmable blanking function. The blank timer is reset when PHASE is changed.

D3 – D7 Fixed Off Time. 5 bits to set the fixed off-time for the internal PWM control circuitry. Fixed off-time is defined by:

$$t_{OFF} = (1 + n) \times P_{OSC} \times 8 - P_{OSC} ,$$

where $n = 0$ to 31.

For example, with a master oscillator frequency of 4 MHz ($P_{OSC} = 250$ ns), the fixed off-time is adjustable from 1.75 to 63.75 μ s, in increments of 2 μ s.

D8 – D11 Fast Decay Time. 4 bits to set the fast decay portion of fixed off-time for the internal PWM control circuitry. The fast decay portion is defined by:

$$t_{fd} = (1 + n) \times P_{OSC} \times 8 - P_{OSC} ,$$

where $n = 0$ to 15.

For example, with a master oscillator frequency of 4 MHz ($P_{OSC} = 250$ ns), the fixed off-time is adjustable from 1.75 to 31.75 μ s, in increments of 2 μ s. For $t_{fd} > t_{off}$, the device will effectively operate in fast decay mode.

D12 – D13 Oscillator Control. 2 bits to set timing options:

| D13 | D12 | Source and Rate |
|-----|-----|---------------------------|
| 0 | 0 | Internal clock 4 MHz |
| 0 | 1 | External clock $f \div 1$ |
| 1 | 0 | External clock $f \div 2$ |
| 1 | 1 | External clock $f \div 4$ |

A 4 MHz internal oscillator can be used for the timing functions. If more precise control is required, an external oscillator can be input to OSC pin. To accommodate a wider range of system clocks, an internal divider is provided to generate the desired MO frequency.

D14 – D15 Synchronous Rectification. 2 bits set the different modes of operation (see Synchronous Rectification in the Functional Description section):

| D15 | D14 | Synchronous Rectifier |
|-----|-----|-----------------------|
| 0 | 0 | Active |
| 0 | 1 | Disabled |
| 1 | 0 | Passive |
| 1 | 1 | Allegro defined use |

D16, D17 (Reserved). 2 bits reserved for testing.

They should be programmed to 0 during normal operation.

D18 Idle Mode. The device can be put into the low-power Idle mode by writing a 0 to D18. The outputs are disabled, the charge pump turned off, and the device consumes a lower supply current. The undervoltage monitor circuit remains active.

Functional Description

VREG. The VREG pin should be decoupled with a 0.22 μ F capacitor to ground. This internally generated supply voltage is used to run the sink side DMOS outputs. VREG is internally monitored and in the case of a fault condition, the outputs of the device are disabled.

Current Regulation. The reference voltage can be set by analog input to the REF terminal, or via the internal 2 V precision reference. The choice of reference voltage and selection of sense resistor set maximum trip current, as follows:

$$I_{TRIPMAX} = V_{REF} / (\text{Range} \times R_{SENSE})$$

Microstepping current levels are set according to the following equations:

$$I_{TRIP} = V_{DAC} / (\text{Range} \times R_{SENSE}), \text{ and}$$

$$V_{DAC} = ((1 + \text{DAC}) \times V_{REF}) / 64,$$

where DAC is the input code, 1 to 63 (Word 0, D1 to D12), and Range is 4 or 8, as selected by Word 0, D18. Programming a DAC input code to 0 disables the corresponding bridge, and results in minimum load current.

PWM Timer Function. The PWM timer is programmable via the serial port to provide fixed off-time

PWM signals to the control block. In mixed decay mode, the first portion of the off-time operates in fast decay, until the fast decay time count is reached, followed by slow decay for the remainder of the fixed off-time. If the fast decay time is set longer than the off-time, the device effectively operates in fast decay mode.

Oscillator. The PWM timer is based on an oscillator input, typically 4 MHz. The A3992 can be configured to select either the 4 MHz internal oscillator or, if more precise accuracy is required, an external clock can be connected to the OSC terminal. If an external clock is used, 3 internal divider choices are selectable via the serial port to allow flexibility in choosing f_{OSC} based on available system clocks. If the internal oscillator option is used, the absolute accuracy is dependent on process variation of resistance and capacitance. A precision resistor can be connected from the OSC terminal to V_{DD} to further improve the tolerance. The frequency is calculated as:

$$f_{OSC} = 204 \times 10^9 / R_{OSC}$$

If the internal oscillator is used without the external resistor the OSC terminal should be connected to GND.

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than V_{BBx} to drive the source FET gates. A $0.22\ \mu\text{F}$ ceramic capacitor is required between CP1 and CP2 for pumping purposes. A $0.22\ \mu\text{F}$ ceramic capacitor is required between VCP and the VBB terminals to act as a reservoir to operate the high-side FETs.

Sleep Mode. Control input on the SLEEP pin is used to minimize power consumption when not the device is not in use. This disables much of the internal circuitry including the output DMOS, regulator, and charge pump. Logic low puts the device into Sleep mode, logic high allows normal operation and startup of the device into the home position. When asserted low, the serial port is reset. All bits are reset to 0s, with the exception of D7, the fixed off-time MSB, which is set to 1. This prevents the off-time from being too short, which could result in a loss of current control. When coming out of Sleep mode, allow 1 ms before issuing a step command, to allow the charge pump to stabilize.

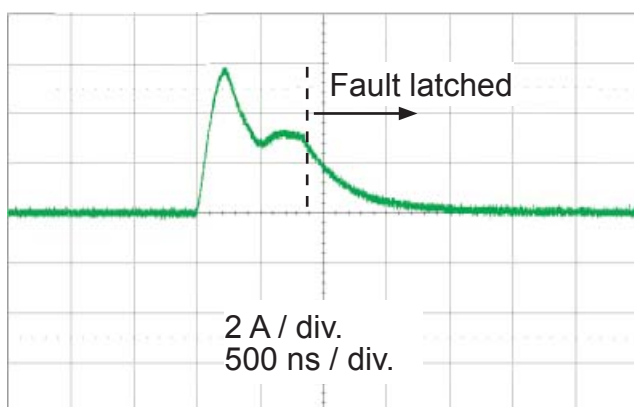
Shutdown. In the event of a fault due to excessive junction temperature, or to low voltage on V_{CP} or V_{REG} , the outputs of the device are disabled until the fault condition is removed. At power up, and in the event of low V_{DD} , the UVLO circuit disables the drivers and resets the data in the serial port.

Short to Ground. Should a motor winding short to ground, the current through the short will rise until the overcurrent (OCP) threshold is exceeded, a minimum of 2 A. The driver will turn off after a short propagation delay and latch the device. The device will remain latched until the SLEEP input goes high or VDD power is removed. As shown in panel A of the figure below, a short to ground will produce a single overcurrent event.

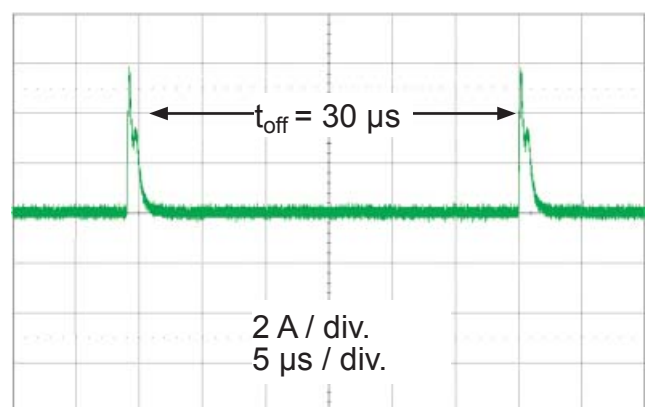
Shorted Load. During a shorted load event, the current path is through the sense resistor. The device will be protected, however, the device does not see this as a fault because the current path is not interrupted, so this condition will not latch the part.

When a bridge turns on, the current will rise and exceed the overcurrent threshold. After a blank time of approximately $1\ \mu\text{s}$, the driver will look at the voltage on the SENSE pin. The voltage on the SENSE pin will be larger than the voltage set by the VREF pin, and the bridge will turn off for the time set by the OSC pin. Panel B of the figure below shows a shorted load condition with an off-time of $30\ \mu\text{s}$.

MUX. The MUX pin is reserved for Allegro internal use and has no function to the end user. In the application, this pin can be tied to ground or left floating.



(A) Short-to-ground event



(B) Short-to-load event

Synchronous Rectification. When a PWM off-cycle is triggered, by a bridge disable command or internal fixed off-time cycle, load current recirculates according to the decay mode selected by control logic. The A3992 synchronous rectification feature turns on the appropriate MOSFETs during current decay, and effectively shorts out the body diodes with the low $R_{DS(on)}$ driver. This lowers power dissipation significantly, and can eliminate the need for external Schottky diodes for most applications.

Three distinct modes of operation can be configured

with the two serial port control bits:

1. *Active mode.* Prevents reversal of load current. Turns off synchronous rectification when a 0 current level is detected.
2. *Passive mode.* Allows reversal of current, but will turn off the synchronous rectifier circuit if the load current inversion ramps up to the current limit.
3. *Disabled.* Prevents MOSFET switching during load recirculation in fast decay portion of the off-time. During the slow decay portion of the off-time, the low-side switch turns on, which recirculates current through the low-side MOSFET and low-side body diode.

Applications Notes

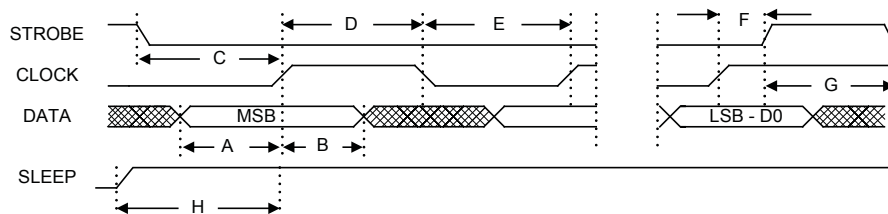
Current Sensing. To minimize inaccuracies in sensing the I_{PEAK} current level caused by ground trace $I \bullet R$ drops, the sense resistor should have an independent ground return to the GND terminal of the device. For low value sense resistors, the $I \bullet R$ drops in the PCB sense resistor traces can be significant and should be taken into account. The use of sockets should be avoided because they can introduce variation in R_{SENSE} due to their contact resistance.

Allegro MicroSystems recommends a value of R_{SENSE} given by:

$$R_{SENSE} = 0.5 / I_{TRIP MAX} \cdot$$

Thermal Protection. Circuitry turns off all drivers when the junction temperature reaches 165°C typical. It is intended only to protect the device from failures due to excessive junction temperatures, and should not imply that output short circuits are permitted. Thermal shutdown has a hysteresis of approximately 15°C.

Serial Port Write Timing Operation. Data is clocked into a shift register on the rising edge of a CLOCK signal. Normally, STROBE is held high, and is only brought low to initiate a write cycle. The data is written MSB first. Refer to the diagram below for timing requirements.



Serial Port Timing Diagram

| | | | |
|--|--------|--|------------|
| A. Minimum Data Setup Time | 15 ns | F. Minimum Setup Clock rising edge to Strobe | 50 ns |
| B. Minimum Data Hold Time | 10 ns | G. Minimum Strobe Pulse Width | 120 ns |
| C. Minimum Setup Strobe to Clock rising edge | 120 ns | H. Minimum Sleep to Clock Setup Time | 50 μ s |
| D. Minimum Clock High Pulse Width | 40 ns | I. Setup "Idle" Release to Output Enable | 1 ms |
| E. Minimum Clock Low Pulse Width | 40 ns | | |

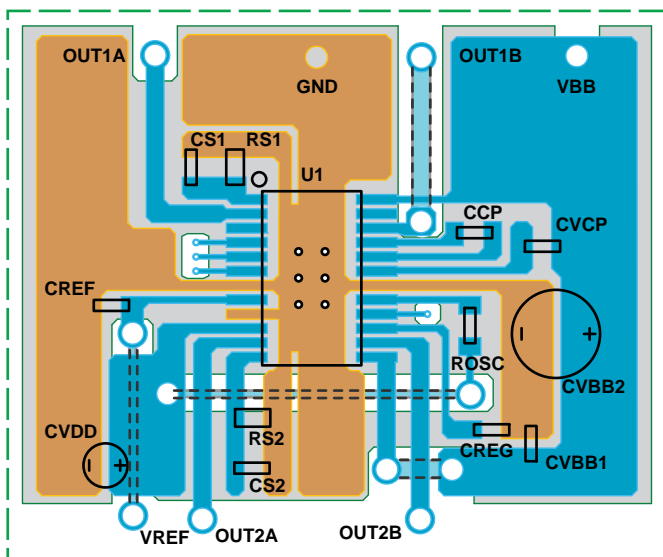
Layout. The printed circuit board should use a heavy groundplane. For optimum electrical and thermal performance, the A3992 must be soldered directly onto the board. On the underside of the A3992 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a star ground, located very close to the device. By making the connection between the pad and the ground plane directly under the A3992, that area becomes an ideal location for a star ground point. A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout, shown in the diagram below, illustrates how to create a star ground

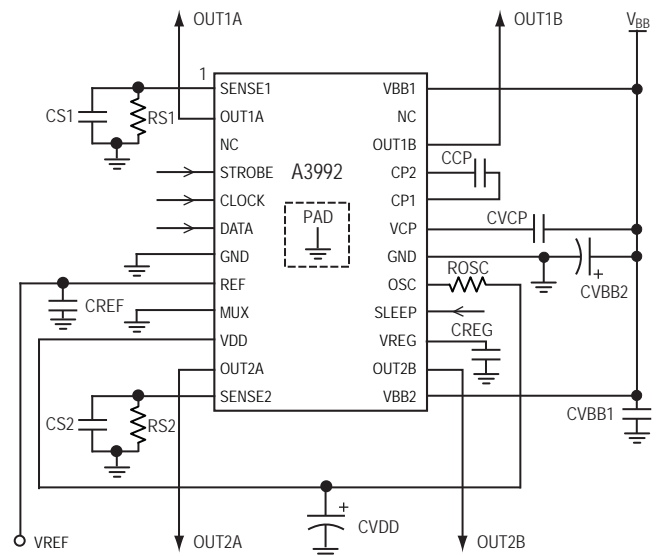
under the device, to serve both as a low impedance ground point and thermal path.

The two input capacitors should be placed in parallel, and as close to the device supply pins as possible. The ceramic capacitor (CVBB1) should be closer to the pins than the bulk capacitor (CVBB2). This is necessary because the ceramic capacitor will be responsible for delivering the high frequency current components.

The sense resistors, RSx, should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSEx pins have very short traces to the RSx resistors and very thick, low impedance traces directly to the star ground underneath the device.

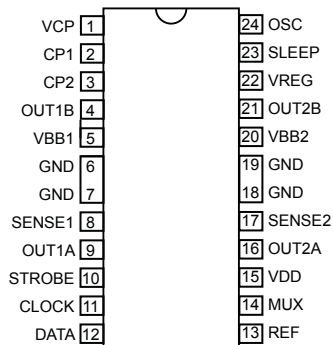


LP package layout shown

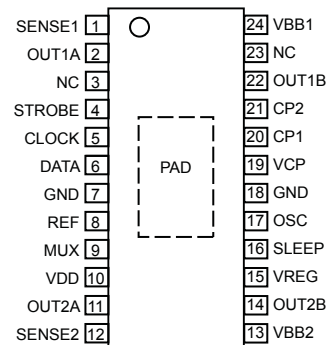


Device Pin-out Diagrams

B Package



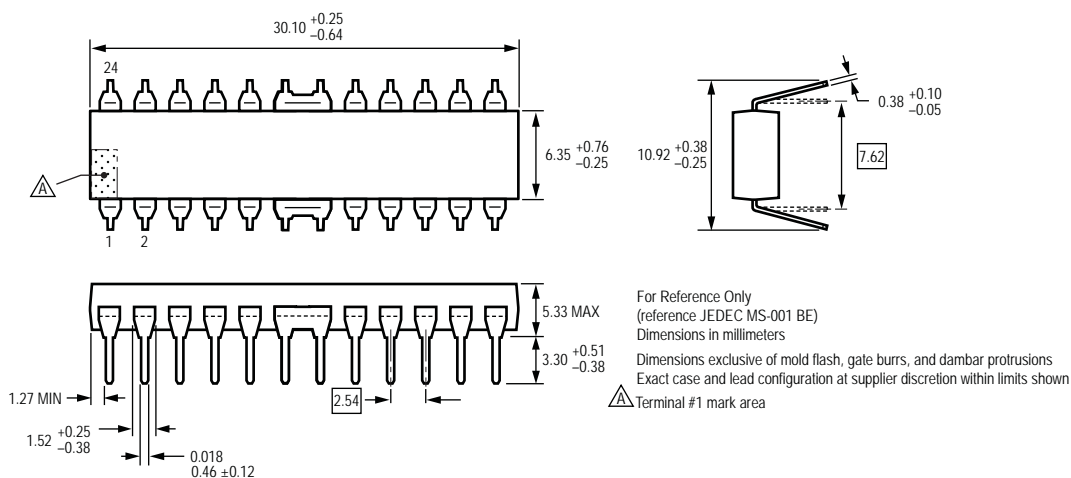
LP Package



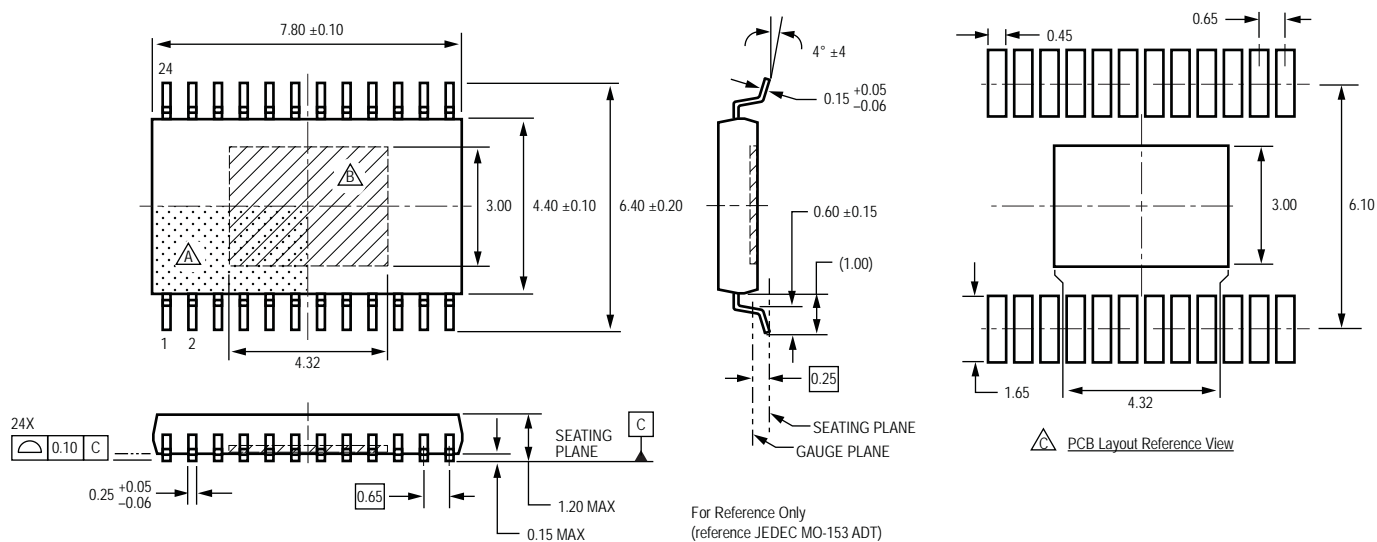
Terminal List Table

| Number | | Name | Pin Description |
|--------------|------------|--------|---|
| B Package | LP Package | | |
| 1 | 19 | VCP | Reservoir capacitor terminal |
| 2 | 20 | CP1 | Charge pump capacitor terminal |
| 3 | 21 | CP2 | Charge pump capacitor terminal |
| 4 | 22 | OUT1B | DMOS Full Bridge 1, output B |
| 5 | 24 | VBB1 | Load supply |
| 6, 7, 18, 19 | 7, 18 | GND | Ground. On B package, internally fused to the die pad for enhanced thermal dissipation. |
| 8 | 1 | SENSE1 | Sense resistor terminal for Full Bridge 1 |
| 9 | 2 | OUT1A | DMOS Full Bridge 1, output A |
| 10 | 4 | STROBE | Logic input |
| 11 | 5 | CLOCK | Logic input |
| 12 | 6 | DATA | Logic input |
| 13 | 8 | REF | G _m reference input |
| 14 | 9 | MUX | Not used |
| 15 | 10 | VDD | Logic supply |
| 16 | 11 | OUT2A | DMOS Full Bridge 2, output A |
| 17 | 12 | SENSE2 | Sense resistor terminal for Full Bridge 2 |
| 20 | 13 | VBB2 | Load supply |
| 21 | 14 | OUT2B | DMOS Full Bridge 2, output B |
| 22 | 15 | VREG | Internal regulator |
| 23 | 16 | SLEEP | Logic input |
| 24 | 17 | OSC | Oscillator input |
| – | 3, 23 | NC | No connection |
| – | – | PAD | Exposed thermal pad for enhanced thermal dissipation. |

Package B, 24 Pin DIP with Fused Pins



Package LP, 24 Pin TSSOP with Exposed Thermal Pad



For Reference Only
(reference JEDEC MO-153 ADT)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (bottom surface)
- △ Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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