

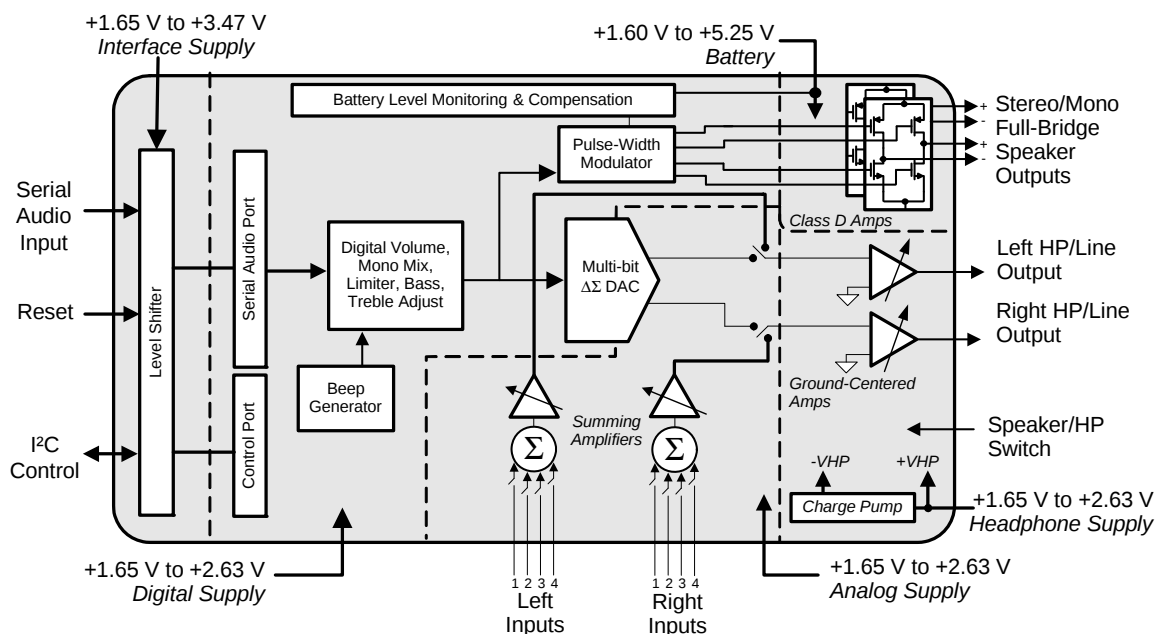
## Low Power, Stereo DAC w/Headphone & Speaker Amps

### FEATURES

- ◆ 98 dB Dynamic Range (A-wtd)
- ◆ 88 dB THD+N
- ◆ Headphone Amplifier - GND Centered
  - No DC-Blocking Capacitors Required
  - Integrated Negative Voltage Regulator
  - 2 x 23 mW into Stereo 16  $\Omega$  @ 1.8 V
  - 2 x 44 mW into Stereo 16  $\Omega$  @ 2.5V
- ◆ Stereo Analog Input Passthrough Architecture
  - Analog Input Mixing
  - Analog Passthrough with Volume Control
- ◆ Digital Signal Processing Engine
  - Bass & Treble Tone Control, De-Emphasis
  - PCM Input w/Independent Vol Control
  - Master Digital Volume Control and Limiter
  - Soft-Ramp & Zero-Cross Transitions
- ◆ Programmable Peak-Detect and Limiter
- ◆ Beep Generator w/Full Tone Control
  - Tone Selections Across Two Octaves
  - Separate Volume Control
  - Programmable On and Off Time Intervals
  - Continuous, Periodic, One-Shot Beep Selections

### Class D Stereo/Mono Speaker Amplifier

- ◆ No External Filter Required
- ◆ High Stereo Output Power at 10% THD+N
  - 2 x 1.00 W into 8  $\Omega$  @ 5.0 V
  - 2 x 550 mW into 8  $\Omega$  @ 3.7 V
  - 2 x 230 mW into 8  $\Omega$  @ 2.5 V
- ◆ High Mono Output Power at 10% THD+N
  - 1 x 1.90 W into 4  $\Omega$  @ 5.0 V
  - 1 x 1.00 W into 4  $\Omega$  @ 3.7 V
  - 1 x 350 mW into 4  $\Omega$  @ 2.5 V
- ◆ Direct Battery Powered Operation
  - Battery Level Monitoring & Compensation
- ◆ 81% Efficiency at 800 mW
- ◆ Phase-Aligned PWM Output Reduces Idle Channel Current
- ◆ Spread Spectrum Modulation
- ◆ Low Quiescent Current



## System Features

- ◆ 12, 24, and 27 MHz Master Clock Support in Addition to Typical Audio Clock Rates
- ◆ High Performance 24-bit Converters
  - Multi-bit Delta-Sigma Architecture
  - Very Low 64Fs Oversampling Clock Reduces Power Consumption
- ◆ Low Power Operation
  - Stereo Analog Passthrough: 10 mW @ 1.8 V
  - Stereo Playback: 14 mW @ 1.8 V
- ◆ Variable Power Supplies
  - 1.8 V to 2.5 V Digital & Analog
  - 1.6 V to 5 V Class D Amplifier
  - 1.8 V to 2.5 V Headphone Amplifier
  - 1.8 V to 3.3 V Interface Logic
- ◆ Power Down Management
  - DAC, Passthrough Amplifier, Headphone Amplifier, Speaker Amplifier
- ◆ Flexible Clocking Options
  - Master or Slave Operation
  - Quarter-Speed Mode - (i.e. allows 8 kHz Fs while maintaining a flat noise floor up to 16 kHz)
  - 4 kHz to 96 kHz Sample Rates
- ◆ I<sup>2</sup>C™ Control Port Operation
- ◆ Headphone/Speaker Detection Input
- ◆ Pop and Click Suppression
- ◆ Pin-Compatible w/CS42L52

## Applications

- ◆ PDA's
- ◆ Personal Media Players
- ◆ Portable Game Consoles

## General Description

The CS43L22 is a highly integrated, low power stereo DAC with headphone and Class D speaker amplifiers. The CS43L22 offers many features suitable for low power, portable system applications.

The **DAC output path** includes a digital signal processing engine with various fixed function controls. Tone Control provides bass and treble adjustment of four selectable corner frequencies. Digital Volume controls may be configured to change on soft ramp transitions while the analog controls can be configured to occur on every zero crossing. The DAC also includes de-emphasis, limiting functions and a BEEP generator delivering tones selectable across a range of two full octaves.

The **stereo headphone amplifier** is powered from a separate positive supply and the integrated **charge pump** provides a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates the need for external DC-blocking capacitors.

The **Class D stereo speaker amplifier** does not require an external filter and provides the high efficiency amplification required by power sensitive portable applications. The speaker amplifier may be powered directly from a battery while the internal DC supply monitoring and compensation provides a constant gain level as the battery's voltage decays.

The CS43L22 accommodates analog routing of the analog input signal directly to the headphone amplifier. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier directly.

In addition to its many features, the CS43L22 operates from a low voltage analog and digital core making it ideal for portable systems that require extremely low power consumption in a minimal amount of space.

The CS43L22 is available in a 40-pin QFN package in Commercial (-40 to +85 °C) grade. The CS43L22 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to ["Ordering Information" on page 66](#) for complete ordering information.

## TABLE OF CONTENTS

|                                                                     |           |
|---------------------------------------------------------------------|-----------|
| <b>1. PIN DESCRIPTIONS .....</b>                                    | <b>7</b>  |
| 1.1 I/O Pin Characteristics .....                                   | 8         |
| <b>2. TYPICAL CONNECTION DIAGRAM .....</b>                          | <b>9</b>  |
| <b>3. CHARACTERISTIC AND SPECIFICATIONS .....</b>                   | <b>10</b> |
| RECOMMENDED OPERATING CONDITIONS .....                              | 10        |
| ABSOLUTE MAXIMUM RATINGS .....                                      | 10        |
| ANALOG OUTPUT CHARACTERISTICS .....                                 | 11        |
| ANALOG PASSTHROUGH CHARACTERISTICS .....                            | 12        |
| PWM OUTPUT CHARACTERISTICS .....                                    | 13        |
| HEADPHONE OUTPUT POWER CHARACTERISTICS .....                        | 14        |
| LINE OUTPUT VOLTAGE LEVEL CHARACTERISTICS .....                     | 15        |
| COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE .....   | 15        |
| SWITCHING SPECIFICATIONS - SERIAL PORT .....                        | 16        |
| SWITCHING SPECIFICATIONS - I <sup>2</sup> C CONTROL PORT .....      | 17        |
| DC ELECTRICAL CHARACTERISTICS .....                                 | 18        |
| DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS .....            | 18        |
| POWER CONSUMPTION .....                                             | 19        |
| <b>4. APPLICATIONS .....</b>                                        | <b>20</b> |
| 4.1 Overview .....                                                  | 20        |
| 4.1.1 Basic Architecture .....                                      | 20        |
| 4.1.2 Line Inputs .....                                             | 20        |
| 4.1.3 Line & Headphone Outputs .....                                | 20        |
| 4.1.4 Speaker Driver Outputs .....                                  | 20        |
| 4.1.5 Fixed Function DSP Engine .....                               | 20        |
| 4.1.6 Beep Generator .....                                          | 20        |
| 4.1.7 Power Management .....                                        | 20        |
| 4.2 DSP Engine .....                                                | 21        |
| 4.2.1 Beep Generator .....                                          | 22        |
| 4.2.2 Limiter .....                                                 | 22        |
| 4.3 Analog Passthrough .....                                        | 24        |
| 4.4 Analog Outputs .....                                            | 25        |
| 4.5 PWM Outputs .....                                               | 26        |
| 4.5.1 Mono Speaker Output Configuration .....                       | 27        |
| 4.5.2 VP Battery Compensation .....                                 | 27        |
| 4.5.2.1 Maintaining a Desired Output Level .....                    | 27        |
| 4.6 Serial Port Clocking .....                                      | 29        |
| 4.7 Digital Interface Formats .....                                 | 30        |
| 4.7.1 DSP Mode .....                                                | 31        |
| 4.8 Initialization .....                                            | 31        |
| 4.9 Recommended Power-Up Sequence .....                             | 31        |
| 4.10 Recommended Power-Down Sequence .....                          | 31        |
| 4.11 Required Initialization Settings .....                         | 32        |
| <b>5. CONTROL PORT OPERATION .....</b>                              | <b>33</b> |
| 5.1 I <sup>2</sup> C Control .....                                  | 33        |
| 5.1.1 Memory Address Pointer (MAP) .....                            | 34        |
| 5.1.1.1 Map Increment (INCR) .....                                  | 34        |
| <b>6. REGISTER QUICK REFERENCE .....</b>                            | <b>35</b> |
| <b>7. REGISTER DESCRIPTION .....</b>                                | <b>37</b> |
| 7.1 Chip I.D. and Revision Register (Address 01h) (Read Only) ..... | 37        |
| 7.1.1 Chip I.D. (Read Only) .....                                   | 37        |
| 7.1.2 Chip Revision (Read Only) .....                               | 37        |
| 7.2 Power Control 1 (Address 02h) .....                             | 37        |

|                                                                                  |    |
|----------------------------------------------------------------------------------|----|
| 7.2.1 Power Down .....                                                           | 37 |
| 7.3 Power Control 2 (Address 04h) .....                                          | 38 |
| 7.3.1 Headphone Power Control .....                                              | 38 |
| 7.3.2 Speaker Power Control .....                                                | 38 |
| 7.4 Clocking Control (Address 05h) .....                                         | 38 |
| 7.4.1 Auto-Detect .....                                                          | 38 |
| 7.4.2 Speed Mode .....                                                           | 39 |
| 7.4.3 32kHz Sample Rate Group .....                                              | 39 |
| 7.4.4 27 MHz Video Clock .....                                                   | 39 |
| 7.4.5 Internal MCLK/LRCK Ratio .....                                             | 39 |
| 7.4.6 MCLK Divide By 2 .....                                                     | 40 |
| 7.5 Interface Control 1 (Address 06h) .....                                      | 40 |
| 7.5.1 Master/Slave Mode .....                                                    | 40 |
| 7.5.2 SCLK Polarity .....                                                        | 40 |
| 7.5.3 DSP Mode .....                                                             | 40 |
| 7.5.4 DAC Interface Format .....                                                 | 40 |
| 7.5.5 Audio Word Length .....                                                    | 41 |
| 7.6 Interface Control 2 (Address 07h) .....                                      | 41 |
| 7.6.1 SCLK equals MCLK .....                                                     | 41 |
| 7.6.2 Speaker/Headphone Switch Invert .....                                      | 41 |
| 7.7 Passthrough x Select: PassA (Address 08h), PassB (Address 09h) .....         | 42 |
| 7.7.1 Passthrough Input Channel Mapping .....                                    | 42 |
| 7.8 Analog ZC and SR Settings (Address 0Ah) .....                                | 42 |
| 7.8.1 Ch. x Analog Soft Ramp .....                                               | 42 |
| 7.8.2 Ch. x Analog Zero Cross .....                                              | 42 |
| 7.9 Passthrough Gang Control (Address 0Ch) .....                                 | 42 |
| 7.9.1 Passthrough Channel B=A gang Control .....                                 | 42 |
| 7.10 Playback Control 1 (Address 0Dh) .....                                      | 43 |
| 7.10.1 Headphone Analog Gain .....                                               | 43 |
| 7.10.2 Playback Volume Setting B=A .....                                         | 43 |
| 7.10.3 Invert PCM Signal Polarity .....                                          | 43 |
| 7.10.4 Master Playback Mute .....                                                | 43 |
| 7.11 Miscellaneous Controls (Address 0Eh) .....                                  | 44 |
| 7.11.1 Passthrough Analog .....                                                  | 44 |
| 7.11.2 Passthrough Mute .....                                                    | 44 |
| 7.11.3 Freeze Registers .....                                                    | 44 |
| 7.11.4 HP/Speaker De-Emphasis .....                                              | 44 |
| 7.11.5 Digital Soft Ramp .....                                                   | 44 |
| 7.11.6 Digital Zero Cross .....                                                  | 45 |
| 7.12 Playback Control 2 (Address 0Fh) .....                                      | 45 |
| 7.12.1 Headphone Mute .....                                                      | 45 |
| 7.12.2 Speaker Mute .....                                                        | 45 |
| 7.12.3 Speaker Volume Setting B=A .....                                          | 45 |
| 7.12.4 Speaker Channel Swap .....                                                | 45 |
| 7.12.5 Speaker MONO Control .....                                                | 46 |
| 7.12.6 Speaker Mute 50/50 Control .....                                          | 46 |
| 7.13 Passthrough x Volume: PASSAVOL (Address 14h) & PASSBVOL (Address 15h) ..... | 46 |
| 7.13.1 Passthrough x Volume .....                                                | 46 |
| 7.14 PCMX Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh) .....                  | 47 |
| 7.14.1 PCM Channel x Mute .....                                                  | 47 |
| 7.14.2 PCM Channel x Volume .....                                                | 47 |
| 7.15 Beep Frequency & On Time (Address 1Ch) .....                                | 47 |
| 7.15.1 Beep Frequency .....                                                      | 47 |
| 7.15.2 Beep On Time .....                                                        | 48 |

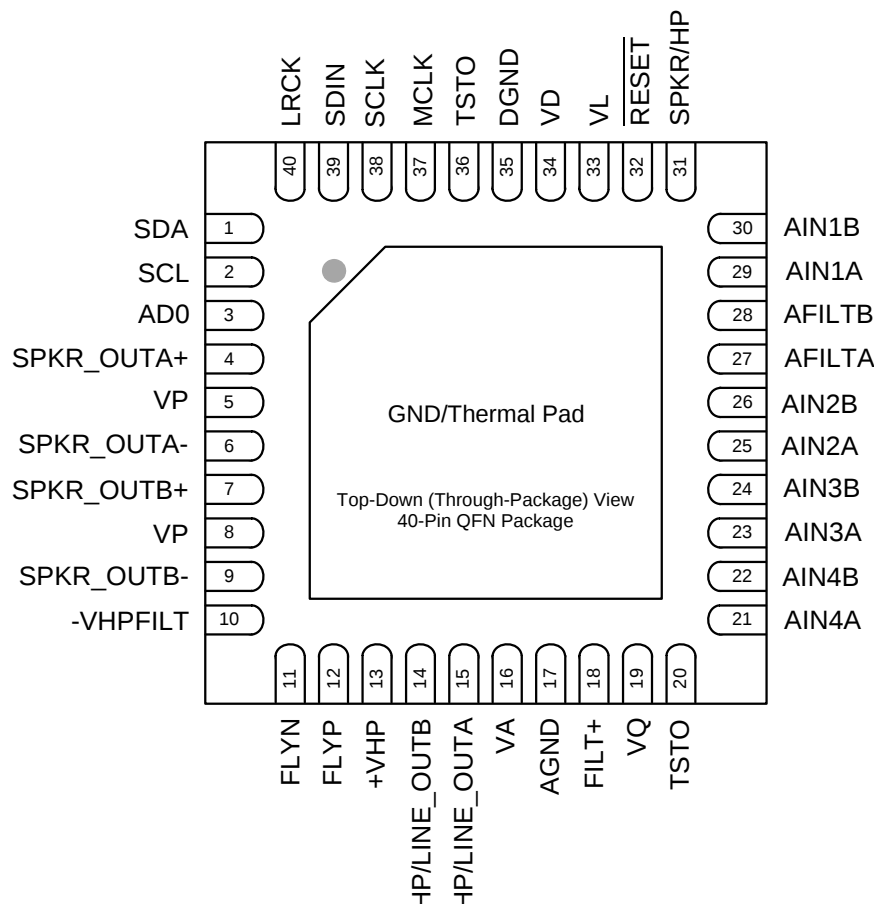
|                                                                            |           |
|----------------------------------------------------------------------------|-----------|
| 7.16 Beep Volume & Off Time (Address 1Dh) .....                            | 48        |
| 7.16.1 Beep Off Time .....                                                 | 48        |
| 7.16.2 Beep Volume .....                                                   | 49        |
| 7.17 Beep & Tone Configuration (Address 1Eh) .....                         | 49        |
| 7.17.1 Beep Configuration .....                                            | 49        |
| 7.17.2 Beep Mix Disable .....                                              | 49        |
| 7.17.3 Treble Corner Frequency .....                                       | 50        |
| 7.17.4 Bass Corner Frequency .....                                         | 50        |
| 7.17.5 Tone Control Enable .....                                           | 50        |
| 7.18 Tone Control (Address 1Fh) .....                                      | 50        |
| 7.18.1 Treble Gain .....                                                   | 50        |
| 7.18.2 Bass Gain .....                                                     | 51        |
| 7.19 Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h) .....  | 51        |
| 7.19.1 Master Volume Control .....                                         | 51        |
| 7.20 Headphone Volume Control: HPA (Address 22h) & HPB (Address 23h) ..... | 51        |
| 7.20.1 Headphone Volume Control .....                                      | 51        |
| 7.21 Speaker Volume Control: SPKA (Address 24h) & SPKB (Address 25h) ..... | 52        |
| 7.21.1 Speaker Volume Control .....                                        | 52        |
| 7.22 PCM Channel Swap (Address 26h) .....                                  | 52        |
| 7.22.1 PCM Channel Swap .....                                              | 52        |
| 7.23 Limiter Control 1, Min/Max Thresholds (Address 27h) .....             | 53        |
| 7.23.1 Limiter Maximum Threshold .....                                     | 53        |
| 7.23.2 Limiter Cushion Threshold .....                                     | 53        |
| 7.23.3 Limiter Soft Ramp Disable .....                                     | 53        |
| 7.23.4 Limiter Zero Cross Disable .....                                    | 54        |
| 7.24 Limiter Control 2, Release Rate (Address 28h) .....                   | 54        |
| 7.24.1 Peak Detect and Limiter .....                                       | 54        |
| 7.24.2 Peak Signal Limit All Channels .....                                | 54        |
| 7.24.3 Limiter Release Rate .....                                          | 54        |
| 7.25 Limiter Attack Rate (Address 29h) .....                               | 55        |
| 7.25.1 Limiter Attack Rate .....                                           | 55        |
| 7.26 Status (Address 2Eh) (Read Only) .....                                | 55        |
| 7.26.1 Serial Port Clock Error (Read Only) .....                           | 55        |
| 7.26.2 DSP Engine Overflow (Read Only) .....                               | 55        |
| 7.26.3 PCMx Overflow (Read Only) .....                                     | 56        |
| 7.27 Battery Compensation (Address 2Fh) .....                              | 56        |
| 7.27.1 Battery Compensation .....                                          | 56        |
| 7.27.2 VP Monitor .....                                                    | 56        |
| 7.27.3 VP Reference .....                                                  | 57        |
| 7.28 VP Battery Level (Address 30h) (Read Only) .....                      | 57        |
| 7.28.1 VP Voltage Level (Read Only) .....                                  | 57        |
| 7.29 Speaker Status (Address 31h) (Read Only) .....                        | 57        |
| 7.29.1 Speaker Current Load Status (Read Only) .....                       | 57        |
| 7.29.2 SPKR/HP Pin Status (Read Only) .....                                | 58        |
| 7.30 Charge Pump Frequency (Address 34h) .....                             | 58        |
| 7.30.1 Charge Pump Frequency .....                                         | 58        |
| <b>8. ANALOG PERFORMANCE PLOTS .....</b>                                   | <b>59</b> |
| 8.1 Headphone THD+N versus Output Power Plots .....                        | 59        |
| <b>9. EXAMPLE SYSTEM CLOCK FREQUENCIES .....</b>                           | <b>61</b> |
| 9.1 Auto Detect Enabled .....                                              | 61        |
| 9.2 Auto Detect Disabled .....                                             | 61        |
| <b>10. PCB LAYOUT CONSIDERATIONS .....</b>                                 | <b>62</b> |
| 10.1 Power Supply, Grounding .....                                         | 62        |
| 10.2 QFN Thermal Pad .....                                                 | 62        |

|                                        |           |
|----------------------------------------|-----------|
| <b>11. DIGITAL FILTER PLOTS .....</b>  | <b>63</b> |
| <b>12. PARAMETER DEFINITIONS .....</b> | <b>64</b> |
| <b>13. PACKAGE DIMENSIONS .....</b>    | <b>65</b> |
| THERMAL CHARACTERISTICS .....          | 65        |
| <b>14. ORDERING INFORMATION .....</b>  | <b>66</b> |
| <b>15. REFERENCES .....</b>            | <b>66</b> |
| <b>16. REVISION HISTORY .....</b>      | <b>66</b> |

## LIST OF FIGURES

|                                                                                 |    |
|---------------------------------------------------------------------------------|----|
| Figure 1. Typical Connection Diagram .....                                      | 9  |
| Figure 2. Headphone Output Test Load .....                                      | 14 |
| Figure 3. Serial Audio Interface Timing .....                                   | 16 |
| Figure 4. Control Port Timing - I <sup>2</sup> C .....                          | 17 |
| Figure 5. DSP Engine Signal Flow .....                                          | 21 |
| Figure 6. Beep Configuration Options .....                                      | 22 |
| Figure 7. Peak Detect & Limiter .....                                           | 23 |
| Figure 8. Analog Passthrough Signal Flow .....                                  | 24 |
| Figure 9. Analog Outputs .....                                                  | 25 |
| Figure 10. PWM Output Stage .....                                               | 26 |
| Figure 11. Battery Compensation .....                                           | 28 |
| Figure 12. I <sup>2</sup> S Format .....                                        | 30 |
| Figure 13. Left-Justified Format .....                                          | 30 |
| Figure 14. Right-Justified Format\ .....                                        | 30 |
| Figure 15. DSP Mode Format) .....                                               | 31 |
| Figure 16. Control Port Timing, I <sup>2</sup> C Write .....                    | 33 |
| Figure 17. Control Port Timing, I <sup>2</sup> C Read .....                     | 33 |
| Figure 18. THD+N vs. Output Power per Channel at 1.8 V (16 $\Omega$ load) ..... | 59 |
| Figure 19. THD+N vs. Output Power per Channel at 2.5 V (16 $\Omega$ load) ..... | 59 |
| Figure 20. THD+N vs. Output Power per Channel at 1.8 V (32 $\Omega$ load) ..... | 60 |
| Figure 21. THD+N vs. Output Power per Channel at 2.5 V (32 $\Omega$ load) ..... | 60 |
| Figure 22. Passband Ripple .....                                                | 63 |
| Figure 23. Stopband .....                                                       | 63 |
| Figure 24. DAC Transition Band .....                                            | 63 |
| Figure 25. Transition Band (Detail) .....                                       | 63 |

## 1. PIN DESCRIPTIONS



| Pin Name        | #      | Pin Description                                                                                                                                                                   |
|-----------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SDA             | 1      | <b>Serial Control Data</b> ( <i>Input/Output</i> ) - SDA is a data I/O in I <sup>2</sup> C Mode.                                                                                  |
| SCL             | 2      | <b>Serial Control Port Clock</b> ( <i>Input</i> ) - Serial clock for the serial control port.                                                                                     |
| AD0             | 3      | <b>Address Bit 0 (I<sup>2</sup>C)</b> ( <i>Input</i> ) - AD0 is a chip address pin in I <sup>2</sup> C Mode.                                                                      |
| SPKR_OUTA+      | 4      | <b>PWM Speaker Output</b> ( <i>Output</i> ) - Full-bridge amplified PWM speaker outputs.                                                                                          |
| SPKR_OUTA-      | 6      |                                                                                                                                                                                   |
| SPKR_OUTB+      | 7      |                                                                                                                                                                                   |
| SPKR_OUTB-      | 9      |                                                                                                                                                                                   |
| VP              | 5<br>8 | <b>Power for PWM Drivers</b> ( <i>Input</i> ) - Power supply for the PWM output driver stages.                                                                                    |
| -VHPFILT        | 10     | <b>Inverting Charge Pump Filter Connection</b> ( <i>Output</i> ) - Power supply from the inverting charge pump that provides the negative rail for the headphone/line amplifiers. |
| FLYN            | 11     | <b>Charge Pump Cap Negative Node</b> ( <i>Output</i> ) - Negative node for the inverting charge pump's flying capacitor.                                                          |
| FLYP            | 12     | <b>Charge Pump Cap Positive Node</b> ( <i>Output</i> ) - Positive node for the inverting charge pump's flying capacitor.                                                          |
| +VHP            | 13     | <b>Positive Analog Power for Headphone</b> ( <i>Input</i> ) - Positive voltage rail and power for the internal headphone amplifiers and inverting charge pump.                    |
| HP/LINE_OUTB, A | 14,15  | <b>Headphone/Line Audio Output</b> ( <i>Output</i> ) - Stereo headphone or line level analog outputs.                                                                             |
| VA              | 16     | <b>Analog Power</b> ( <i>Input</i> ) - Positive power for the internal analog section.                                                                                            |

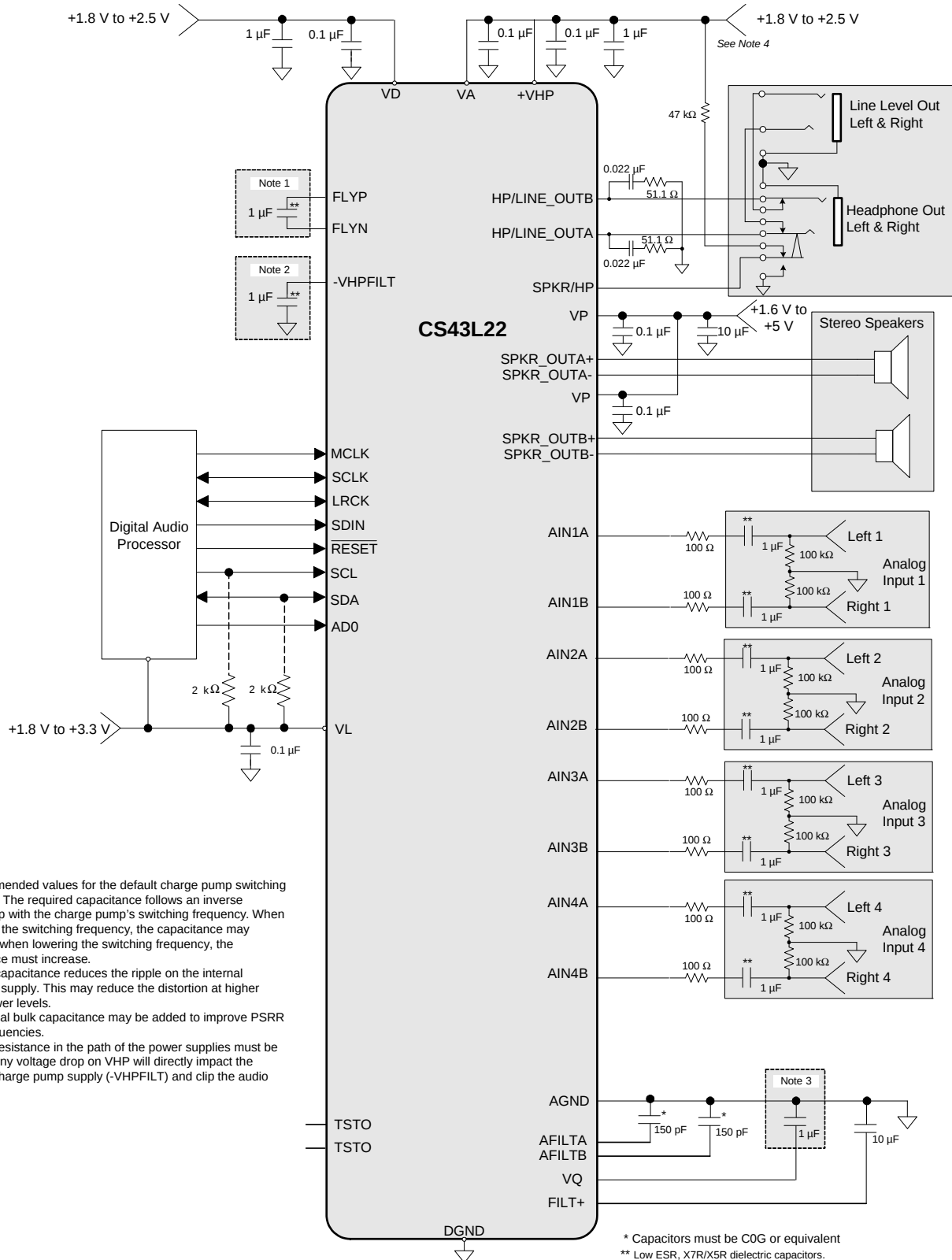
|                 |       |                                                                                                                                               |
|-----------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| AGND            | 17    | <b>Analog Ground (Input)</b> - Ground reference for the internal analog section.                                                              |
| FILT+           | 18    | <b>Positive Voltage Reference (Output)</b> - Filter connection for the internal sampling circuits.                                            |
| VQ              | 19    | <b>Quiescent Voltage (Output)</b> - Filter connection for the internal quiescent voltage.                                                     |
| TSTO            | 20,36 | <b>Test Out (Output)</b> - This pin is an output used for test purposes only and must be left "floating" (no connection external to the pin). |
| AIN4A,B         | 21,22 | <b>Line-Level Analog Inputs (Input)</b> - Single-ended stereo line-level analog inputs.                                                       |
| AIN3A,B         | 23,24 |                                                                                                                                               |
| AIN2A,B         | 25,26 |                                                                                                                                               |
| AIN1A,B         | 29,30 |                                                                                                                                               |
| AFILTA,AFILTB   | 27,28 | <b>Anti-alias Filter Connection (Output)</b> - Anti-alias filter connection for analog passthrough mode.                                      |
| SPKR/HP         | 31    | <b>Speaker/Headphone Switch (Input)</b> - Powers down the left and/or right channel of the speaker and/or headphone outputs.                  |
| RESET           | 32    | <b>Reset (Input)</b> - The device enters a low power mode when this pin is driven low.                                                        |
| VL              | 33    | <b>Digital Interface Power (Input)</b> - Determines the required signal level for the serial audio interface and host control port.           |
| VD              | 34    | <b>Digital Power (Input)</b> - Positive power for the internal digital section.                                                               |
| DGND            | 35    | <b>Digital Ground (Input)</b> - Ground reference for the internal digital section.                                                            |
| MCLK            | 37    | <b>Master Clock (Input)</b> - Clock source for the delta-sigma modulators.                                                                    |
| SCLK            | 38    | <b>Serial Clock (Input/Output)</b> - Serial clock for the serial audio interface.                                                             |
| SDIN            | 39    | <b>Serial Audio Data Input (Input)</b> - Input for two's complement serial audio data.                                                        |
| LRCK            | 40    | <b>Left Right Clock (Input/Output)</b> - Determines which channel, Left or Right, is currently active on the serial audio data line.          |
| GND/Thermal Pad | -     | Ground reference for PWM power FETs and charge pump; thermal relief pad for optimized heat dissipation.                                       |

## 1.1 I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

| Power Supply | Pin Name   | I/O          | Internal Connections | Driver                           | Receiver                         |
|--------------|------------|--------------|----------------------|----------------------------------|----------------------------------|
| VL           | RESET      | Input        | -                    | -                                | 1.65 V - 3.47 V, with Hysteresis |
|              | AD0        | Input        | -                    | -                                | 1.65 V - 3.47 V, with Hysteresis |
|              | SCL        | Input        | -                    | -                                | 1.65 V - 3.47 V, with Hysteresis |
|              | SDA        | Input/Output | -                    | 1.65 V - 3.47 V, CMOS/Open Drain | 1.65 V - 3.47 V, with Hysteresis |
|              | MCLK       | Input        | -                    | -                                | 1.65 V - 3.47 V                  |
|              | LRCK       | Input/Output | Weak Pull-up (~1 MΩ) | 1.65 V - 3.47 V, CMOS            | 1.65 V - 3.47 V                  |
|              | SCLK       | Input/Output | Weak Pull-up (~1 MΩ) | 1.65 V - 3.47 V, CMOS            | 1.65 V - 3.47 V                  |
|              | SDIN       | Input        | -                    | -                                | 1.65 V - 3.47 V                  |
| VA           | SPKR/HP    | Input        | -                    | -                                | 1.65 V - 2.63 V                  |
| VP           | SPKR_OUTA+ | Output       | -                    | 1.6 V - 5.25 V Power MOSFET      | -                                |
|              | SPKR_OUTA- | Output       | -                    | 1.6 V - 5.25 V Power MOSFET      | -                                |
|              | SPKR_OUTB+ | Output       | -                    | 1.6 V - 5.25 V Power MOSFET      | -                                |
|              | SPKR_OUTB- | Output       | -                    | 1.6 V - 5.25 V Power MOSFET      | -                                |

## 2. TYPICAL CONNECTION DIAGRAM



**Figure 1. Typical Connection Diagram**

### 3. CHARACTERISTIC AND SPECIFICATIONS

#### RECOMMENDED OPERATING CONDITIONS

AGND=DGND=0 V, all voltages with respect to ground.

| Parameters                    | Symbol              | Min  | Max  | Units |
|-------------------------------|---------------------|------|------|-------|
| DC Power Supply               |                     |      |      |       |
| Analog                        | VA                  | 1.65 | 2.63 | V     |
| Headphone Amplifier           | +VHP                | 1.65 | 2.63 | V     |
| Speaker Amplifier             | VP                  | 1.60 | 5.25 | V     |
| Digital                       | VD                  | 1.65 | 2.63 | V     |
| Serial/Control Port Interface | VL                  | 1.65 | 3.47 | V     |
| Ambient Temperature           | Commercial<br>$T_A$ | -40  | +85  | °C    |

#### ABSOLUTE MAXIMUM RATINGS

AGND = DGND = 0 V; all voltages with respect to ground.

| Parameters                                    | Symbol                | Min        | Max        | Units |
|-----------------------------------------------|-----------------------|------------|------------|-------|
| DC Power Supply                               |                       |            |            |       |
| Analog                                        | VA, VHP               | -0.3       | 3.0        | V     |
| Speaker                                       | VP                    | -0.3       | 5.5        | V     |
| Digital                                       | VD                    | -0.3       | 3.0        | V     |
| Serial/Control Port Interface                 | VL                    | -0.3       | 4.0        | V     |
| Input Current                                 | (Note 1)<br>$I_{in}$  | -          | ±10        | mA    |
| Analog Input Voltage                          | (Note 2)<br>$V_{IN}$  | AGND-0.7   | VA+0.7     | V     |
| External Voltage Applied to Analog Input      | (Note 2)<br>$V_{IN}$  | AGND-0.3   | VA+0.3     | V     |
| External Voltage Applied to Analog Output     | $V_{IN}$              | -VHP - 0.3 | +VHP + 0.3 | V     |
| External Voltage Applied to Digital Input     | (Note 2)<br>$V_{IND}$ | -0.3       | VL+ 0.3    | V     |
| Ambient Operating Temperature (power applied) | $T_A$                 | -50        | +115       | °C    |
| Storage Temperature                           | $T_{stg}$             | -65        | +150       | °C    |

**WARNING:** Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

#### Notes:

- Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
- The maximum over/under voltage is limited by the input current.

## ANALOG OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; All Supplies =  $V_A$ ;  $T_A = +25^\circ\text{C}$ ; Sample Frequency = 48 kHz; Measurement bandwidth is 20 Hz to 20 kHz; Test load  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$  for the line output (see [Figure 2](#)); Test load  $R_L = 16\text{ }\Omega$ ,  $C_L = 10\text{ pF}$  (see [Figure 2](#)) for the headphone output;  $\text{HP\_GAIN}[2:0] = 011$ .

| Parameters (Note 3)                                                   |                            | VA = 2.5 V                                                         |        |      | VA = 1.8 V |        |      | Unit   |
|-----------------------------------------------------------------------|----------------------------|--------------------------------------------------------------------|--------|------|------------|--------|------|--------|
|                                                                       |                            | Min                                                                | Typ    | Max  | Min        | Typ    | Max  |        |
| <b><i>R<sub>L</sub> = 10 kΩ</i></b>                                   |                            |                                                                    |        |      |            |        |      |        |
| <b><i>Dynamic Range</i></b>                                           |                            |                                                                    |        |      |            |        |      |        |
| 18 to 24-Bit                                                          | A-weighted                 | 92                                                                 | 98     | -    | 89         | 95     | -    | dB     |
|                                                                       | unweighted                 | 89                                                                 | 95     | -    | 86         | 92     | -    | dB     |
|                                                                       | 16-Bit A-weighted          | -                                                                  | 96     | -    | -          | 93     | -    | dB     |
|                                                                       | unweighted                 | -                                                                  | 93     | -    | -          | 90     | -    | dB     |
| <b><i>Total Harmonic Distortion + Noise</i></b>                       |                            |                                                                    |        |      |            |        |      |        |
| 18 to 24-Bit                                                          | 0 dB                       | -                                                                  | -86    | -80  | -          | -88    | -82  | dB     |
|                                                                       | -20 dB                     | -                                                                  | -75    | -    | -          | -72    | -    | dB     |
|                                                                       | -60 dB                     | -                                                                  | -35    | -29  | -          | -32    | -26  | dB     |
|                                                                       | 16-Bit 0 dB                | -                                                                  | -86    | -    | -          | -88    | -    | dB     |
|                                                                       | -20 dB                     | -                                                                  | -73    | -    | -          | -70    | -    | dB     |
|                                                                       | -60 dB                     | -                                                                  | -33    | -    | -          | -30    | -    | dB     |
| <b><i>R<sub>L</sub> = 16 Ω</i></b>                                    |                            |                                                                    |        |      |            |        |      |        |
| <b><i>Dynamic Range</i></b>                                           |                            |                                                                    |        |      |            |        |      |        |
| 18 to 24-Bit                                                          | A-weighted                 | 92                                                                 | 98     | -    | 89         | 95     | -    | dB     |
|                                                                       | unweighted                 | 89                                                                 | 95     | -    | 86         | 92     | -    | dB     |
|                                                                       | 16-Bit A-weighted          | -                                                                  | 96     | -    | -          | 93     | -    | dB     |
|                                                                       | unweighted                 | -                                                                  | 93     | -    | -          | 90     | -    | dB     |
| <b><i>Total Harmonic Distortion + Noise</i></b>                       |                            |                                                                    |        |      |            |        |      |        |
| 18 to 24-Bit                                                          | 0 dB                       | -                                                                  | -75    | -69  | -          | -75    | -69  | dB     |
|                                                                       | -20 dB                     | -                                                                  | -75    | -    | -          | -72    | -    | dB     |
|                                                                       | -60 dB                     | -                                                                  | -35    | -29  | -          | -32    | -26  | dB     |
|                                                                       | 16-Bit 0 dB                | -                                                                  | -75    | -    | -          | -75    | -    | dB     |
|                                                                       | -20 dB                     | -                                                                  | -73    | -    | -          | -70    | -    | dB     |
|                                                                       | -60 dB                     | -                                                                  | -33    | -    | -          | -30    | -    | dB     |
| <b><i>Other Characteristics for R<sub>L</sub> = 16 Ω or 10 kΩ</i></b> |                            |                                                                    |        |      |            |        |      |        |
| Output Parameters (Note 4)                                            | Modulation Index (MI)      | -                                                                  | 0.6787 | -    | -          | 0.6787 | -    | V/V    |
|                                                                       | Analog Gain Multiplier (G) | -                                                                  | 0.6047 | -    | -          | 0.6047 | -    | V/V    |
| Full-scale Output Voltage (2•G•MI•VA) (Note 4)                        |                            | Refer to Table "Headphone Output Power Characteristics" on page 14 |        |      |            |        |      | Vpp    |
| Full-scale Output Power (Note 4)                                      |                            | Refer to Table "Headphone Output Power Characteristics" on page 14 |        |      |            |        |      |        |
| Interchannel Isolation (1 kHz)                                        | 16 Ω                       | -                                                                  | 80     | -    | -          | 80     | -    | dB     |
|                                                                       | 10 kΩ                      | -                                                                  | 95     | -    | -          | 93     | -    | dB     |
| Speaker Amp to HP Amp Isolation                                       |                            | -                                                                  | 80     | -    | -          | 80     | -    | dB     |
| Interchannel Gain Mismatch                                            |                            | -                                                                  | 0.1    | 0.25 | -          | 0.1    | 0.25 | dB     |
| Gain Drift                                                            |                            | -                                                                  | ±100   | -    | -          | ±100   | -    | ppm/°C |
| AC-Load Resistance (R <sub>L</sub> ) (Note 5)                         |                            | 16                                                                 | -      | -    | 16         | -      | -    | Ω      |
| Load Capacitance (C <sub>L</sub> ) (Note 5)                           |                            | -                                                                  | -      | 150  | -          | -      | 150  | pF     |

- One (least-significant bit) LSB of triangular PDF dither is added to data.
- Full-scale output voltage and power is determined by the gain setting, G, in register "Headphone Analog Gain" on page 43. High gain settings at certain  $V_A$  and VHP supply levels may cause clipping when the audio signal approaches full-scale, maximum power output, as shown in [Figures 18 - 21 on page 60](#).

5. See Figure 2.  $R_L$  and  $C_L$  reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity. In this circuit topology,  $C_L$  will effectively move the band-limiting pole of the amp in the output stage. Increasing this value beyond the recommended 150 pF can cause the internal op-amp to become unstable.

## ANALOG PASSTHROUGH CHARACTERISTICS

Test Conditions (unless otherwise specified): Input sine wave (relative to full-scale): 1 kHz through passive input filter; Passthrough Amplifier and HP/Line Gain = 0 dB; All Supplies = VA;  $T_A = +25^\circ\text{C}$ ; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz.

| Parameters                        |            | VA = 2.5 V |         |     | VA = 1.8 V |         |     | Unit |
|-----------------------------------|------------|------------|---------|-----|------------|---------|-----|------|
|                                   |            | Min        | Typ     | Max | Min        | Typ     | Max |      |
| Analog In to HP/Line Amp          |            |            |         |     |            |         |     |      |
| RL = 10 kΩ                        |            |            |         |     |            |         |     |      |
| Dynamic Range                     | A-weighted | -          | -96     | -   | -          | -94     | -   | dB   |
|                                   | unweighted | -          | -93     | -   | -          | -91     | -   | dB   |
| Total Harmonic Distortion + Noise | -1 dBFS    | -          | -70     | -   | -          | -70     | -   | dB   |
|                                   | -20 dBFS   | -          | -73     | -   | -          | -71     | -   | dB   |
|                                   | -60 dBFS   | -          | -33     | -   | -          | -31     | -   | dB   |
| Full-scale Input Voltage          |            | -          | 0.91•VA | -   | -          | 0.91•VA | -   | Vpp  |
| Full-scale Output Voltage         |            | -          | 0.84•VA | -   | -          | 0.84•VA | -   | Vpp  |
| Passband Ripple                   |            | -          | 0/-0.3  | -   | -          | 0/-0.3  | -   | dB   |
| RL = 16 Ω                         |            |            |         |     |            |         |     |      |
| Dynamic Range                     | A-weighted | -          | -96     | -   | -          | -94     | -   | dB   |
|                                   | unweighted | -          | -93     | -   | -          | -91     | -   | dB   |
| Total Harmonic Distortion + Noise | -1 dBFS    | -          | -70     | -   | -          | -70     | -   | dB   |
|                                   | -20 dBFS   | -          | -73     | -   | -          | -71     | -   | dB   |
|                                   | -60 dBFS   | -          | -33     | -   | -          | -31     | -   | dB   |
| Full-scale Input Voltage          |            | -          | 0.91•VA | -   | -          | 0.91•VA | -   | Vpp  |
| Full-scale Output Voltage         |            | -          | 0.84•VA | -   | -          | 0.84•VA | -   | Vpp  |
| Output Power                      |            | -          | 32      | -   | -          | 17      | -   | mW   |
| Passband Ripple                   |            | -          | 0/-0.3  | -   | -          | 0/-0.3  | -   | dB   |

## PWM OUTPUT CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full scale 997 Hz signal; MCLK = 12.2880 MHz; Measurement Bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load  $R_L = 8\ \Omega$  for stereo full-bridge,  $R_L = 4\ \Omega$  for mono parallel full-bridge;  $V_D = V_L = V_A = V_{HP} = 1.8V$ ; PWM Modulation Index of 0.85; PWM Switch Rate = 384 kHz.

| Parameters (Note 7)                      | Symbol       | Conditions                                                       | Min | Typ          | Max | Units                  |
|------------------------------------------|--------------|------------------------------------------------------------------|-----|--------------|-----|------------------------|
| <b>VP = 5.0 V</b>                        |              |                                                                  |     |              |     |                        |
| <b>Power Output per Channel</b>          | $P_O$        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 1.00<br>0.80 | -   | $W_{rms}$<br>$W_{rms}$ |
| Mono Parallel Full-Bridge                |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 1.90<br>1.50 | -   | $W_{rms}$<br>$W_{rms}$ |
| <b>Total Harmonic Distortion + Noise</b> | THD+N        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = 0\ dBFS = 0.8W$                                           | -   | 0.52         | -   | %                      |
| Mono Parallel Full-Bridge                |              | $P_O = -3\ dBFS = 0.75\ W$<br>$P_O = 0\ dBFS = 1.5\ W$           | -   | 0.10<br>0.50 | -   | %<br>%                 |
| <b>Dynamic Range</b>                     | DR           |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 91<br>88     | -   | dB<br>dB               |
| Mono Parallel Full-Bridge                |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 91<br>88     | -   | dB<br>dB               |
| <b>VP = 3.7 V</b>                        |              |                                                                  |     |              |     |                        |
| <b>Power Output per Channel</b>          | $P_O$        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 0.55<br>0.45 | -   | $W_{rms}$<br>$W_{rms}$ |
| Mono Parallel Full-Bridge                |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 1.00<br>0.84 | -   | $W_{rms}$<br>$W_{rms}$ |
| <b>Total Harmonic Distortion + Noise</b> | THD+N        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = 0\ dBFS = 0.43\ W$                                        | -   | 0.54         | -   | %                      |
| Mono Parallel Full-Bridge                |              | $P_O = -3\ dBFS = 0.41\ W$<br>$P_O = 0\ dBFS = 0.81\ W$          | -   | 0.09<br>0.45 | -   | %<br>%                 |
| <b>Dynamic Range</b>                     | DR           |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 91<br>88     | -   | dB<br>dB               |
| Mono Parallel Full-Bridge                |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 95<br>92     | -   | dB<br>dB               |
| <b>VP = 2.5 V</b>                        |              |                                                                  |     |              |     |                        |
| <b>Power Output per Channel</b>          | $P_O$        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 0.23<br>0.19 | -   | $W_{rms}$<br>$W_{rms}$ |
| Mono Parallel Full-Bridge                |              | THD+N < 10%<br>THD+N < 1%                                        | -   | 0.44<br>0.35 | -   | $W_{rms}$<br>$W_{rms}$ |
| <b>Total Harmonic Distortion + Noise</b> | THD+N        |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = 0\ dBFS = 0.18\ W$                                        | -   | 0.50         | -   | %                      |
| Mono Parallel Full-Bridge                |              | $P_O = -3\ dBFS = 0.17\ W$<br>$P_O = 0\ dBFS = 0.35\ W$          | -   | 0.08<br>0.43 | -   | %<br>%                 |
| <b>Dynamic Range</b>                     | DR           |                                                                  |     |              |     |                        |
| Stereo Full-Bridge                       |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 91<br>88     | -   | dB<br>dB               |
| Mono Parallel Full-Bridge                |              | $P_O = -60\ dBFS$ , A-Weighted<br>$P_O = -60\ dBFS$ , Unweighted | -   | 94<br>91     | -   | dB<br>dB               |
| MOSFET On Resistance                     | $R_{DS(ON)}$ | VP = 5.0V, $I_d = 0.5\ A$                                        | -   | 600          | -   | m $\Omega$             |
| MOSFET On Resistance                     | $R_{DS(ON)}$ | VP = 3.7V, $I_d = 0.5\ A$                                        | -   | 640          | -   | m $\Omega$             |

| Parameters (Note 7)           | Symbol       | Conditions                                          | Min | Typ | Max | Units      |
|-------------------------------|--------------|-----------------------------------------------------|-----|-----|-----|------------|
| MOSFET On Resistance          | $R_{DS(ON)}$ | $V_P = 2.5V, I_d = 0.5 A$                           | -   | 760 | -   | m $\Omega$ |
| Efficiency                    | $\eta$       | $V_P = 5.0 V, P_O = 2 \times 0.8 W, R_L = 8 \Omega$ | -   | 81  | -   | %          |
| Output Operating Peak Current | $I_{PC}$     |                                                     | -   | -   | 1.5 | A          |
| VP Input Current During Reset | $I_{VP}$     | $\overline{RESET}$ , pin 32, is held low            | -   | 0.8 | 5.0 | $\mu A$    |

6. The PWM driver should be used in captive speaker systems only.

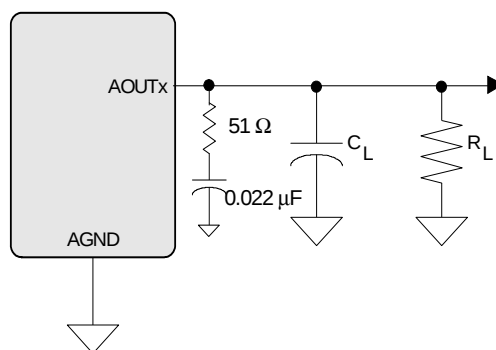
7. Optimal PWM performance is achieved when MCLK > 12 MHz.

## HEADPHONE OUTPUT POWER CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; Sample Frequency = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Test load  $R_L = 16 \Omega$ ,  $C_L = 10$  pF (see Figure 2); "Required Initialization Settings" on page 32 written on power up.

| Parameters                                           |                 |       | VA = 2.5V                                    |     |     | VA = 1.8V                                    |     |     | Unit              |
|------------------------------------------------------|-----------------|-------|----------------------------------------------|-----|-----|----------------------------------------------|-----|-----|-------------------|
|                                                      |                 |       | Min                                          | Typ | Max | Min                                          | Typ | Max |                   |
| <b>AOUTx Power Into <math>R_L = 16 \Omega</math></b> |                 |       |                                              |     |     |                                              |     |     |                   |
| HP_GAIN[2:0]                                         | Analog Gain (G) | VHP   |                                              |     |     |                                              |     |     |                   |
| 000                                                  | 0.3959          | 1.8 V | -                                            | 14  | -   | -                                            | 7   | -   | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V | -                                            | 14  | -   | -                                            | 7   | -   | mW <sub>rms</sub> |
| 001                                                  | 0.4571          | 1.8 V | -                                            | 19  | -   | -                                            | 10  | -   | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V | -                                            | 19  | -   | -                                            | 10  | -   | mW <sub>rms</sub> |
| 010                                                  | 0.5111          | 1.8 V | -                                            | 23  | -   | -                                            | 12  | -   | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V | -                                            | 23  | -   | -                                            | 12  | -   | mW <sub>rms</sub> |
| 011 (default)                                        | 0.6047          | 1.8 V | (Note 8)                                     |     |     | -                                            | 17  | -   | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V | -                                            | 32  | -   | -                                            | 17  | -   | mW <sub>rms</sub> |
| 100                                                  | 0.7099          | 1.8 V | (Note 8)                                     |     |     | -                                            | 23  | -   | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V | -                                            | 44  | -   | -                                            | 23  | -   | mW <sub>rms</sub> |
| 101                                                  | 0.8399          | 1.8 V | (Note 4, 8) See Figures 18 and 19 on page 59 |     |     | (Note 4) See Figure 18 on page 59            |     |     | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V |                                              |     |     | -                                            | 32  | -   | mW <sub>rms</sub> |
| 110                                                  | 1.0000          | 1.8 V | (Note 4, 8) See Figures 18 and 19 on page 59 |     |     | (Note 4, 8) See Figures 18 and 19 on page 59 |     |     | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V |                                              |     |     |                                              |     |     | mW <sub>rms</sub> |
| 111                                                  | 1.1430          | 1.8 V | (Note 4, 8) See Figures 18 and 19 on page 59 |     |     | (Note 4, 8) See Figures 18 and 19 on page 59 |     |     | mW <sub>rms</sub> |
|                                                      |                 | 2.5 V |                                              |     |     |                                              |     |     | mW <sub>rms</sub> |

8. VHP settings lower than VA reduces the headroom of the headphone amplifier. As a result, the DAC may not achieve the full THD+N performance at full-scale output voltage and power.



**Figure 2. Headphone Output Test Load**

## LINE OUTPUT VOLTAGE LEVEL CHARACTERISTICS

Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; measurement bandwidth is 20 Hz to 20 kHz; Sample Frequency = 48 kHz; Test load  $R_L = 10\text{ k}\Omega$ ,  $C_L = 10\text{ pF}$  (see [Figure 2](#)); “Required Initialization Settings” on [page 32](#) written on power up.

| Parameters                                                     |                 |       | VA = 2.5V                       |      |      | VA = 1.8V |      |      | Unit     |
|----------------------------------------------------------------|-----------------|-------|---------------------------------|------|------|-----------|------|------|----------|
|                                                                |                 |       | Min                             | Typ  | Max  | Min       | Typ  | Max  |          |
| <b>AOUTx Voltage Into <math>R_L = 10\text{ k}\Omega</math></b> |                 |       |                                 |      |      |           |      |      |          |
| HP_GAIN[2:0]                                                   | Analog Gain (G) | VHP   |                                 |      |      |           |      |      |          |
| 000                                                            | 0.3959          | 1.8 V | -                               | 1.34 | -    | -         | 0.97 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 1.34 | -    | -         | 0.97 | -    | $V_{pp}$ |
| 001                                                            | 0.4571          | 1.8 V | -                               | 1.55 | -    | -         | 1.12 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 1.55 | -    | -         | 1.12 | -    | $V_{pp}$ |
| 010                                                            | 0.5111          | 1.8 V | -                               | 1.73 | -    | -         | 1.25 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 1.73 | -    | -         | 1.25 | -    | $V_{pp}$ |
| 011 (default)                                                  | 0.6047          | 1.8 V | -                               | 2.05 | -    | 1.41      | 1.48 | 1.55 | $V_{pp}$ |
|                                                                |                 | 2.5 V | 1.95                            | 2.05 | 2.15 | -         | 1.48 | -    | $V_{pp}$ |
| 100                                                            | 0.7099          | 1.8 V | -                               | 2.41 | -    | -         | 1.73 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 2.41 | -    | -         | 1.73 | -    | $V_{pp}$ |
| 101                                                            | 0.8399          | 1.8 V | -                               | 2.85 | -    | -         | 2.05 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 2.85 | -    | -         | 2.05 | -    | $V_{pp}$ |
| 110                                                            | 1.0000          | 1.8 V | -                               | 3.39 | -    | -         | 2.44 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 3.39 | -    | -         | 2.44 | -    | $V_{pp}$ |
| 111                                                            | 1.1430          | 1.8 V | (See <a href="#">(Note 8)</a> ) |      |      |           | 2.79 | -    | $V_{pp}$ |
|                                                                |                 | 2.5 V | -                               | 3.88 | -    | -         | 2.79 | -    | $V_{pp}$ |

## COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

| Parameters <a href="#">(Note 9)</a>            | Min                | Typ  | Max         | Unit |
|------------------------------------------------|--------------------|------|-------------|------|
| Frequency Response 10 Hz to 20 kHz             | -0.01              | -    | +0.08       | dB   |
| Passband                                       | to -0.05 dB corner | 0    | 0.4780      | Fs   |
|                                                | to -3 dB corner    | 0    | 0.4996      | Fs   |
| StopBand                                       | 0.5465             | -    | -           | Fs   |
| StopBand Attenuation <a href="#">(Note 10)</a> | 50                 | -    | -           | dB   |
| Group Delay                                    | -                  | 9/Fs | -           | s    |
| De-emphasis Error                              | Fs = 32 kHz        | -    | +1.5/+0     | dB   |
|                                                | Fs = 44.1 kHz      | -    | +0.05/-0.25 | dB   |
|                                                | Fs = 48 kHz        | -    | -0.2/-0.4   | dB   |

9. Response is clock dependent and will scale with Fs. Note that the response plots ([Figures 22 and 25 on page 63](#)) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
10. Measurement Bandwidth is from Stopband to 3 Fs.

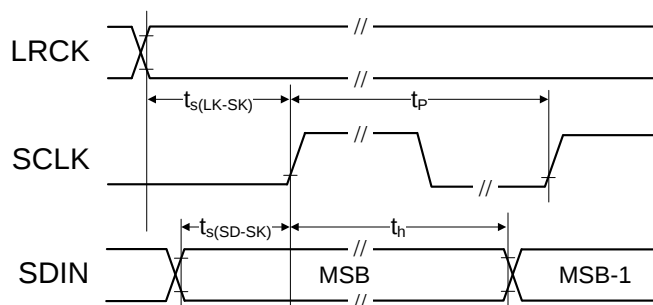
## SWITCHING SPECIFICATIONS - SERIAL PORT

Inputs: Logic 0 = DGND; Logic 1 = VL.

| Parameters                              | Symbol                | Min                                     | Max               | Units             |     |
|-----------------------------------------|-----------------------|-----------------------------------------|-------------------|-------------------|-----|
| RESET pin Low Pulse Width (Note 11)     |                       | 1                                       | -                 | ms                |     |
| MCLK Frequency (Note 12)                |                       | (See “Serial Port Clocking” on page 29) |                   | MHz               |     |
| MCLK Duty Cycle                         |                       | 45                                      | 55                | %                 |     |
| <b>Slave Mode</b>                       |                       |                                         |                   |                   |     |
| Sample Rate (LRCK)                      | F <sub>s</sub>        | (See “Serial Port Clocking” on page 29) |                   | kHz               |     |
| LRCK Duty Cycle                         |                       | 45                                      | 55                | %                 |     |
| SCLK Frequency                          | 1/t <sub>P</sub>      | -                                       | 64•F <sub>s</sub> | Hz                |     |
| SCLK Duty Cycle                         |                       | 45                                      | 55                | %                 |     |
| LRCK Setup Time Before SCLK Rising Edge | t <sub>s(LK-SK)</sub> | 40                                      | -                 | ns                |     |
| SDIN Setup Time Before SCLK Rising Edge | t <sub>s(SD-SK)</sub> | 20                                      | -                 | ns                |     |
| SDIN Hold Time After SCLK Rising Edge   | t <sub>h</sub>        | 20                                      | -                 | ns                |     |
| <b>Master Mode</b>                      |                       |                                         |                   |                   |     |
| Sample Rate (LRCK)                      | F <sub>s</sub>        | (See “Serial Port Clocking” on page 29) |                   | Hz                |     |
| LRCK Duty Cycle                         |                       | 45                                      | 55                | %                 |     |
| SCLK Frequency                          | SCLK=MCLK mode        | 1/t <sub>P</sub>                        | -                 | 12.0000           | MHz |
|                                         | MCLK=12.0000 MHz      | 1/t <sub>P</sub>                        | -                 | 68•F <sub>s</sub> | Hz  |
|                                         | all other modes       | 1/t <sub>P</sub>                        | -                 | 64•F <sub>s</sub> | Hz  |
| SCLK Duty Cycle                         |                       | 45                                      | 55                | %                 |     |
| SDIN Setup Time Before SCLK Rising Edge | t <sub>s(SD-SK)</sub> | 20                                      | -                 | ns                |     |
| SDIN Hold Time After SCLK Rising Edge   | t <sub>h</sub>        | 20                                      | -                 | ns                |     |

11. After powering up the CS43L22, RESET should be held low after the power supplies and clocks are settled.

12. See "Example System Clock Frequencies" on page 61 for typical MCLK frequencies.



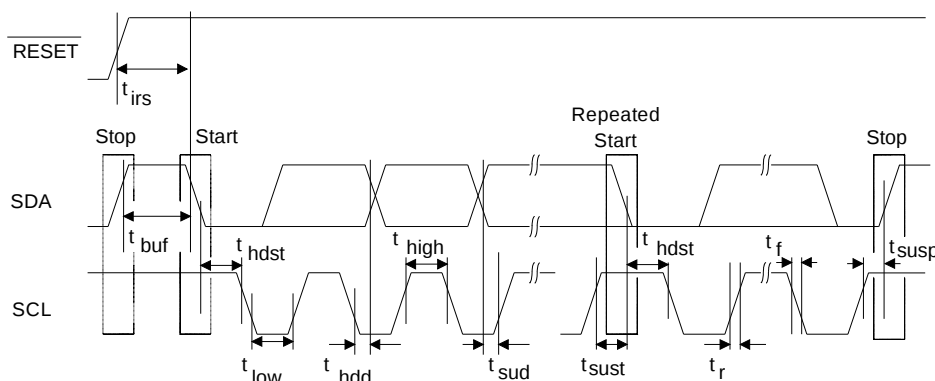
**Figure 3. Serial Audio Interface Timing**

## SWITCHING SPECIFICATIONS - I<sup>2</sup>C CONTROL PORT

Inputs: Logic 0 = DGND; Logic 1 = V; SDA C<sub>L</sub> = 30 pF.

| Parameters                                             | Symbol     | Min | Max  | Unit |
|--------------------------------------------------------|------------|-----|------|------|
| SCL Clock Frequency                                    | $f_{scl}$  | -   | 100  | kHz  |
| RESET Rising Edge to Start                             | $t_{irs}$  | 550 | -    | ns   |
| Bus Free Time Between Transmissions                    | $t_{buf}$  | 4.7 | -    | μs   |
| Start Condition Hold Time (prior to first clock pulse) | $t_{hdst}$ | 4.0 | -    | μs   |
| Clock Low time                                         | $t_{low}$  | 4.7 | -    | μs   |
| Clock High Time                                        | $t_{high}$ | 4.0 | -    | μs   |
| Setup Time for Repeated Start Condition                | $t_{sust}$ | 4.7 | -    | μs   |
| SDA Hold Time from SCL Falling (Note 13)               | $t_{hdd}$  | 0   | -    | μs   |
| SDA Setup time to SCL Rising                           | $t_{sud}$  | 250 | -    | ns   |
| Rise Time of SCL and SDA                               | $t_{rc}$   | -   | 1    | μs   |
| Fall Time SCL and SDA                                  | $t_{fc}$   | -   | 300  | ns   |
| Setup Time for Stop Condition                          | $t_{susp}$ | 4.7 | -    | μs   |
| Acknowledge Delay from SCL Falling                     | $t_{ack}$  | 300 | 1000 | ns   |

13. Data must be held for sufficient time to bridge the transition time,  $t_{fc}$ , of SCL.



**Figure 4. Control Port Timing - I<sup>2</sup>C**

## DC ELECTRICAL CHARACTERISTICS

AGND = 0 V; all voltages with respect to ground.

| Parameters                                          | Min                     | Typ    | Max | Units |    |
|-----------------------------------------------------|-------------------------|--------|-----|-------|----|
| <b>VQ Characteristics</b>                           |                         |        |     |       |    |
| Nominal Voltage                                     | -                       | 0.5•VA | -   | V     |    |
| Output Impedance                                    | -                       | 23     | -   | kΩ    |    |
| DC Current Source/Sink                              | -                       | -      | 1   | μA    |    |
| <b>Power Supply Rejection Ratio Characteristics</b> |                         |        |     |       |    |
| PSRR @ 1 kHz (Note 14)                              | DAC (HP & Line Amps)    | -      | 60  | -     | dB |
| PSRR @ 60 Hz (Note 14)                              | DAC (HP & Line Amps)    | -      | 60  | -     | dB |
| PSRR @ 217 Hz                                       | Full-Bridge PWM Outputs | -      | 56  | -     | dB |

14. Valid with the recommended capacitor values on FILT+ and VQ. Increasing the capacitance will also increase the PSRR.

## DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

| Parameters (Note 15)                                  | Symbol          | Min                  | Max                 | Units |
|-------------------------------------------------------|-----------------|----------------------|---------------------|-------|
| Input Leakage Current                                 | I <sub>in</sub> | -                    | ±10                 | μA    |
| Input Capacitance                                     |                 | -                    | 10                  | pF    |
| <b>1.8 V - 3.3 V Logic</b>                            |                 |                      |                     |       |
| High-Level Output Voltage (I <sub>OH</sub> = -100 μA) | V <sub>OH</sub> | V <sub>L</sub> - 0.2 | -                   | V     |
| Low-Level Output Voltage (I <sub>OL</sub> = 100 μA)   | V <sub>OL</sub> | -                    | 0.2                 | V     |
| High-Level Input Voltage                              | V <sub>IH</sub> | 0.85•V <sub>L</sub>  | -                   | V     |
|                                                       |                 | 0.77•V <sub>L</sub>  | -                   | V     |
|                                                       |                 | 0.68•V <sub>L</sub>  | -                   | V     |
|                                                       |                 | 0.65•V <sub>L</sub>  | -                   | V     |
| Low-Level Input Voltage                               | V <sub>IL</sub> | -                    | 0.30•V <sub>L</sub> | V     |

15. See "I/O Pin Characteristics" on page 8 for serial and control port power rails.

**POWER CONSUMPTION** See (Note 16)

|   | Operation                       | Register Settings |               |               |                |                | V          | Typical Current (mA) |                 |                 |                                         |                            | Total Power (mW <sub>rms</sub> ) |
|---|---------------------------------|-------------------|---------------|---------------|----------------|----------------|------------|----------------------|-----------------|-----------------|-----------------------------------------|----------------------------|----------------------------------|
|   |                                 | 02h               | 04h           |               |                |                |            | i <sub>VHP</sub>     | i <sub>VA</sub> | i <sub>VD</sub> | i <sub>VL</sub><br>VL=3.3V<br>(Note 19) | i <sub>VP</sub><br>VP=3.7V |                                  |
|   |                                 | PDN[7:0]          | PDN_HP[B[1:0] | PDN_HP[A[1:0] | PDN_SPK[B[1:0] | PDN_SPK[A[1:0] |            |                      |                 |                 |                                         |                            |                                  |
| 1 | Off (Note 17)                   | x                 | x             | x             | x              | x              | 1.8<br>2.5 | 0.00<br>0.00         | 0.00<br>0.00    | 0.00<br>0.00    | 0.00<br>0.00                            | 0.00<br>0.00               |                                  |
| 2 | Standby (Note 18)               | 0x9F              | x             | x             | x              | x              | 1.8<br>2.5 | 0.00<br>0.00         | 0.00<br>0.00    | 0.01<br>0.02    | 0.00<br>0.00                            | 0.00<br>0.00               | 0.02<br>0.05                     |
| 3 | Stereo Passthrough to Headphone | 0x9E              | 10            | 10            | 11             | 11             | 1.8<br>2.5 | 2.79<br>3.18         | 1.91<br>2.14    | 1.06<br>1.81    | 0.01<br>0.00                            | 0.00<br>0.00               | 10.39<br>17.85                   |
| 4 | Mono Playback to Headphone      | 0x9E              | 10            | 11            | 11             | 11             | 1.8<br>2.5 | 1.59<br>2.07         | 1.99<br>2.62    | 2.72<br>4.27    | 0.01<br>0.00                            | 0.00<br>0.00               | 11.36<br>22.43                   |
| 5 | Stereo Playback to Headphone    | 0x9E              | 10            | 10            | 11             | 11             | 1.8<br>2.5 | 2.77<br>3.27         | 2.00<br>2.63    | 2.91<br>4.28    | 0.01<br>0.00                            | 0.00<br>0.00               | 13.84<br>25.48                   |
| 6 | Mono Playback to Speaker        | 0x9E              | 11            | 11            | 10             | 10             | 1.8<br>2.5 | 0.00<br>0.00         | 0.20<br>0.22    | 4.42<br>6.77    | 0.01<br>1.00                            | 1.00<br>1.00               | 12.05<br>21.21                   |
| 7 | Stereo Playback to Speaker      | 0x9E              | 11            | 11            | 10             | 10             | 1.8<br>2.5 | 0.00<br>0.00         | 0.20<br>0.22    | 4.38<br>6.80    | 0.01<br>1.00                            | 1.00<br>1.00               | 11.98<br>21.28                   |

16. Unless otherwise noted, test conditions are as follows: All zeros input, Slave Mode, sample rate = 48 kHz; No load. Digital (VD) and logic (VL) supply current will vary depending on speed mode and master/slave operation. "Required Initialization Settings" on page 32 written on power up.

17.  $\overline{\text{RESET}}$  pin 25 held LO, all clocks and data lines are held LO.

18.  $\overline{\text{RESET}}$  pin 25 held HI, all clocks and data lines are held HI.

19. VL current will slightly increase in Master Mode.

---

## 4. APPLICATIONS

### 4.1 Overview

#### 4.1.1 Basic Architecture

The CS43L22 is a highly integrated, low power, 24-bit audio DAC comprised of a Digital Signal Processing Engine, headphone amplifiers, a digital PWM modulator and two full-bridge power back-ends. Other features include battery level monitoring and compensation and temperature monitoring. The DAC is designed using multi-bit delta-sigma techniques and operates at an oversampling ratio of 128Fs, where Fs is equal to the system sample rate.

The PWM modulator operates at a fixed frequency of 384 kHz. The power MOSFETs are configured for either stereo full-bridge or mono parallel full bridge output. The DAC operates in one of four sample rate speed modes: Quarter, Half, Single and Double. It accepts and is capable of generating serial port clocks (SCLK, LRCK) derived from an input Master Clock (MCLK).

#### 4.1.2 Line Inputs

4 pairs of stereo analog inputs are provided for applications that require analog passthrough directly to the HP/Line amplifiers. This analog input portion allows selection from and configuration of multiple combinations of these stereo sources.

#### 4.1.3 Line & Headphone Outputs

The analog output portion of the CS43L22 includes a headphone amplifier capable of driving headphone and line-level loads. An on-chip charge pump creates a negative headphone supply allowing a full-scale output swing centered around ground. This eliminates the need for large DC-Blocking capacitors and allows the amplifier to deliver more power to headphone loads at lower supply voltages.

#### 4.1.4 Speaker Driver Outputs

The Class D power amplifiers drive 8  $\Omega$  (stereo) and 4  $\Omega$  (mono) speakers directly, without the need for an external filter. The power MOSFETs are powered directly from a battery eliminating the efficiency loss associated with an external regulator. Battery level monitoring and compensation maintains a steady output as battery levels fall. A temperature monitor continually measures the die temperature and registers when predefined thresholds are exceeded. **NOTE:** The CS43L22 should only be used in captive speaker systems where the outputs are permanently tied to the speaker terminals.

#### 4.1.5 Fixed Function DSP Engine

The fixed-function digital signal processing engine processes the PCM serial input data. Independent volume control, left/right channel swaps, mono mixes, tone control and limiting functions also comprise the DSP engine.

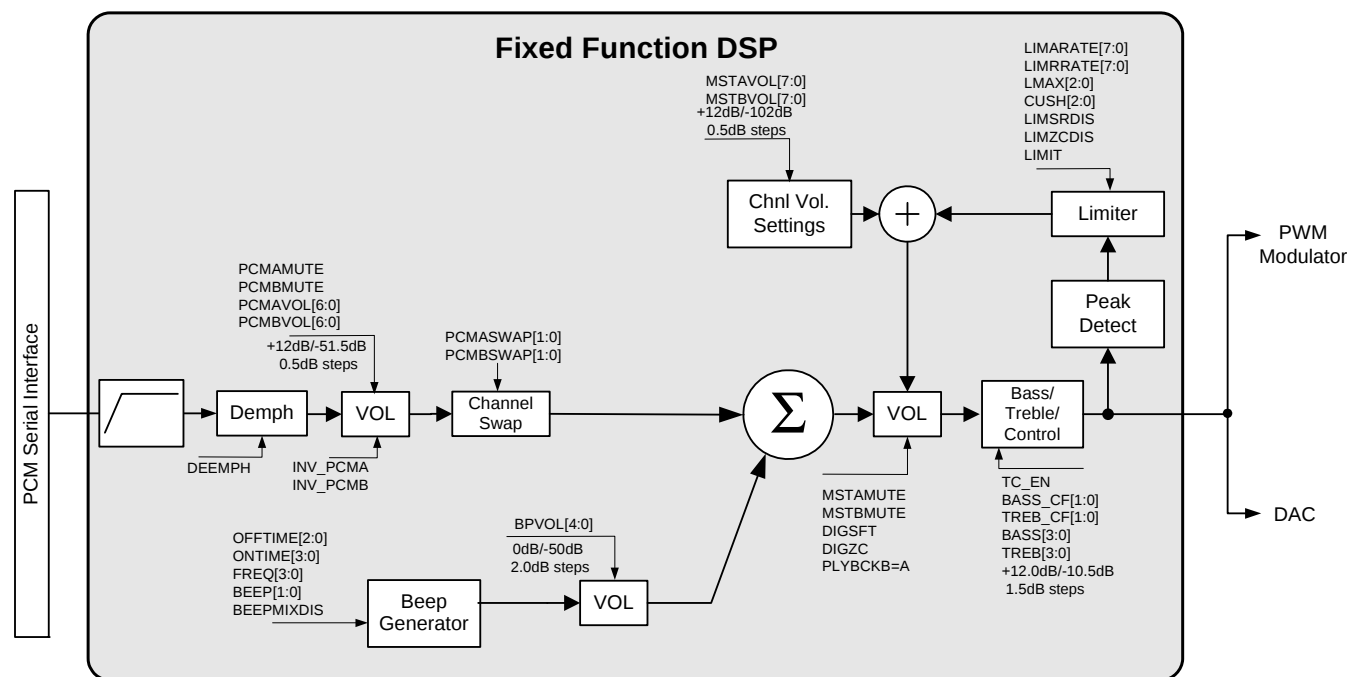
#### 4.1.6 Beep Generator

The beep generator delivers tones at select frequencies across approximately two octave major scales. With independent volume control, beeps may be configured to occur continuously, periodically, or at single time intervals.

#### 4.1.7 Power Management

Two control registers provide independent power-down control of the DAC, Headphone and Speaker output blocks in the CS43L22 allowing operation in select applications with minimal power consumption.

## 4.2 DSP Engine



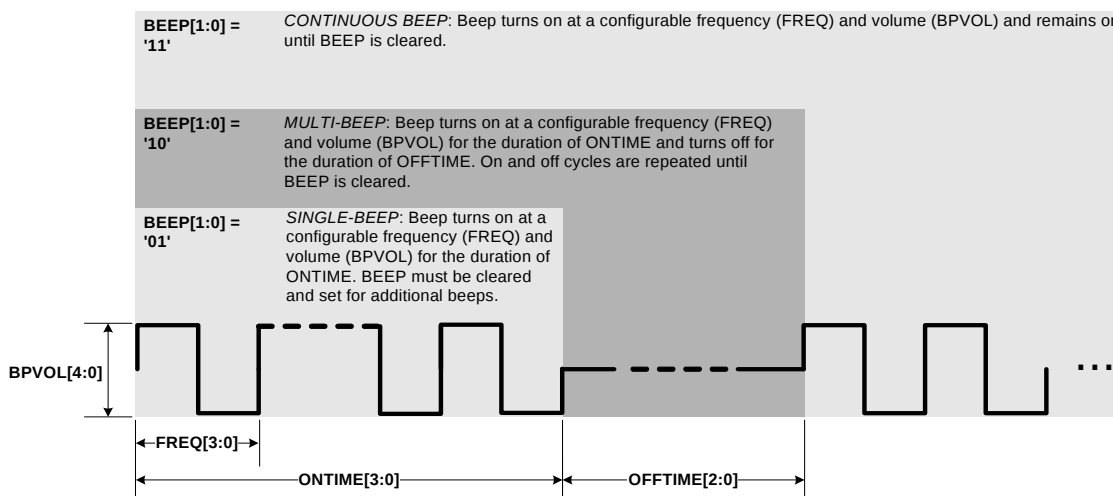
**Figure 5. DSP Engine Signal Flow**

| Referenced Control  | Register Location                        |
|---------------------|------------------------------------------|
| <b>DSP</b>          |                                          |
| DEEMPH .....        | "HP/Speaker De-Emphasis" on page 44      |
| PCMXMUTE .....      | "PCM Channel x Mute" on page 47          |
| PCMXVOL[6:0] .....  | "PCM Channel x Volume" on page 47        |
| INV_PCMA .....      | "Invert PCM Signal Polarity" on page 43  |
| PCMXSWAP[1:0] ..... | "PCM Channel Swap" on page 52            |
| MSTxVOL[7:0] .....  | "Master Volume Control" on page 51       |
| MSTxMUTE .....      | "Master Playback Mute" on page 43        |
| DIGSFT .....        | "Digital Soft Ramp" on page 44           |
| DIGZC .....         | "Digital Zero Cross" on page 45          |
| PLYBCKB=A .....     | "Playback Volume Setting B=A" on page 43 |
| TC_EN .....         | "Tone Control Enable" on page 50         |
| BASS_CF[1:0] .....  | "Bass Corner Frequency" on page 50       |
| TREB_CF[1:0] .....  | "Treble Corner Frequency" on page 50     |
| BASS[3:0] .....     | "Bass Gain" on page 51                   |
| TREB[3:0] .....     | "Treble Gain" on page 50                 |
| LIMIT .....         | "Peak Detect and Limiter" on page 54     |
| LIMSRDIS .....      | "Limiter Soft Ramp Disable" on page 53   |
| LIMZCDIS .....      | "Limiter Zero Cross Disable" on page 54  |
| LMAX[2:0] .....     | "Limiter Maximum Threshold" on page 53   |
| CUSH[2:0] .....     | "Limiter Cushion Threshold" on page 53   |
| LIMARATE[7:0] ..... | "Limiter Attack Rate" on page 55         |
| LIMRRATE[7:0] ..... | "Limiter Release Rate" on page 54        |

### 4.2.1 Beep Generator

The Beep Generator generates audio frequencies across approximately two octave major scales. It offers three modes of operation: Continuous, multiple and single (one-shot) beeps. Sixteen on and eight off times are available.

**Note:** The Beep is generated before the limiter and may affect desired limiting performance. If the limiter function is used, it may be required to set the beep volume sufficiently below the threshold to prevent the peak detect from triggering. Since the master volume control, MSTxVOL[7:0], will affect the beep volume, DAC volume may alternatively be controlled using the PCMxVOL[6:0] bits.



**Figure 6. Beep Configuration Options**

| Referenced Control | Register Location                                                           |
|--------------------|-----------------------------------------------------------------------------|
| MSTxVOL[7:0] ..... | "Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 51 |
| PCMxVOL[6:0] ..... | "PCMx Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)" on page 47           |
| OFFTIME[2:0] ..... | "Beep Off Time" on page 48                                                  |
| ONTIME[3:0] .....  | "Beep On Time" on page 48                                                   |
| FREQ[3:0] .....    | "Beep Frequency" on page 47                                                 |
| BEEP[1:0] .....    | "Beep Configuration" on page 49                                             |
| BEEP MIXDIS .....  | "Beep Mix Disable" on page 49                                               |
| BPVOL[4:0] .....   | "Beep Volume" on page 49                                                    |

### 4.2.2 Limiter

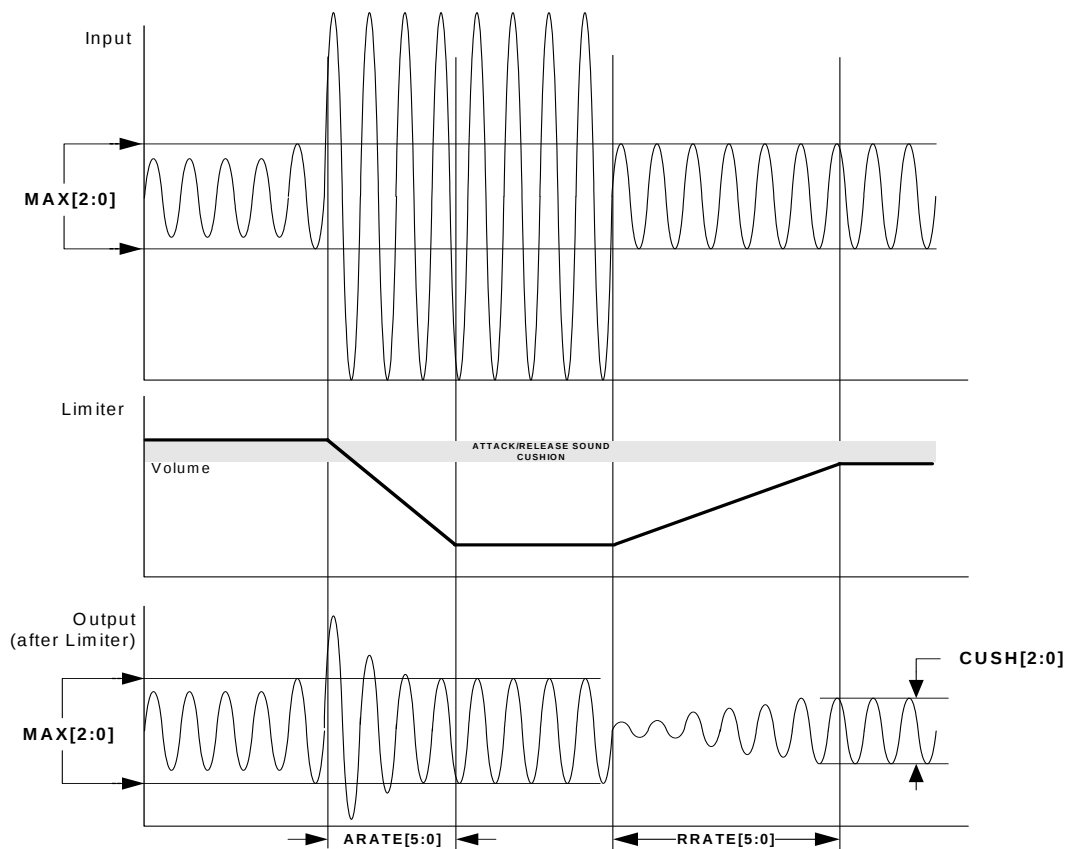
When enabled, the limiter monitors the digital input signal before the DAC and PWM modulators, detects when levels exceed the maximum threshold settings and lowers the master volume at a programmable attack rate below the maximum threshold. When the input signal level falls below the maximum threshold, the AOUT volume returns to its original level set in the Master Volume Control register at a programmable release rate. Attack and release rates are affected by the DAC soft ramp/zero cross settings and sample rate, Fs. Limiter soft ramp and zero cross dependency may be independently enabled/disabled.

#### Notes:

1. *Recommended settings:* Best limiting performance may be realized with the fastest attack and slowest release setting with soft ramp enabled in the control registers. The MIN bits allow the user to set a threshold slightly below the maximum threshold for hysteresis control - this cushions the sound as the limiter attacks and releases.
2. The Limiter maintains the output signal between the CUSH and MAX thresholds. As the digital input signal level changes, the level-controlled output may not always be the same but will always fall within

the thresholds.

| Referenced Control         | Register Location                                                                                          |
|----------------------------|------------------------------------------------------------------------------------------------------------|
| Limiter Controls .....     | "Limiter Control 2, Release Rate (Address 28h)" on page 54, "Limiter Attack Rate (Address 29h)" on page 55 |
| Master Volume Control..... | "Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)" on page 51                                |

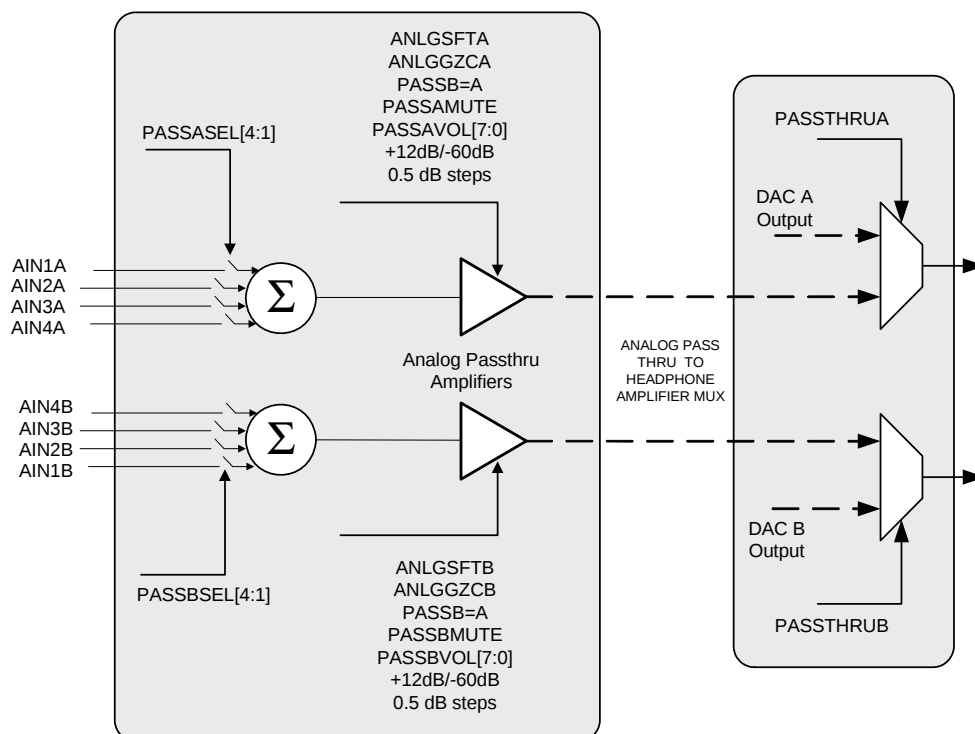


**Figure 7. Peak Detect & Limiter**

### 4.3 Analog Passthrough

The CS43L22 accommodates analog routing of the analog input signal directly to the headphone amplifiers by using the PASSTHRUx mux. This feature is useful in applications that utilize an FM tuner where audio recovered over-the-air must be transmitted to the headphone amplifier directly. This analog passthrough path reduces power consumption and is immune to modulator switching noise that could interfere with some tuners.

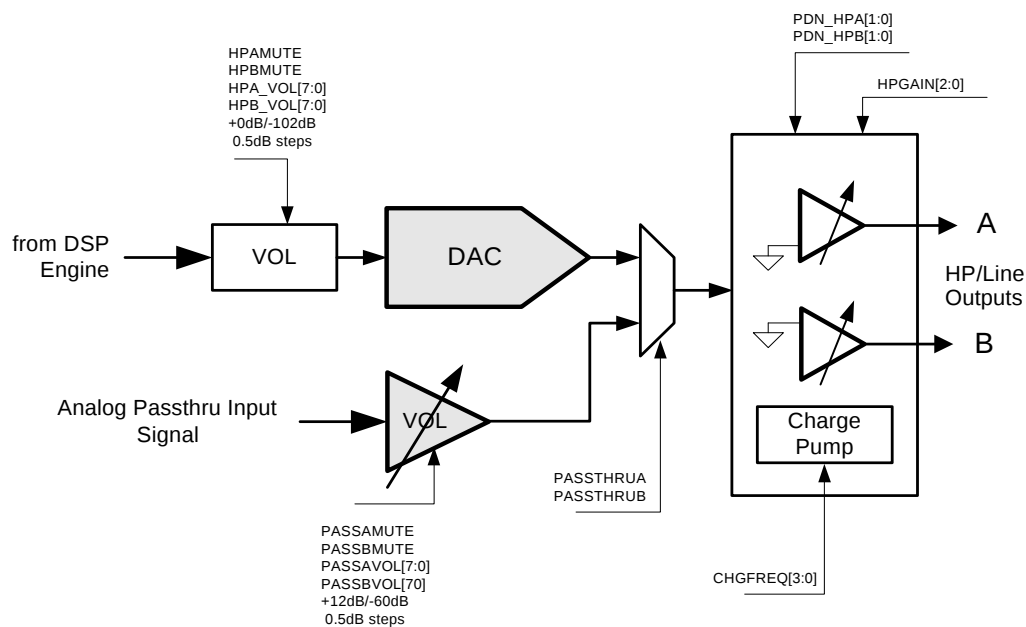
Four analog input channels can be chosen or summed by using the PASSxSEL bits as shown in [Figure 8](#) to provide input to the CS43L22 when in analog passthrough mode. A pair of passthrough amplifiers can be used to mute and apply gain to the input signals.



**Figure 8. Analog Passthrough Signal Flow**

| Referenced Control      | Register Location                                 |
|-------------------------|---------------------------------------------------|
| <b>Analog Front End</b> |                                                   |
| PASSB=A .....           | "Passthrough Channel B=A Gang Control" on page 42 |
| ANLGSFTx .....          | "Ch. x Analog Soft Ramp" on page 42               |
| ANLGZCx .....           | "Ch. x Analog Zero Cross" on page 42              |
| PASSxSEL4,3,2,1 .....   | "Passthrough Input Channel Mapping" on page 42    |
| PASSxMUTE .....         | "Passthrough Mute" on page 44                     |
| PASSxVOL[7:0] .....     | "Passthrough x Volume" on page 46                 |
| PASSTHRUx .....         | "Passthrough Analog" on page 44                   |

## 4.4 Analog Outputs

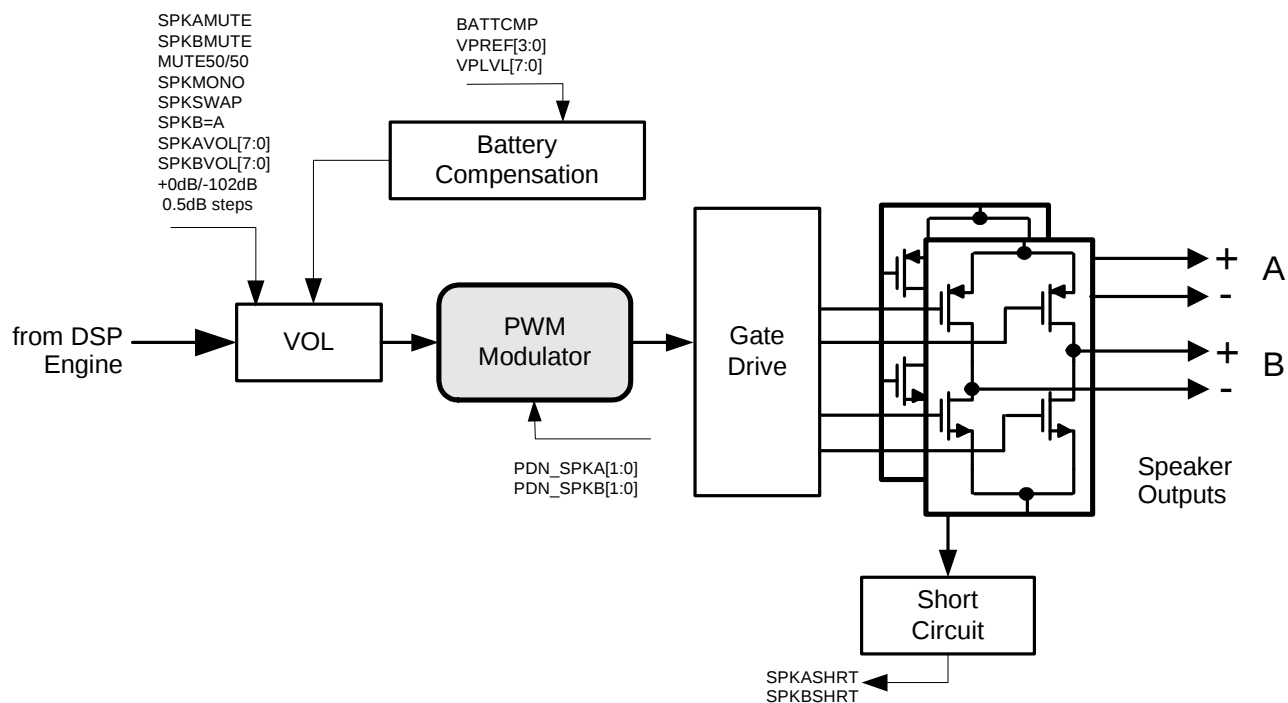


**Figure 9. Analog Outputs**

| Referenced Control   | Register Location                     |
|----------------------|---------------------------------------|
| <b>Analog Output</b> |                                       |
| HPxMUTE .....        | "Headphone Mute" on page 45           |
| HPxVOL[7:0] .....    | "Headphone Volume Control" on page 51 |
| PDN_HP[1:0] .....    | "Headphone Power Control" on page 38  |
| HPGAIN[2:0] .....    | "Headphone Analog Gain" on page 43    |
| PASSTHRUx .....      | "Passthrough Analog" on page 44       |
| PASSxMUTE .....      | "Passthrough Mute" on page 44         |
| PASSxVOL[7:0] .....  | "Passthrough x Volume" on page 46     |
| CHGFREQ .....        | "Charge Pump Frequency" on page 58    |

## 4.5 PWM Outputs

**Note:** The PWM speaker amplifiers should not be used in the 384x MCLK modes (18.4320 and 16.9344 MHz).



**Figure 10. PWM Output Stage**

| Referenced Control  | Register Location                                    |
|---------------------|------------------------------------------------------|
| <b>PWM Control</b>  |                                                      |
| SPKxMUTE .....      | "Speaker Mute" on page 45                            |
| MUTE50/50 .....     | "Speaker Mute 50/50 Control" on page 46              |
| SPKMONO .....       | "Speaker MONO Control" on page 46                    |
| SPKxVOL[7:0] .....  | "Speaker Volume Control" on page 52                  |
| SPKSWAP .....       | "Speaker Channel Swap" on page 45                    |
| SPKB=A .....        | "Speaker Volume Setting B=A" on page 45              |
| BATTCPMP .....      | "Battery Compensation" on page 56                    |
| VPREF[3:0] .....    | "VP Reference" on page 57                            |
| VPLVL[7:0] .....    | "VP Voltage Level (Read Only)" on page 57            |
| PDN_SPKx[1:0] ..... | "Speaker Power Control" on page 38                   |
| SPKxSHRT .....      | "Speaker Current Load Status (Read Only)" on page 57 |

### 4.5.1 Mono Speaker Output Configuration

The CS43L22 accommodates a stereo as well as a mono speaker output configuration. In mono mode the output drivers of each channel are connected in parallel to deliver maximum power to a 4 ohm speaker. Refer to the table below for pin mapping in mono configuration.

| Pin | Speaker Output |           |           |           |
|-----|----------------|-----------|-----------|-----------|
|     | SPKMONO=0      |           | SPKMONO=1 |           |
|     | SPKSWAP=0      | SPKSWAP=1 | SPKSWAP=0 | SPKSWAP=1 |
| 4   | SPKOUTA+       | SPKOUTB+  | SPKOUTA+  | SPKOUTB+  |
| 6   | SPKOUTA-       | SPKOUTB-  | SPKOUTA+  | SPKOUTB+  |
| 7   | SPKOUTB+       | SPKOUTA+  | SPKOUTA-  | SPKOUTB-  |
| 9   | SPKOUTB-       | SPKOUTA-  | SPKOUTA-  | SPKOUTB-  |

| Referenced Control | Register Location                 |
|--------------------|-----------------------------------|
| SPKMONO.....       | "Speaker MONO Control" on page 46 |
| SPKSWAP.....       | "Speaker Channel Swap" on page 45 |

### 4.5.2 VP Battery Compensation

The CS43L22 provides the option to maintain a desired power output level, independent of the VP supply. When enabled, this feature works by monitoring the voltage on the VP supply and *reducing the attenuation* on the speaker outputs when VP voltage levels fall.

**Note:** The internal ADC that monitors the VP supply operates from the VA supply. Calculations are based on typical VA levels of 1.8 V and 2.5 V using the VPREF bits.

#### 4.5.2.1 Maintaining a Desired Output Level

Using SPKxVOL, the speaker output level must first be attenuated by the decibel equivalent of the expected VP supply range (MAX relative to MIN). The CS43L22 then gradually *reduces* the attenuation as the VP supply drops from its maximum level, maintaining a nearly constant power output.

**Compensation Example 1** (VP Battery supply ranges from 4.5 V to 3.0 V)

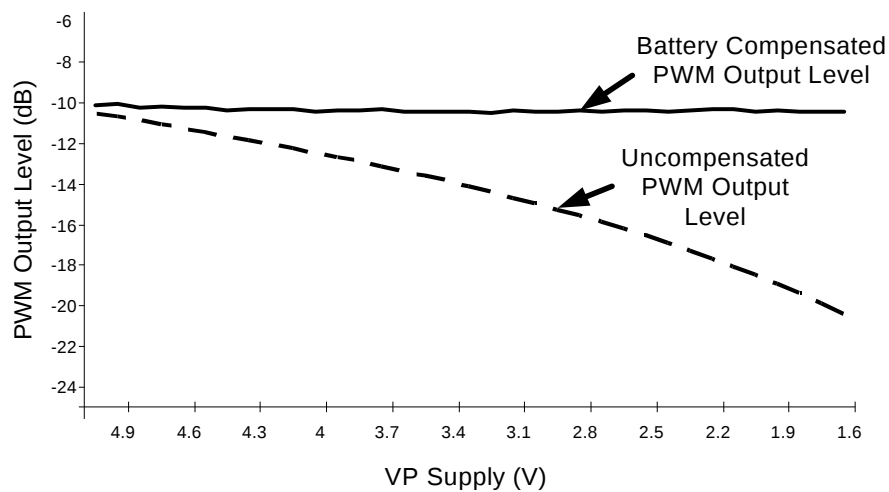
1. Set speaker attenuation (SPKxVOL) to -3.5 dB. *The VP supply changes ~3.5 dB.*
2. Set the reference VP supply (VPREF) to 4.5 V.
3. Enable battery compensation (BATTCMP).

*The CS43L22 automatically adjusts the output level as the battery discharges.*

**Compensation Example 2** (VP Battery supply ranges from 5.0 V to 1.6 V)

1. Set speaker attenuation (SPKxVOL) to -10 dB. *The VP supply changes ~9.9 dB.*
2. Set the reference VP supply (VPREF) to 5.0 V.
3. Enable battery compensation (BATTCMP).

*The CS43L22 automatically adjusts the output level as the battery discharges. Refer to [Figure 11 on page 28](#). In this example, the VP supply changes over a wide range, illustrating the accuracy of the CS43L22's battery compensation.*



**Figure 11. Battery Compensation**

| Referenced Control | Register Location                                   |
|--------------------|-----------------------------------------------------|
| VPREF .....        | <a href="#">"VP Reference" on page 57</a>           |
| SPKxVOL .....      | <a href="#">"Speaker Volume Control" on page 52</a> |

## 4.6 Serial Port Clocking

The CS43L22 serial audio interface port operates either as a slave or master, determined by the  $M/\bar{S}$  bit. It accepts externally generated clocks in Slave Mode and will generate synchronous clocks derived from an input master clock (MCLK) in Master Mode. Refer to the tables below for the required setting in register 05h and 06h associated with a given MCLK and sample rate.

| Referenced Control | Register Location                              |
|--------------------|------------------------------------------------|
| $M/\bar{S}$ .....  | "Master/Slave Mode" on page 40                 |
| Register 05h.....  | "Clocking Control (Address 05h)" on page 38    |
| Register 06h.....  | "Interface Control 1 (Address 06h)" on page 40 |

| MCLK (MHz)                | Sample Rate, Fs (kHz) | SPEED[1:0] (AUTO='0'b) | 32kGROUP | VIDEOCLK | RATIO[1:0] | MCLKDIV2 |
|---------------------------|-----------------------|------------------------|----------|----------|------------|----------|
| 12.2880                   | 8.0000                | 11                     | 1        | 0        | 00         | 0        |
|                           | 12.0000               | 11                     | 0        | 0        | 00         | 0        |
|                           | 16.0000               | 10                     | 1        | 0        | 00         | 0        |
|                           | 24.0000               | 10                     | 0        | 0        | 00         | 0        |
|                           | 32.0000               | 01                     | 1        | 0        | 00         | 0        |
|                           | 48.0000               | 01                     | 0        | 0        | 00         | 0        |
| 11.2896                   | 96.0000               | 00                     | 0        | 0        | 00         | 0        |
|                           | 11.0250               | 11                     | 0        | 0        | 00         | 0        |
|                           | 22.0500               | 10                     | 0        | 0        | 00         | 0        |
|                           | 44.1000               | 01                     | 0        | 0        | 00         | 0        |
| 18.4320 (Slave Mode ONLY) | 88.2000               | 00                     | 0        | 0        | 00         | 0        |
|                           | 8.0000                | 11                     | 1        | 0        | 00         | 0        |
|                           | 12.0000               | 11                     | 0        | 0        | 00         | 0        |
|                           | 16.0000               | 10                     | 1        | 0        | 00         | 0        |
|                           | 24.0000               | 10                     | 0        | 0        | 00         | 0        |
|                           | 32.0000               | 01                     | 1        | 0        | 00         | 0        |
| 16.9344 (Slave Mode ONLY) | 48.0000               | 01                     | 0        | 0        | 00         | 0        |
|                           | 96.0000               | 00                     | 0        | 0        | 00         | 0        |
|                           | *8.0182...            | 11                     | 0        | 0        | 10         | 0        |
|                           | 11.0250               | 11                     | 0        | 0        | 00         | 0        |
|                           | 22.0500               | 10                     | 0        | 0        | 00         | 0        |
| 12.0000                   | 44.1000               | 01                     | 0        | 0        | 00         | 0        |
|                           | 88.2000               | 00                     | 0        | 0        | 00         | 0        |
|                           | 8.0000                | 11                     | 1        | 0        | 01         | 0        |
|                           | *11.0294...           | 11                     | 0        | 0        | 11         | 0        |
|                           | 12.0000               | 11                     | 0        | 0        | 01         | 0        |
|                           | 16.0000               | 10                     | 1        | 0        | 01         | 0        |
|                           | *22.0588...           | 10                     | 0        | 0        | 11         | 0        |
|                           | 24.0000               | 10                     | 0        | 0        | 01         | 0        |
|                           | 32.0000               | 01                     | 1        | 0        | 01         | 0        |
|                           | *44.1176...           | 01                     | 0        | 0        | 11         | 0        |
|                           | 48.0000               | 01                     | 0        | 0        | 01         | 0        |
| 24.0000                   | *88.2353...           | 00                     | 0        | 0        | 11         | 0        |
|                           | 96.0000               | 00                     | 0        | 0        | 01         | 0        |
|                           | 8.0000                | 11                     | 1        | 0        | 01         | 1        |
|                           | *11.0294...           | 11                     | 0        | 0        | 11         | 1        |
|                           | 12.0000               | 11                     | 0        | 0        | 01         | 1        |
|                           | 16.0000               | 10                     | 1        | 0        | 01         | 1        |
|                           | *22.0588...           | 10                     | 0        | 0        | 11         | 1        |
|                           | 24.0000               | 10                     | 0        | 0        | 01         | 1        |
|                           | 32.0000               | 01                     | 1        | 0        | 01         | 1        |
|                           | *44.1176...           | 01                     | 0        | 0        | 11         | 1        |
|                           | 48.0000               | 01                     | 0        | 0        | 01         | 1        |
|                           | *88.2353...           | 00                     | 0        | 0        | 11         | 1        |
|                           | 96.0000               | 00                     | 0        | 0        | 01         | 1        |

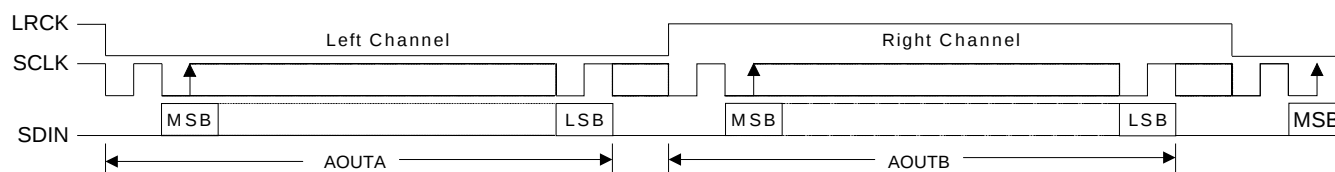
| MCLK (MHz) | Sample Rate, Fs (kHz) | SPEED[1:0] (AUTO='0'b) | 32kGROUP | VIDEOCLK | RATIO[1:0] | MCLKDIV2 |
|------------|-----------------------|------------------------|----------|----------|------------|----------|
| 27.0000    | 8.0000                | 11                     | 1        | 1        | 01         | 0        |
|            | 12.0000               | 11                     | 0        | 1        | 01         | 0        |
|            | 24.0000               | 10                     | 0        | 1        | 01         | 0        |
|            | 32.0000               | 01                     | 1        | 1        | 01         | 0        |
|            | *44.1176...           | 01                     | 0        | 1        | 11         | 0        |
|            | 48.0000               | 01                     | 0        | 1        | 01         | 0        |
|            | *11.0294...           | 11                     | 0        | 1        | 11         | 0        |
|            | *22.0588...           | 10                     | 0        | 1        | 11         | 0        |
|            | 16.0000               | 10                     | 1        | 1        | 01         | 0        |

**Note:** \*The marked sample rate values are not exact representations of the actual frame clock frequency. They have been truncated to 4 decimal places. The exact value can be calculated by dividing the MCLK being used by the desired MCLK/LRCK ratio.

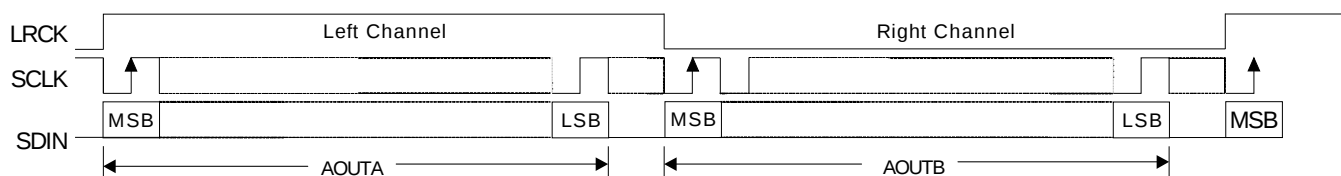
**Table 1. Serial Port Clocking**

## 4.7 Digital Interface Formats

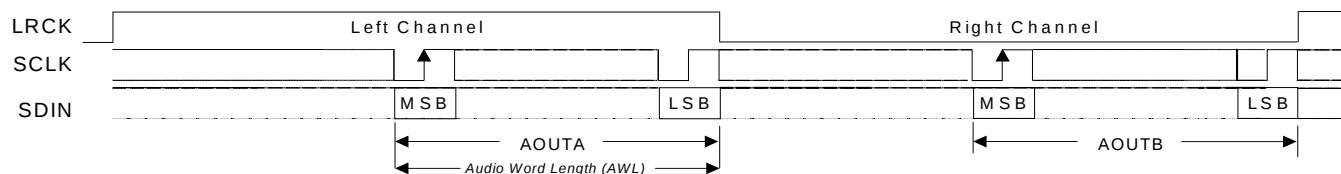
The serial port operates in standard I<sup>2</sup>S, Left-Justified, Right-Justified, or DSP Mode digital interface formats with varying bit depths from 16 to 24. Data is clocked into the DAC on the rising edge of SCLK.



**Figure 12. I<sup>2</sup>S Format**



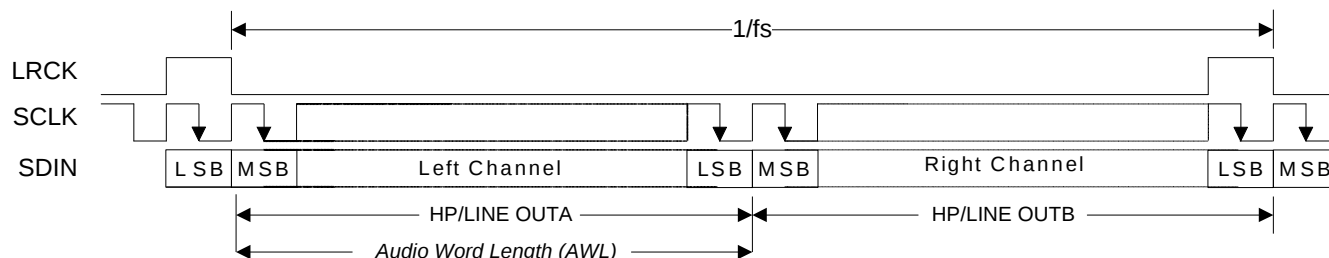
**Figure 13. Left-Justified Format**



**Figure 14. Right-Justified Format**

### 4.7.1 DSP Mode

In DSP Mode, the LRCK acts as a frame sync for 2 data-packed words (left and right channel) input on SDIN. The MSB is input on the first SCLK rising edge after the frame sync rising edge. The right channel immediately follows the left channel.



**Figure 15. DSP Mode Format)**

## 4.8 Initialization

The CS43L22 enters a Power-Down state upon initial power-up. The interpolation and decimation filters, delta-sigma and PWM modulators and control port registers are reset. The internal voltage reference, and switched-capacitor low-pass filters are powered down.

The device will remain in the Power-Down state until the  $\overline{\text{RESET}}$  pin is brought high. The control port is accessible once  $\overline{\text{RESET}}$  is high and the desired register settings can be loaded per the interface descriptions in the [“Register Description” on page 37](#).

Once MCLK is valid, the quiescent voltage, VQ, and the internal voltage reference, FILT+, will begin powering up to normal operation. The charge pump slowly powers up and charges the capacitors. Power is then applied to the headphone amplifiers and switched-capacitor filters, and the analog/digital outputs enter a muted state. Once LRCK is valid, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio and normal operation begins.

## 4.9 Recommended Power-Up Sequence

1. Hold  $\overline{\text{RESET}}$  low until the power supplies are stable.
2. Bring  $\overline{\text{RESET}}$  high.
3. The default state of the “Power Ctl. 1” register (0x02) is 0x01. Load the desired register settings while keeping the “Power Ctl 1” register set to 0x01.
4. Load the required initialization settings listed in [Section 4.11](#).
5. Apply MCLK at the appropriate frequency, as discussed in [Section 4.6](#). SCLK may be applied or set to master at any time; LRCK may only be applied or set to master while the PDN bit is set to 1.
6. Set the “Power Ctl 1” register (0x02) to 0x9E.
7. Bring  $\overline{\text{RESET}}$  low if the analog or digital supplies drop below the recommended operating condition to prevent power glitch related issues.

## 4.10 Recommended Power-Down Sequence

To minimize audible pops when turning off or placing the DAC in standby,

1. Mute the DAC’s and PWM outputs.
2. Disable soft ramp and zero cross volume transitions.
3. Set the “Power Ctl 1” register (0x02) to 0x9F.

4. Wait at least 100  $\mu$ s.  
The device will be fully powered down after this 100  $\mu$ s delay. Prior to the removal of the master clock (MCLK), this delay of at least 100  $\mu$ s must be implemented after step 3 to avoid premature disruption of the DAC's power down sequence.

A disruption in the device's power down sequence (i.e. removing the MCLK signal before this 100  $\mu$ s delay) has consequences on both the headphone and PWM speaker amplifiers: The charge pump may stop abruptly, causing the headphone amplifiers to drive the outputs up to the +VHP supply. Also, the last state of each '+' and '-' PWM output terminal before the premature removal of MCLK could randomly be held at either VP or AGND. When this event occurs, it is possible for each PWM terminal to output opposing potentials, creating a DC source into the speaker voice coil.

The disruption of the device's power down sequence may also cause clicks and pops on the output of the DAC's as the modulator holds the last output level before the MCLK signal was removed.

5. MCLK may be removed at this time.
6. To achieve the lowest operating quiescent current, bring  $\overline{\text{RESET}}$  low. All control port registers will be reset to their default state.

#### **4.11 Required Initialization Settings**

Various sections in the device must be adjusted by implementing the initialization settings shown below after power-up sequence step 3. All performance and power consumption measurements were taken with the following settings:

1. Write 0x99 to register 0x00.
2. Write 0x80 to register 0x47.
3. Write '1'b to bit 7 in register 0x32.
4. Write '0'b to bit 7 in register 0x32.
5. Write 0x00 to register 0x00.

## 5. CONTROL PORT OPERATION

The control port is used to access the registers allowing the CS43L22 to be configured for the desired operational modes and formats. The operation of the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

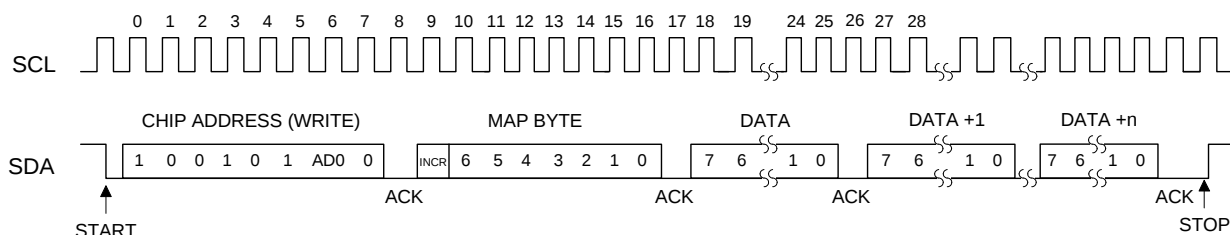
The control port operates using an I<sup>2</sup>C interface with the CS43L22 acting as a slave device.

### 5.1 I<sup>2</sup>C Control

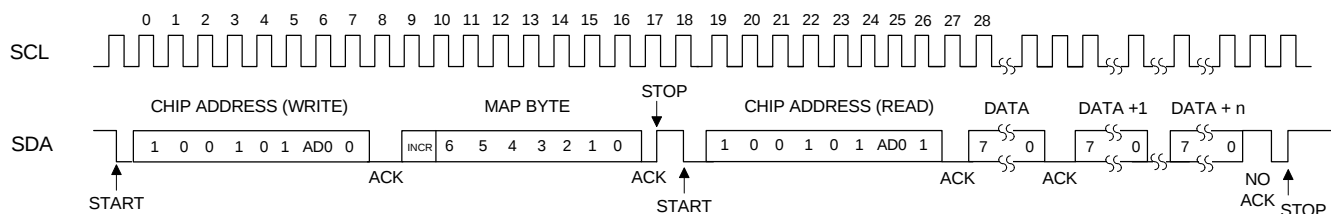
SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 pin sets the LSB of the chip address; '0' when connected to DGND, '1' when connected to VL. This pin may be driven by a host controller or directly connected to VL or DGND. The AD0 pin state is sensed and the LSB of the chip address is set upon the release of the RESET signal (a low-to-high transition).

The signal timings for a read and write cycle are shown in Figure 16 and Figure 17. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is defined as a rising transition of SDA while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS43L22 after a Start condition consists of a 7-bit chip address field and a R/W bit (high for a read, low for a write).

The upper 6 bits of the address field are fixed at 100101. To communicate with the CS43L22, the chip address field, which is the first byte sent to the CS43L22, should match 100101 followed by the setting of the AD0 pin. The eighth bit of the address is the R/W bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP), which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto-increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS43L22 after each input byte is read and is input to the CS43L22 from the microcontroller after each transmitted byte.



**Figure 16. Control Port Timing, I<sup>2</sup>C Write**



**Figure 17. Control Port Timing, I<sup>2</sup>C Read**

Since the read operation cannot set the MAP, an aborted write operation is used as a preamble. As shown in Figure 17, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.  
Send 10010100 (chip address & write operation).  
Receive acknowledge bit.  
Send MAP byte, auto-increment off.  
Receive acknowledge bit.  
Send stop condition, aborting write.  
Send start condition.  
Send 10010101 (chip address & read operation).  
Receive acknowledge bit.  
Receive byte, contents of selected register.  
Send acknowledge bit.  
Send stop condition.

Setting the auto-increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

### **5.1.1 Memory Address Pointer (MAP)**

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudo code above for implementation details.

#### **5.1.1.1 Map Increment (INCR)**

The device has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I<sup>2</sup>C writes or reads. If INCR is set to 1, MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

## 6. REGISTER QUICK REFERENCE

Default values are shown below the bit names. Unless otherwise specified, all “Reserved” bits must maintain their default value.

| Adr.                        | Function                  | 7              | 6              | 5                | 4              | 3              | 2              | 1              | 0              |
|-----------------------------|---------------------------|----------------|----------------|------------------|----------------|----------------|----------------|----------------|----------------|
| 01h<br><a href="#">p 37</a> | ID                        | CHIPID4<br>1   | CHIPID3<br>1   | CHIPID2<br>1     | CHIPID1<br>0   | CHIPID0<br>0   | REVID2<br>x    | REVID1<br>x    | REVID0<br>x    |
| 02h<br><a href="#">p 37</a> | Power Ctl 1               | PDN7<br>0      | PDN6<br>0      | PDN5<br>0        | PDN4<br>0      | PDN3<br>0      | PDN2<br>0      | PDN1<br>0      | PDN0<br>1      |
| 03h                         | Reserved                  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  |
| 04h<br><a href="#">p 38</a> | Power Ctl 2               | PDN_HPB1<br>0  | PDN_HPB0<br>0  | PDN_HPA1<br>0    | PDN_HPA0<br>0  | PDN_SPKB1<br>0 | PDN_SPKB0<br>1 | PDN_SPKA1<br>0 | PDN_SPKA0<br>1 |
| 05h<br><a href="#">p 38</a> | Clocking Ctl              | AUTO<br>1      | SPEED1<br>0    | SPEED0<br>1      | 32kGROUP<br>0  | VIDEOCLK<br>0  | RATIO1<br>0    | RATIO0<br>0    | MCLKDIV2<br>0  |
| 06h<br><a href="#">p 40</a> | Interface Ctl 1           | M/S<br>0       | INV_SCLK<br>0  | Reserved<br>0    | DSP<br>0       | DACDIF1<br>0   | DACDIF0<br>0   | AWL1<br>0      | AWL0<br>0      |
| 07h<br><a href="#">p 41</a> | Interface Ctl 2           | Reserved<br>0  | SCLK=MCLK<br>0 | Reserved<br>0    | Reserved<br>0  | INV_SWCH<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 08h<br><a href="#">p 42</a> | Passthrough A Select      | Reserved<br>1  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | PASSASEL4<br>0 | PASSASEL3<br>0 | PASSASEL2<br>0 | PASSASEL1<br>1 |
| 09h<br><a href="#">p 42</a> | Passthrough B Select      | Reserved<br>1  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | PASSBSEL4<br>0 | PASSBSEL3<br>0 | PASSBSEL2<br>0 | PASSBSEL1<br>1 |
| 0Ah<br><a href="#">p 42</a> | Analog ZC and SR Settings | Reserved<br>1  | Reserved<br>0  | Reserved<br>1    | Reserved<br>0  | ANLGSFTB<br>0  | ANLGZCB<br>1   | ANLGSFTA<br>0  | ANLGZCA<br>1   |
| 0Bh                         | Reserved                  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 0Ch<br><a href="#">p 42</a> | Passthrough Gang Control  | PASSB=A<br>0   | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 0Dh<br><a href="#">p 43</a> | Playback Ctl 1            | HPGAIN2<br>0   | HPGAIN1<br>1   | HPGAIN0<br>1     | PLYBCKB=A<br>0 | INV_PCMB<br>0  | INV_PCMA<br>0  | MSTBMUTE<br>0  | MSTAMUTE<br>0  |
| 0Eh<br><a href="#">p 44</a> | Misc. Ctl                 | PASSTHRUB<br>0 | PASSTHRUA<br>0 | PASSBMUTE<br>0   | PASSAMUTE<br>0 | FREEZE<br>0    | DEEMPH<br>0    | DIGSFT<br>1    | DIGZC<br>0     |
| 0Fh<br><a href="#">p 45</a> | Playback Ctl 2            | HPBMUTE<br>0   | HPAMUTE<br>0   | SPKBMUTE<br>0    | SPKAMUTE<br>0  | SPKB=A<br>0    | SPKSWAP<br>0   | SPKMONO<br>0   | MUTE50/50<br>0 |
| 10h-13h                     | Reserved                  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 14h<br><a href="#">p 46</a> | Passthrough A Vol         | PASSAVOL7<br>0 | PASSAVOL6<br>0 | PASSAVOL5<br>0   | PASSAVOL4<br>0 | PASSAVOL3<br>0 | PASSAVOL2<br>0 | PASSAVOL1<br>0 | PASSAVOL0<br>0 |
| 15h<br><a href="#">p 46</a> | Passthrough B Vol         | PASSBVOL7<br>0 | PASSBVOL6<br>0 | PASSBVOL5<br>0   | PASSBVOL4<br>0 | PASSBVOL3<br>0 | PASSBVOL2<br>0 | PASSBVOL1<br>0 | PASSBVOL0<br>0 |
| 16h-17h                     | Reserved                  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 18h-19h                     | Reserved                  | Reserved<br>1  | Reserved<br>0  | Reserved<br>0    | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 1Ah<br><a href="#">p 47</a> | PCMA Vol                  | PCMAMUTE<br>0  | PCMAVOL6<br>0  | PCMAVOL5<br>0    | PCMAVOL4<br>0  | PCMAVOL3<br>0  | PCMAVOL2<br>0  | PCMAVOL1<br>0  | PCMAVOL0<br>0  |
| 1Bh<br><a href="#">p 47</a> | PCMB Vol                  | PCMBMUTE<br>0  | PCMBVOL6<br>0  | PCMBVOL5<br>0    | PCMBVOL4<br>0  | PCMBVOL3<br>0  | PCMBVOL2<br>0  | PCMBVOL1<br>0  | PCMBVOL0<br>0  |
| 1Ch<br><a href="#">p 47</a> | BEEP Freq, On Time        | FREQ3<br>0     | FREQ2<br>0     | FREQ1<br>0       | FREQ0<br>0     | ONTIME3<br>0   | ONTIME2<br>0   | ONTIME1<br>0   | ONTIME0<br>0   |
| 1Dh<br><a href="#">p 48</a> | BEEP Vol, Off Time        | OFFTIME2<br>0  | OFFTIME1<br>0  | OFFTIME0<br>0    | BPVOL4<br>0    | BPVOL3<br>0    | BPVOL2<br>0    | BPVOL1<br>0    | BPVOL0<br>0    |
| 1Eh<br><a href="#">p 49</a> | BEEP, Tone Cfg.           | BEEP1<br>0     | BEEP0<br>0     | BEEP MIXDIS<br>0 | TREB_CF1<br>0  | TREB_CF0<br>0  | BASS_CF1<br>0  | BASS_CF0<br>0  | TC_EN<br>0     |
| 1Fh<br><a href="#">p 50</a> | Tone Ctl                  | TREB3<br>1     | TREB2<br>0     | TREB1<br>0       | TREB0<br>0     | BASS3<br>1     | BASS2<br>0     | BASS1<br>0     | BASS0<br>0     |

| Adr.                        | Function                  | 7             | 6              | 5              | 4              | 3              | 2              | 1              | 0              |
|-----------------------------|---------------------------|---------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 20h<br><a href="#">p 51</a> | Master A Vol              | MSTAVOL7<br>0 | MSTAVOL6<br>0  | MSTAVOL5<br>0  | MSTAVOL4<br>0  | MSTAVOL3<br>0  | MSTAVOL2<br>0  | MSTAVOL1<br>0  | MSTAVOL0<br>0  |
| 21h<br><a href="#">p 51</a> | Master B Vol              | MSTBVOL7<br>0 | MSTBVOL6<br>0  | MSTBVOL5<br>0  | MSTBVOL4<br>0  | MSTBVOL3<br>0  | MSTBVOL2<br>0  | MSTBVOL1<br>0  | MSTBVOL0<br>0  |
| 22h<br><a href="#">p 51</a> | Headphone A Volume        | HPAVOL7<br>0  | HPAVOL6<br>0   | HPAVOL5<br>0   | HPAVOL4<br>0   | HPAVOL3<br>0   | HPAVOL2<br>0   | HPAVOL1<br>0   | HPAVOL0<br>0   |
| 23h<br><a href="#">p 51</a> | Headphone B Volume        | HPBVOL7<br>0  | HPBVOL6<br>0   | HPBVOL5<br>0   | HPBVOL4<br>0   | HPBVOL3<br>0   | HPBVOL2<br>0   | HPBVOL1<br>0   | HPBVOL0<br>0   |
| 24h<br><a href="#">p 52</a> | Speaker A Volume          | SPKAVOL7<br>0 | SPKAVOL6<br>0  | SPKAVOL5<br>0  | SPKAVOL4<br>0  | SPKAVOL3<br>0  | SPKAVOL2<br>0  | SPKAVOL1<br>0  | SPKAVOL0<br>0  |
| 25h<br><a href="#">p 52</a> | Speaker B Volume          | SPKBVOL7<br>0 | SPKBVOL6<br>0  | SPKBVOL5<br>0  | SPKBVOL4<br>0  | SPKBVOL3<br>0  | SPKBVOL2<br>0  | SPKBVOL1<br>0  | SPKBVOL0<br>0  |
| 26h<br><a href="#">p 52</a> | Channel Mixer & Swap      | PCMASWP1<br>0 | PCMASWP0<br>0  | PCMBSWP1<br>0  | PCMBSWP0<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 27h<br><a href="#">p 53</a> | Limit Ctl 1, Thresholds   | LMAX2<br>0    | LMAX1<br>0     | LMAX0<br>0     | CUSH2<br>0     | CUSH1<br>0     | CUSH0<br>0     | LIMSRDIS<br>0  | LIMZCDIS<br>0  |
| 28h<br><a href="#">p 54</a> | Limit Ctl 2, Release Rate | LIMIT<br>0    | LIMIT_ALL<br>1 | LIMRRATE5<br>1 | LIMRRATE4<br>1 | LIMRRATE3<br>1 | LIMRRATE2<br>1 | LIMRRATE1<br>1 | LIMRRATE0<br>1 |
| 29h<br><a href="#">p 55</a> | Limiter Attack Rate       | Reserved<br>0 | Reserved<br>0  | LIMARATE5<br>0 | LIMARATE4<br>0 | LIMARATE3<br>0 | LIMARATE2<br>0 | LIMARATE1<br>0 | LIMARATE0<br>0 |
| 2Ah                         | Reserved                  | Reserved<br>0 | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 2Bh                         | Reserved                  | Reserved<br>0 | Reserved<br>0  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  |
| 2Ch-2Dh                     | Reserved                  | Reserved<br>0 | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 2Eh<br><a href="#">p 55</a> | Overflow & Clock Status   | Reserved<br>0 | SPCLKERR<br>0  | DSPBOVFL<br>0  | DSPAOVFL<br>0  | PCMAOVFL<br>0  | PCMBOVFL<br>0  | Reserved<br>0  | Reserved<br>0  |
| 2Fh<br><a href="#">p 56</a> | Battery Compensation      | BATTCMP<br>0  | VPMONITOR<br>0 | Reserved<br>0  | Reserved<br>0  | VPREF3<br>0    | VPREF2<br>0    | VPREF1<br>0    | VPREF0<br>0    |
| 30h<br><a href="#">p 57</a> | VP Battery Level          | VPLVL7<br>0   | VPLVL6<br>0    | VPLVL5<br>0    | VPLVL4<br>0    | VPLVL3<br>0    | VPLVL2<br>0    | VPLVL1<br>0    | VPLVL0<br>0    |
| 31h<br><a href="#">p 57</a> | Speaker Status            | Reserved<br>0 | Reserved<br>0  | SPKASHRT<br>0  | SPKBSHRT<br>0  | SPKR/HP<br>0   | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 32h                         | Reserved                  | Reserved<br>0 | Reserved<br>0  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>0  | Reserved<br>1  | Reserved<br>1  |
| 33h                         | Reserved                  | Reserved<br>0 | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  | Reserved<br>0  |
| 34h<br><a href="#">p 58</a> | Charge Pump Frequency     | CHGFREQ3<br>0 | CHGFREQ2<br>1  | CHGFREQ1<br>0  | CHGFREQ0<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  | Reserved<br>1  |

## 7. REGISTER DESCRIPTION

All registers are read/write except for the chip I.D. and Revision Register and Interrupt Status Register which are read only. See the following bit definition tables for bit assignment information. The default state of each bit after a power-up sequence or reset is shown as shaded in the table. Unless otherwise specified, all “Reserved” bits must maintain their default value.

### 7.1 Chip I.D. and Revision Register (Address 01h) (Read Only)

| 7       | 6       | 5       | 4       | 3       | 2      | 1      | 0      |
|---------|---------|---------|---------|---------|--------|--------|--------|
| CHIPID4 | CHIPID3 | CHIPID2 | CHIPID1 | CHIPID0 | REVID2 | REVID1 | REVID0 |

#### 7.1.1 Chip I.D. (Read Only)

I.D. code for the CS43L22.

| CHIPID[4:0] | Device  |
|-------------|---------|
| 11100       | CS43L22 |

#### 7.1.2 Chip Revision (Read Only)

CS43L22 revision level.

| REVID[2:0] | Revision Level |
|------------|----------------|
| 000        | A0             |
| 001        | A1             |
| 010        | B0             |
| 011        | B1             |

### 7.2 Power Control 1 (Address 02h)

| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|------|------|------|------|------|------|------|------|
| PDN7 | PDN6 | PDN5 | PDN4 | PDN3 | PDN2 | PDN1 | PDN0 |

#### 7.2.1 Power Down

Configures the power state of the CS43L22.

| PDN[7:0]  | Status                                   |
|-----------|------------------------------------------|
| 0000 0001 | Powered Down - same as setting 1001 1111 |
| 1001 1110 | Powered Up                               |
| 1001 1111 | Powered Down - same as setting 0000 0001 |

**Note:**

1. All states of PDN[7:0] not shown in the table are reserved.

## 7.3 Power Control 2 (Address 04h)

| 7         | 6         | 5         | 4         | 3          | 2          | 1          | 0          |
|-----------|-----------|-----------|-----------|------------|------------|------------|------------|
| PDN_HP B1 | PDN_HP B0 | PDN_HP A1 | PDN_HP A0 | PDN_SPK B1 | PDN_SPK B0 | PDN_SPK A1 | PDN_SPK A0 |

### 7.3.1 Headphone Power Control

Configures how the SPK/HP\_SW pin, 6, controls the power for the headphone amplifier.

| PDN_HP x[1:0] | Headphone Status                                                                                                        |
|---------------|-------------------------------------------------------------------------------------------------------------------------|
| 00            | Headphone channel is ON when the SPK/HP_SW pin, 6, is LO.<br>Headphone channel is OFF when the SPK/HP_SW pin, 6, is HI. |
| 01            | Headphone channel is ON when the SPK/HP_SW pin, 6, is HI.<br>Headphone channel is OFF when the SPK/HP_SW pin, 6, is LO. |
| 10            | Headphone channel is always ON.                                                                                         |
| 11            | Headphone channel is always OFF.                                                                                        |

### 7.3.2 Speaker Power Control

Configures how the SPK/HP\_SW pin, 6, controls the power for the speaker amplifier.

| PDN_SPK x[1:0] | Speaker Status                                                                                                      |
|----------------|---------------------------------------------------------------------------------------------------------------------|
| 00             | Speaker channel is ON when the SPK/HP_SW pin, 6, is LO.<br>Speaker channel is OFF when the SPK/HP_SW pin, 6, is HI. |
| 01             | Speaker channel is ON when the SPK/HP_SW pin, 6, is HI.<br>Speaker channel is OFF when the SPK/HP_SW pin, 6, is LO. |
| 10             | Speaker channel is always ON.                                                                                       |
| 11             | Speaker channel is always OFF.                                                                                      |

## 7.4 Clocking Control (Address 05h)

| 7    | 6      | 5      | 4         | 3        | 2      | 1      | 0        |
|------|--------|--------|-----------|----------|--------|--------|----------|
| AUTO | SPEED1 | SPEED0 | 32k_GROUP | VIDEOCLK | RATIO1 | RATIO0 | MCLKDIV2 |

### 7.4.1 Auto-Detect

Configures the auto-detect circuitry for detecting the speed mode of the CS43L22 when operating as a slave.

| AUTO         | Auto-detection of Speed Mode                      |
|--------------|---------------------------------------------------|
| 0            | Disabled                                          |
| 1            | Enabled                                           |
| Application: | <a href="#">"Serial Port Clocking" on page 29</a> |

#### Notes:

1. The SPEED[1:0] bits are ignored and speed is determined by the MCLK/LRCK ratio.
2. When AUTO is disabled and the CS43L22 operates in Master Mode, the MCLKDIV2 bit is ignored.
3. Certain sample and MCLK frequencies require setting the SPEED[1:0] bits, the 32k\_GROUP bit (["32kHz Sample Rate Group" on page 39](#)) and/or the VIDEOCLK bit (["27 MHz Video Clock" on page 39](#)) and RATIO[1:0] bits (["Internal MCLK/LRCK Ratio" on page 39](#)). Low sample rates may also affect dynamic range performance in the typical audio band. Refer to the referenced application for more information.

## 7.4.2 Speed Mode

Configures the speed mode of the DAC in Slave Mode and sets the appropriate MCLK divide ratio for LRCK and SCLK in Master Mode.

| SPEED[1:0]   | Slave Mode                                    | Master Mode     |                 |
|--------------|-----------------------------------------------|-----------------|-----------------|
|              | Serial Port Speed                             | MCLK/LRCK Ratio | SCLK/LRCK Ratio |
| 00           | Double-Speed Mode (DSM - 50 kHz -100 kHz Fs)  | 512             | 64              |
| 01           | Single-Speed Mode (SSM - 4 kHz -50 kHz Fs)    | 256             | 64              |
| 10           | Half-Speed Mode (HSM - 12.5kHz -25 kHz Fs)    | 128             | 64              |
| 11           | Quarter-Speed Mode (QSM - 4 kHz -12.5 kHz Fs) | 128             | 64              |
| Application: | "Serial Port Clocking" on page 29             |                 |                 |

### Notes:

1. Slave/Master Mode is determined by the M/ $\bar{S}$  bit in "Master/Slave Mode" on page 40.
2. Certain sample and MCLK frequencies require setting the SPEED[1:0] bits, the 32k\_GROUP bit ("32kHz Sample Rate Group" on page 39) and/or the VIDEOCLK bit ("27 MHz Video Clock" on page 39) and RATIO[1:0] bits ("Internal MCLK/LRCK Ratio" on page 39). Low sample rates may also affect dynamic range performance in the typical audio band. Refer to the referenced application for more information.
3. These bits are ignored when the AUTO bit ("Auto-Detect" on page 38) is enabled.

## 7.4.3 32kHz Sample Rate Group

Specifies whether or not the input/output sample rate is 8 kHz, 16 kHz or 32 kHz.

| 32kGROUP     | 8 kHz, 16 kHz or 32 kHz sample rate? |
|--------------|--------------------------------------|
| 0            | No                                   |
| 1            | Yes                                  |
| Application: | "Serial Port Clocking" on page 29    |

## 7.4.4 27 MHz Video Clock

Specifies whether or not the external MCLK frequency is 27 MHz

| VIDEOCLK     | 27 MHz MCLK?                      |
|--------------|-----------------------------------|
| 0            | No                                |
| 1            | Yes                               |
| Application: | "Serial Port Clocking" on page 29 |

## 7.4.5 Internal MCLK/LRCK Ratio

Configures the internal MCLK/LRCK ratio.

| RATIO[1:0]   | Internal MCLK Cycles per LRCK     | SCLK/LRCK Ratio in Master Mode |
|--------------|-----------------------------------|--------------------------------|
| 00           | 128                               | 64                             |
| 01           | 125                               | 62                             |
| 10           | 132                               | 66                             |
| 11           | 136                               | 68                             |
| Application: | "Serial Port Clocking" on page 29 |                                |

### 7.4.6 MCLK Divide By 2

Divides the input MCLK by 2 prior to all internal circuitry.

| MCLKDIV2     | MCLK signal into DAC                              |
|--------------|---------------------------------------------------|
| 0            | No divide                                         |
| 1            | Divided by 2                                      |
| Application: | <a href="#">"Serial Port Clocking" on page 29</a> |

**Note:** In Slave Mode, this bit is ignored when the AUTO bit (["Auto-Detect" on page 38](#)) is disabled.

## 7.5 Interface Control 1 (Address 06h)

| 7   | 6        | 5        | 4   | 3       | 2       | 1    | 0    |
|-----|----------|----------|-----|---------|---------|------|------|
| M/S | INV_SCLK | Reserved | DSP | DACDIF1 | DACDIF0 | AWL1 | AWL0 |

### 7.5.1 Master/Slave Mode

Configures the serial port I/O clocking.

| M/S | Serial Port Clocks   |
|-----|----------------------|
| 0   | Slave (input ONLY)   |
| 1   | Master (output ONLY) |

### 7.5.2 SCLK Polarity

Configures the polarity of the SCLK signal.

| INV_SCLK | SCLK Polarity |
|----------|---------------|
| 0        | Not Inverted  |
| 1        | Inverted      |

### 7.5.3 DSP Mode

Configures a data-packed interface format for the DAC.

| DSP          | DSP Mode                              |
|--------------|---------------------------------------|
| 0            | Disabled                              |
| 1            | Enabled                               |
| Application: | <a href="#">"DSP Mode" on page 31</a> |

**Notes:**

1. Select the audio word length using the AWL[1:0] bits (["Audio Word Length" on page 41](#)).
2. The interface format for the DAC must be set to "Left-Justified" when DSP Mode is enabled.

### 7.5.4 DAC Interface Format

Configures the digital interface format for data on SDIN.

| DACDIF[1:0]  | DAC Interface Format                                   |
|--------------|--------------------------------------------------------|
| 00           | Left Justified, up to 24-bit data                      |
| 01           | I <sup>2</sup> S, up to 24-bit data                    |
| 10           | Right Justified                                        |
| 11           | Reserved                                               |
| Application: | <a href="#">"Digital Interface Formats" on page 30</a> |

**Note:** Select the audio word length for Right Justified using the AWL[1:0] bits (["Audio Word Length" on page 41](#)).

### 7.5.5 Audio Word Length

Configures the audio sample word length used for the data into SDIN.

| AWL[1:0]     | Audio Word Length     |                 |
|--------------|-----------------------|-----------------|
|              | DSP Mode              | Right Justified |
| 00           | 32-bit data           | 24-bit data     |
| 01           | 24-bit data           | 20-bit data     |
| 10           | 20-bit data           | 18-bit data     |
| 11           | 16-bit data           | 16-bit data     |
| Application: | "DSP Mode" on page 31 |                 |

**Note:** When the internal MCLK/LRCK ratio is set to 125 in Master Mode, the 32-bit data width option for DSP Mode is not valid unless SCLK=MCLK.

## 7.6 Interface Control 2 (Address 07h)

| 7        | 6         | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|-----------|----------|----------|----------|----------|----------|----------|
| Reserved | SCLK=MCLK | Reserved | Reserved | INV_SWCH | Reserved | Reserved | Reserved |

### 7.6.1 SCLK equals MCLK

Configures the SCLK signal source for Master Mode.

| SCLK=MCLK | Output SCLK                                      |
|-----------|--------------------------------------------------|
| 0         | Re-timed signal, synchronously derived from MCLK |
| 1         | Non-retimed, MCLK signal                         |

**Note:** This bit is only valid for MCLK = 12.0000 MHz.

### 7.6.2 Speaker/Headphone Switch Invert

Determines the control signal polarity of the SPK/HP\_SW pin.

| INV_SWCH | SPK/HP_SW pin 6 Control |
|----------|-------------------------|
| 0        | Not inverted            |
| 1        | Inverted                |

## 7.7 Passthrough x Select: PassA (Address 08h), PassB (Address 09h)

| 7        | 6        | 5        | 4        | 3         | 2         | 1         | 0         |
|----------|----------|----------|----------|-----------|-----------|-----------|-----------|
| Reserved | Reserved | Reserved | Reserved | PASSASEL4 | PASSASEL3 | PASSASEL2 | PASSASEL1 |

### 7.7.1 Passthrough Input Channel Mapping

Selects one or sums/mixes the analog input signal into the passthrough Amplifier. Each bit of the PASSx\_SEL[4:1] word corresponds to individual channels (i.e. PASSx\_SEL1 selects AIN1x, PASSx\_SEL2 selects AIN2x, etc.).

| PASSxSEL[4:1] | Selected Input to Passthrough Channel x         |
|---------------|-------------------------------------------------|
| 00000         | No inputs selected                              |
| 00001         | AIN1x                                           |
| 00010         | AIN2x                                           |
| 00100         | AIN3x                                           |
| 01000         | AIN4x                                           |
| Application:  | <a href="#">"Analog Passthrough" on page 24</a> |

Note: Table does not show all possible combinations.

## 7.8 Analog ZC and SR Settings (Address 0Ah)

| 7        | 6        | 5        | 4        | 3        | 2       | 1        | 0       |
|----------|----------|----------|----------|----------|---------|----------|---------|
| Reserved | Reserved | Reserved | Reserved | ANLGSFTB | ANLGZCB | ANLGSFTA | ANLGZCA |

### 7.8.1 Ch. x Analog Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

| ANLGSFTx   | Volume Changes                | Affected Analog Volume Controls                   |
|------------|-------------------------------|---------------------------------------------------|
| 0          | Do not occur with a soft ramp | PASSxVOL[7:0] (“Passthrough x Volume” on page 46) |
| 1          | Occur with a soft ramp        |                                                   |
| Ramp Rate: | 1/2 dB every 16 LRCK cycles   |                                                   |

### 7.8.2 Ch. x Analog Zero Cross

Configures when the signal level changes occur for the analog volume controls.

| ANLGZCx | Volume Changes                  | Affected Analog Volume Controls                                     |
|---------|---------------------------------|---------------------------------------------------------------------|
| 0       | Do not occur on a zero crossing | PASSxVOL[7:0] ( <a href="#">"Passthrough x Volume" on page 46</a> ) |
| 1       | Occur on a zero crossing        |                                                                     |

**Note:** If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period of 1024 sample periods (approximately 10.7 ms at 48 kHz sample rate).

## 7.9 Passthrough Gang Control (Address 0Ch)

| 7       | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|---------|----------|----------|----------|----------|----------|----------|----------|
| PASSB=A | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

### 7.9.1 Passthrough Channel B=A Gang Control

Configures independent or ganged control of the passthrough channel settings. Mute is not affected.

| PASSB=A | Single Volume Control |
|---------|-----------------------|
| 0       | Disabled              |
| 1       | Enabled               |

## 7.10 Playback Control 1 (Address 0Dh)

| 7       | 6       | 5       | 4         | 3        | 2        | 1        | 0        |
|---------|---------|---------|-----------|----------|----------|----------|----------|
| HPGAIN2 | HPGAIN1 | HPGAIN0 | PLYBCKB=A | INV_PCMB | INV_PCMA | MSTBMUTE | MSTAMUTE |

### 7.10.1 Headphone Analog Gain

Selects the gain multiplier for the headphone/line outputs.

| HPGAIN[2:0] | Headphone/Line Gain Setting (G) |
|-------------|---------------------------------|
| 000         | 0.3959                          |
| 001         | 0.4571                          |
| 010         | 0.5111                          |
| 011         | 0.6047                          |
| 100         | 0.7099                          |
| 101         | 0.8399                          |
| 110         | 1.000                           |
| 111         | 1.1430                          |

**Note:** Refer to “Headphone Output Power Characteristics” on page 14 and “Headphone Output Power Characteristics” on page 14.

### 7.10.2 Playback Volume Setting B=A

Configures independent or ganged volume control of all playback channels. Mute is not affected.

| PLYBCKB=A | Single Volume Control for all Playback Channels |
|-----------|-------------------------------------------------|
| 0         | Disabled                                        |
| 1         | Enabled                                         |

### 7.10.3 Invert PCM Signal Polarity

Configures the polarity of the digital input signal.

| INV_PCMx | PCM Signal Polarity |
|----------|---------------------|
| 0        | Not Inverted        |
| 1        | Inverted            |

### 7.10.4 Master Playback Mute

Configures a digital mute on the master volume control for channel x.

| MSTxMUTE | Master Mute  |
|----------|--------------|
| 0        | Not Inverted |
| 1        | Inverted     |

**Note:** The muting function is affected by the DIGSFT (“Digital Soft Ramp” on page 44) and DIGZC (“Digital Zero Cross” on page 45) bits.

## 7.11 Miscellaneous Controls (Address 0Eh)

| 7         | 6         | 5         | 4         | 3      | 2      | 1      | 0     |
|-----------|-----------|-----------|-----------|--------|--------|--------|-------|
| PASSTHRUB | PASSTHRUA | PASSBMUTE | PASSAMUTE | FREEZE | DEEMPH | DIGSFT | DIGZC |

### 7.11.1 Passthrough Analog

Configures an analog passthrough from the analog inputs to the headphone/line outputs.

| PASSTHRUx | Analog In Routed to HP/Line Output |
|-----------|------------------------------------|
| 0         | Disabled                           |
| 1         | Enabled                            |

### 7.11.2 Passthrough Mute

Configures an analog mute on the channel x analog in to analog out passthrough.

| PASSxMUTE | Passthrough Mute |
|-----------|------------------|
| 0         | Disabled         |
| 1         | Enabled          |

### 7.11.3 Freeze Registers

Configures a hold on all register settings.

| FREEZE | Control Port Status                                                                                                           |
|--------|-------------------------------------------------------------------------------------------------------------------------------|
| 0      | Register changes take effect immediately                                                                                      |
| 1      | Modifications may be made to all control port registers without the changes taking effect until after the FREEZE is disabled. |

### 7.11.4 HP/Speaker De-Emphasis

Configures a 15μs/50μs digital de-emphasis filter response on the headphone/line and speaker outputs.

| DEEMPHASIS | Control Port Status |
|------------|---------------------|
| 0          | Disabled            |
| 1          | Enabled             |

### 7.11.5 Digital Soft Ramp

Configures an incremental volume ramp from the current level to the new level at the specified rate.

| DIGSFT     | Volume Changes                  | Affected Digital Volume Controls                                                                                                                                                   |
|------------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0          | Does not occur with a soft ramp | MSTxMUTE ("Master Playback Mute" on page 43),<br>HPxMUTE, SPKxMUTE ("Playback Control 2 (Address 0Fh)" on page 45),<br>PCMxMUTE, PCMxVOL[7:0] ("PCM Channel x Volume" on page 47), |
| 1          | Occurs with a soft ramp         | MSTxVOL[7:0] ("Master Volume Control" on page 51),<br>HPxVOL[7:0] ("Headphone Volume Control" on page 51),<br>SPKxVOL[7:0] ("Speaker Volume Control" on page 52),                  |
| Ramp Rate: |                                 | 1/8 dB every LRCK cycle                                                                                                                                                            |

### 7.11.6 Digital Zero Cross

Configures when the signal level changes occur for the digital volume controls.

| DIGZC | Volume Changes                  | Affected Digital Volume Controls                                                                                                                                                   |
|-------|---------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | Do not occur on a zero crossing | MSTxMUTE ("Master Playback Mute" on page 43),<br>HPxMUTE, SPKxMUTE ("Playback Control 2 (Address 0Fh)" on page 45),<br>PCMxMUTE, PCMxVOL[7:0] ("PCM Channel x Volume" on page 47), |
| 1     | Occur on a zero crossing        | MSTxVOL[7:0] ("Master Volume Control" on page 51),<br>HPxVOL[7:0] ("Headphone Volume Control" on page 51),<br>SPKxVOL[7:0] ("Speaker Volume Control" on page 52),                  |

#### Notes:

1. If the signal does not encounter a zero crossing, the requested volume change will occur after a timeout period between 1024 and 2048 sample periods (21.3 ms to 42.7 ms at 48 kHz sample rate).
2. The zero cross function is independently monitored and implemented for each channel.
3. The DIS\_LIMSFT bit ("Limiter Soft Ramp Disable" on page 53) is ignored when zero cross is enabled.

### 7.12 Playback Control 2 (Address 0Fh)

| 7       | 6       | 5        | 4        | 3      | 2       | 1       | 0         |
|---------|---------|----------|----------|--------|---------|---------|-----------|
| HPBMUTE | HPAMUTE | SPKBMUTE | SPKAMUTE | SPKB=A | SPKSWAP | SPKMONO | MUTE50/50 |

#### 7.12.1 Headphone Mute

Configures a digital mute on headphone channel x.

| HPxMUTE | Headphone Mute |
|---------|----------------|
| 0       | Disabled       |
| 1       | Enabled        |

#### 7.12.2 Speaker Mute

Configures a digital mute on speaker channel x.

| SPKxMUTE | Speaker Mute |
|----------|--------------|
| 0        | Disabled     |
| 1        | Enabled      |

#### 7.12.3 Speaker Volume Setting B=A

Configures independent or ganged volume control of the speaker volume. Mute is not affected.

| SPKB=A | Single Volume Control for the Speaker Channel |
|--------|-----------------------------------------------|
| 0      | Disabled                                      |
| 1      | Enabled                                       |

#### 7.12.4 Speaker Channel Swap

Configures a channel swap on the speaker channels.

| SPKSWAP      | Speaker Output                                 |
|--------------|------------------------------------------------|
| 0            | Channel A                                      |
| 1            | Channel B                                      |
| Application: | "Mono Speaker Output Configuration" on page 27 |

### 7.12.5 Speaker MONO Control

Configures a parallel full bridge output for the speaker channels.

| SPKMONO      | Parallel Full Bridge Output                                    |
|--------------|----------------------------------------------------------------|
| 0            | Disabled                                                       |
| 1            | Enabled                                                        |
| Application: | <a href="#">"Mono Speaker Output Configuration" on page 27</a> |

### 7.12.6 Speaker Mute 50/50 Control

Configures how the speaker channels mute.

| MUTE50/50 | Speaker Mute 50/50                                                                                             |
|-----------|----------------------------------------------------------------------------------------------------------------|
| 0         | Disabled; The PWM amplifiers outputs modulated silence when SPKxMUTE is enabled.                               |
| 1         | Enabled; The PWM amplifiers switch at an exact 50%-duty-cycle signal (not modulated) when SPKxMUTE is enabled. |

## 7.13 Passthrough x Volume: PASSAVOL (Address 14h) & PASSBVOL (Address 15h)

| 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| PASSxVOL7 | PASSxVOL6 | PASSxVOL5 | PASSxVOL4 | PASSxVOL3 | PASSxVOL2 | PASSxVOL1 | PASSxVOL0 |

### 7.13.1 Passthrough x Volume

Sets the volume/gain of the analog input signal routed to the headphone/line output.

| PASSxVOL[7:0] | Gain                                            |
|---------------|-------------------------------------------------|
| 0111 1111     | 12 dB                                           |
| ...           | ...                                             |
| 0001 1000     | 12 dB                                           |
| ...           | ...                                             |
| 0000 0001     | +0.5 dB                                         |
| 0000 0000     | 0 dB                                            |
| 1111 1111     | -0.5 dB                                         |
| ...           | ...                                             |
| 1000 1000     | -60.0 dB                                        |
| ...           | ...                                             |
| 1000 0000     | -60.0 dB                                        |
| Step Size:    | 0.5 dB (approximate)                            |
| Application:  | <a href="#">"Passthrough Analog" on page 44</a> |

#### Notes:

1. This register is ignored when the PASSTHRUx bit (["Passthrough Analog" on page 44](#)) is disabled.
2. The step size may deviate from 0.5 dB at settings below -40 dB. Code settings 0x95, 0xA1, 0xAD and 0xB9 are not guaranteed to be monotonic.

## 7.14 PCMx Volume: PCMA (Address 1Ah) & PCMB (Address 1Bh)

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| PCMxMUTE | PCMxVOL6 | PCMxVOL5 | PCMxVOL4 | PCMxVOL3 | PCMxVOL2 | PCMxVOL1 | PCMxVOL0 |

### 7.14.1 PCM Channel x Mute

Configures a digital mute on the PCM data from the serial data input (SDIN) to the DSP.

| PCMxMUTE | PCM Mute |
|----------|----------|
| 0        | Disabled |
| 1        | Enabled  |

### 7.14.2 PCM Channel x Volume

Sets the volume/gain of the PCM data from the serial data input (SDIN) to the DSP.

| PCMxVOL[6:0] | Volume   |
|--------------|----------|
| 001 1000     | +12.0 dB |
| ...          | ...      |
| 000 0001     | +0.5 dB  |
| 000 0000     | 0 dB     |
| 111 1111     | -0.5 dB  |
| ...          | ...      |
| 001 1001     | -51.5 dB |
| Step Size:   | 0.5 dB   |

## 7.15 Beep Frequency & On Time (Address 1Ch)

| 7     | 6     | 5     | 4     | 3       | 2       | 1       | 0       |
|-------|-------|-------|-------|---------|---------|---------|---------|
| FREQ3 | FREQ2 | FREQ1 | FREQ0 | ONTIME3 | ONTIME2 | ONTIME1 | ONTIME0 |

### 7.15.1 Beep Frequency

Sets the frequency of the beep signal.

| FREQ[3:0]    | Frequency ( $F_s = 12, 24, 48$ or $96$ kHz) | Pitch |
|--------------|---------------------------------------------|-------|
| 0000         | 260.87 Hz                                   | C4    |
| 0001         | 521.74 Hz                                   | C5    |
| 0010         | 585.37 Hz                                   | D5    |
| 0011         | 666.67 Hz                                   | E5    |
| 0100         | 705.88 Hz                                   | F5    |
| 0101         | 774.19 Hz                                   | G5    |
| 0110         | 888.89 Hz                                   | A5    |
| 0111         | 1000.00 Hz                                  | B5    |
| 1000         | 1043.48 Hz                                  | C6    |
| 1001         | 1200.00 Hz                                  | D6    |
| 1010         | 1333.33 Hz                                  | E6    |
| 1011         | 1411.76 Hz                                  | F6    |
| 1100         | 1600.00 Hz                                  | G6    |
| 1101         | 1714.29 Hz                                  | A6    |
| 1110         | 2000.00 Hz                                  | B6    |
| 1111         | 2181.82 Hz                                  | C7    |
| Application: | <a href="#">"Beep Generator" on page 22</a> |       |

**Notes:**

1. This setting must not change when BEEP is enabled.
2. Beep frequency will scale directly with sample rate,  $F_s$ , but is fixed at the nominal  $F_s$  within each speed mode.

### 7.15.2 Beep On Time

Sets the on duration of the beep signal.

| ONTIME[3:0]  | On Time ( $F_s = 12, 24, 48$ or $96$ kHz)   |
|--------------|---------------------------------------------|
| 0000         | ~86 ms                                      |
| 0001         | ~430 ms                                     |
| 0010         | ~780 ms                                     |
| 0011         | ~1.20 s                                     |
| 0100         | ~1.50 s                                     |
| 0101         | ~1.80 s                                     |
| 0110         | ~2.20 s                                     |
| 0111         | ~2.50 s                                     |
| 1000         | ~2.80 s                                     |
| 1001         | ~3.20 s                                     |
| 1010         | ~3.50 s                                     |
| 1011         | ~3.80 s                                     |
| 1100         | ~4.20 s                                     |
| 1101         | ~4.50 s                                     |
| 1110         | ~4.80 s                                     |
| 1111         | ~5.20 s                                     |
| Application: | <a href="#">"Beep Generator" on page 22</a> |

**Notes:**

1. This setting must not change when BEEP is enabled.
2. Beep on time will scale inversely with sample rate,  $F_s$ , but is fixed at the nominal  $F_s$  within each speed mode.

### 7.16 Beep Volume & Off Time (Address 1Dh)

| 7        | 6        | 5        | 4      | 3      | 2      | 1      | 0      |
|----------|----------|----------|--------|--------|--------|--------|--------|
| OFFTIME2 | OFFTIME1 | OFFTIME0 | BPVOL4 | BPVOL3 | BPVOL2 | BPVOL1 | BPVOL0 |

#### 7.16.1 Beep Off Time

Sets the off duration of the beep signal.

| OFFTIME[2:0] | Off Time ( $F_s = 48$ or $96$ kHz)          |
|--------------|---------------------------------------------|
| 000          | ~1.23 s                                     |
| 001          | ~2.58 s                                     |
| 010          | ~3.90 s                                     |
| 011          | ~5.20 s                                     |
| 100          | ~6.60 s                                     |
| 101          | ~8.05 s                                     |
| 110          | ~9.35 s                                     |
| 111          | ~10.80 s                                    |
| Application: | <a href="#">"Beep Generator" on page 22</a> |

**Notes:**

1. This setting must not change when BEEP is enabled.
2. Beep off time will scale inversely with sample rate, Fs, but is fixed at the nominal Fs within each speed mode.

### 7.16.2 Beep Volume

Sets the volume of the beep signal.

| BEEPVOL[4:0] | Gain                                        |
|--------------|---------------------------------------------|
| 00110        | +6.0 dB                                     |
| ...          | ...                                         |
| 00000        | -6 dB                                       |
| 11111        | -8 dB                                       |
| 11110        | -10 dB                                      |
| ...          | ...                                         |
| 00111        | -56 dB                                      |
| Step Size:   | 2 dB                                        |
| Application: | <a href="#">"Beep Generator" on page 22</a> |

**Note:** This setting must not change when BEEP is enabled.

## 7.17 Beep & Tone Configuration (Address 1Eh)

| 7     | 6     | 5          | 4       | 3       | 2       | 1       | 0    |
|-------|-------|------------|---------|---------|---------|---------|------|
| BEEP1 | BEEP0 | BEEPMIXDIS | TREBCF1 | TREBCF0 | BASSCF1 | BASSCF0 | TCEN |

### 7.17.1 Beep Configuration

Configures a beep mixed with the HP/Line and SPK output.

| BEEP[1:0]    | Beep Occurrence                             |
|--------------|---------------------------------------------|
| 00           | Off                                         |
| 01           | Single                                      |
| 10           | Multiple                                    |
| 11           | Continuous                                  |
| Application: | <a href="#">"Beep Generator" on page 22</a> |

**Notes:**

1. When used in analog pass through mode, the output alternates between the signal from the Passthrough Amplifier and the beep signal. The beep signal does not mix with the analog signal from the Passthrough Amplifier.
2. Re-engaging the beep before it has completed its initial cycle will cause the beep signal to remain ON for the maximum ONTIME duration.

### 7.17.2 Beep Mix Disable

Configures how the beep mixes with the serial data input.

| BEEPMIXDIS   | Beep Output to HP/Line and Speaker                                                                                                                                                      |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0            | Mix Enabled; The beep signal mixes with the digital signal from the serial data input.                                                                                                  |
| 1            | Mix Disabled; The output alternates between the signal from the serial data input and the beep signal. The beep signal does not mix with the digital signal from the serial data input. |
| Application: | <a href="#">"Beep Generator" on page 22</a>                                                                                                                                             |

**Note:** This setting must not change when BEEP is enabled.

### 7.17.3 Treble Corner Frequency

Sets the corner frequency (-3 dB point) for the treble shelving filter.

| TREBCF[1:0] | Treble Corner Frequency Setting |
|-------------|---------------------------------|
| 00          | 5 kHz                           |
| 01          | 7 kHz                           |
| 10          | 10 kHz                          |
| 11          | 15 kHz                          |

### 7.17.4 Bass Corner Frequency

Sets the corner frequency (-3 dB point) for the bass shelving filter.

| BASSCF[1:0] | Bass Corner Frequency Setting |
|-------------|-------------------------------|
| 00          | 50 Hz                         |
| 01          | 100 Hz                        |
| 10          | 200 Hz                        |
| 11          | 250 Hz                        |

### 7.17.5 Tone Control Enable

Configures the treble and bass activation.

| TCEN         | Bass and Treble Control                     |
|--------------|---------------------------------------------|
| 0            | Disabled                                    |
| 1            | Enabled                                     |
| Application: | <a href="#">"Beep Generator" on page 22</a> |

## 7.18 Tone Control (Address 1Fh)

| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
|-------|-------|-------|-------|-------|-------|-------|-------|
| TREB3 | TREB2 | TREB1 | TREB0 | BASS3 | BASS2 | BASS1 | BASS0 |

### 7.18.1 Treble Gain

Sets the gain of the treble shelving filter.

| TREB[3:0]  | Gain Setting |
|------------|--------------|
| 0000       | +12.0 dB     |
| ...        | ...          |
| 0111       | +1.5 dB      |
| 1000       | 0 dB         |
| 1001       | -1.5 dB      |
| ...        | ...          |
| 1111       | -10.5 dB     |
| Step Size: | 1.5 dB       |

### 7.18.2 Bass Gain

Sets the gain of the bass shelving filter.

| TREB[3:0]  | Gain Setting |
|------------|--------------|
| 0000       | +12.0 dB     |
| ...        | ...          |
| 0111       | +1.5 dB      |
| 1000       | 0 dB         |
| 1001       | -1.5 dB      |
| ...        | ...          |
| 1111       | -10.5 dB     |
| Step Size: | 1.5 dB       |

## 7.19 Master Volume Control: MSTA (Address 20h) & MSTB (Address 21h)

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| MSTxVOL7 | MSTxVOL6 | MSTxVOL5 | MSTxVOL4 | MSTxVOL3 | MSTxVOL2 | MSTxVOL1 | MSTxVOL0 |

### 7.19.1 Master Volume Control

Sets the volume of the signal out the DSP.

| MSTxVOL[7:0] | Master Volume |
|--------------|---------------|
| 0001 1000    | +12.0 dB      |
| ...          | ...           |
| 0000 0000    | 0 dB          |
| 1111 1111    | -0.5 dB       |
| 1111 1110    | -1.0 dB       |
| ...          | ...           |
| 0011 0100    | -102 dB       |
| ...          | ...           |
| 0001 1001    | -102 dB       |
| Step Size:   | 0.5 dB        |

## 7.20 Headphone Volume Control: HPA (Address 22h) & HPB (Address 23h)

| 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
|---------|---------|---------|---------|---------|---------|---------|---------|
| HPxVOL7 | HPxVOL6 | HPxVOL5 | HPxVOL4 | HPxVOL3 | HPxVOL2 | HPxVOL1 | HPxVOL0 |

### 7.20.1 Headphone Volume Control

Sets the volume of the signal out the DAC.

| HPxVOL[7:0] | Headphone Volume |
|-------------|------------------|
| 0000 0000   | 0 dB             |
| 1111 1111   | -0.5 dB          |
| 1111 1110   | -1.0 dB          |
| ...         | ...              |
| 0011 0100   | -96.0 dB         |
| ...         | ...              |
| 0000 0001   | Muted            |
| Step Size:  | 0.5 dB           |

## 7.21 Speaker Volume Control: SPKA (Address 24h) & SPKB (Address 25h)

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| SPKxVOL7 | SPKxVOL6 | SPKxVOL5 | SPKxVOL4 | SPKxVOL3 | SPKxVOL2 | SPKxVOL1 | SPKxVOL0 |

### 7.21.1 Speaker Volume Control

Sets the volume of the signal out the PWM modulator.

| SPKxVOL[7:0]      | Speaker Volume |
|-------------------|----------------|
| 0000 0000         | 0 dB           |
| 1111 1111         | -0.5 dB        |
| 1111 1110         | -1.0 dB        |
| ...               | ...            |
| 0100 0000         | -96.0 dB       |
| ...               | ...            |
| 0000 0001         | Muted          |
| <b>Step Size:</b> | 0.5 dB         |

**Note:** The maximum step size error is +/-0.15 dB.

## 7.22 PCM Channel Swap (Address 26h)

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| PCMASWP1 | PCMASWP0 | PCMBSWP1 | PCMBSWP0 | Reserved | Reserved | Reserved | Reserved |

### 7.22.1 PCM Channel Swap

Configures a mix/swap of the PCM data to the headphone/line or speaker outputs.

| PCMxSWP[1:0] | PCM to HP/LINEOUTA | PCM to HP/LINEOUTB |
|--------------|--------------------|--------------------|
| 00           | Left               | Right              |
| 01           | (Left + Right)/2   | (Left + Right)/2   |
| 10           |                    |                    |
| 11           | Right              | Left               |

## 7.23 Limiter Control 1, Min/Max Thresholds (Address 27h)

| 7     | 6     | 5     | 4     | 3     | 2     | 1        | 0        |
|-------|-------|-------|-------|-------|-------|----------|----------|
| LMAX2 | LMAX1 | LMAX0 | CUSH2 | CUSH1 | CUSH0 | LIMSRDIS | LIMZCDIS |

### 7.23.1 Limiter Maximum Threshold

Sets the maximum level, below full scale, at which to limit and attenuate the output signal at the attack rate (LIMARATE - [“Limiter Release Rate” on page 54](#)).

| LMAX[2:0]    | Threshold Setting                    |
|--------------|--------------------------------------|
| 000          | 0 dB                                 |
| 001          | -3 dB                                |
| 010          | -6 dB                                |
| 011          | -9 dB                                |
| 100          | -12 dB                               |
| 101          | -18 dB                               |
| 110          | -24 dB                               |
| 111          | -30 dB                               |
| Application: | <a href="#">“Limiter” on page 22</a> |

**Note:** Bass, Treble and digital gain settings that boost the signal beyond the maximum threshold may trigger an attack.

### 7.23.2 Limiter Cushion Threshold

Sets the minimum level at which to disengage the Limiter’s attenuation at the release rate (LIMRRATE - [“Limiter Release Rate” on page 54](#)) until levels lie between the LMAX and CUSH thresholds.

| CUSH[2:0]    | Threshold Setting                    |
|--------------|--------------------------------------|
| 000          | 0 dB                                 |
| 001          | -3 dB                                |
| 010          | -6 dB                                |
| 011          | -9 dB                                |
| 100          | -12 dB                               |
| 101          | -18 dB                               |
| 110          | -24 dB                               |
| 111          | -30 dB                               |
| Application: | <a href="#">“Limiter” on page 22</a> |

**Note:** This setting is usually set slightly below the LMAX threshold.

### 7.23.3 Limiter Soft Ramp Disable

Configures an override of the digital soft ramp setting.

| LIMSRDIS     | Limiter Soft Ramp Disable                                                                                     |
|--------------|---------------------------------------------------------------------------------------------------------------|
| 0            | OFF; Limiter Attack Rate is dictated by the DIGSFT ( <a href="#">“Digital Soft Ramp” on page 44</a> ) setting |
| 1            | ON; Limiter volume changes take effect in one step, regardless of the DIGSFT setting.                         |
| Application: | <a href="#">“Limiter” on page 22</a>                                                                          |

**Note:** This bit is ignored when the DIGZC ([“Digital Zero Cross” on page 45](#)) is enabled.

### 7.23.4 Limiter Zero Cross Disable

Configures an override of the digital zero cross setting.

| LIMZCDIS     | Limiter Zero Cross Disable                                                                                    |
|--------------|---------------------------------------------------------------------------------------------------------------|
| 0            | OFF; Limiter Attack Rate is dictated by the DIGZC ( <a href="#">“Digital Zero Cross” on page 45</a> ) setting |
| 1            | ON; Limiter volume changes take effect in one step, regardless of the DIGZC setting.                          |
| Application: | <a href="#">“Limiter” on page 22</a>                                                                          |

## 7.24 Limiter Control 2, Release Rate (Address 28h)

| 7     | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
|-------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| LIMIT | LIMIT_ALL | LIMRRATE5 | LIMRRATE4 | LIMRRATE3 | LIMRRATE2 | LIMRRATE1 | LIMRRATE0 |

### 7.24.1 Peak Detect and Limiter

Configures the peak detect and limiter circuitry.

| LIMIT        | Limiter Status                       |
|--------------|--------------------------------------|
| 0            | Disabled                             |
| 1            | Enabled                              |
| Application: | <a href="#">“Limiter” on page 22</a> |

### 7.24.2 Peak Signal Limit All Channels

Sets how channels are attenuated when the limiter is enabled.

| LIMIT_ALL    | Limiter action:                                                                                                                                                                                                                                                     |
|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0            | Apply the necessary attenuation on a specific channel only when the signal amplitude on <i>that</i> specific channel rises above LMAX.<br>Remove attenuation on a specific channel only when the signal amplitude on <i>that</i> specific channel falls below CUSH. |
| 1            | Apply the necessary attenuation on BOTH channels when the signal amplitude on any ONE channel rises above LMAX.<br>Remove attenuation on BOTH channels only when the signal amplitude on BOTH channels fall below CUSH.                                             |
| Application: | <a href="#">“Limiter” on page 22</a>                                                                                                                                                                                                                                |

### 7.24.3 Limiter Release Rate

Sets the rate at which the limiter releases the digital attenuation from levels below the CUSH[2:0] threshold ([“Limiter Cushion Threshold” on page 53](#)) and returns the analog output level to the MSTxVOL[7:0] ([“Master Volume Control” on page 51](#)) setting.

| LIMRRATE[5:0] | Release Time                         |
|---------------|--------------------------------------|
| 00 0000       | Fastest Release                      |
| ...           | ...                                  |
| 11 1111       | Slowest Release                      |
| Application:  | <a href="#">“Limiter” on page 22</a> |

**Note:** The limiter release rate is user-selectable but is also a function of the sampling frequency, Fs, and the DIGSFT ([“Digital Soft Ramp” on page 44](#)) and DIGZC ([“Digital Zero Cross” on page 45](#)) setting.

## 7.25 Limiter Attack Rate (Address 29h)

| 7        | 6        | 5         | 4         | 3         | 2         | 1         | 0         |
|----------|----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Reserved | Reserved | LIMARATE5 | LIMARATE4 | LIMARATE3 | LIMARATE2 | LIMARATE1 | LIMARATE0 |

### 7.25.1 Limiter Attack Rate

Sets the rate at which the limiter applies digital attenuation from levels above the MAX[2:0] threshold ([“Limiter Maximum Threshold” on page 53](#)).

| LIMARATE[5:0] | Attack Time                          |
|---------------|--------------------------------------|
| 00 0000       | Fastest Attack                       |
| ...           | ...                                  |
| 11 1111       | Slowest Attack                       |
| Application:  | <a href="#">“Limiter” on page 22</a> |

**Note:** The limiter attack rate is user-selectable but is also a function of the sampling frequency,  $F_s$ , and the DIGSFT ([“Digital Soft Ramp” on page 44](#)) and DIGZC ([“Digital Zero Cross” on page 45](#)) setting unless the respective disable bit ([“Limiter Soft Ramp Disable” on page 53](#) or [“Limiter Zero Cross Disable” on page 54](#)) is enabled.

## 7.26 Status (Address 2Eh) (Read Only)

For all bits in this register, a “1” means the associated error condition has occurred at least once since the register was last read. A “0” means the associated error condition has NOT occurred since the last reading of the register. Reading the register resets all bits to 0.

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| Reserved | SPCLKERR | DSPAOVFL | DSPBOVFL | PCMAOVFL | PCMBOVFL | Reserved | Reserved |

### 7.26.1 Serial Port Clock Error (Read Only)

Indicates the status of the MCLK to LRCK ratio.

| SPCLKERR     | Serial Port Clock Status:                         |
|--------------|---------------------------------------------------|
| 0            | MCLK/LRCK ratio is valid.                         |
| 1            | MCLK/LRCK ratio is not valid.                     |
| Application: | <a href="#">“Serial Port Clocking” on page 29</a> |

**Note:** On initial power up and application of clocks, this bit will report ‘1’b as the serial port re-synchronizes.

### 7.26.2 DSP Engine Overflow (Read Only)

Indicates the over-range status in the DSP data path.

| DSPxOVFL     | DSP Overflow Status:                                             |
|--------------|------------------------------------------------------------------|
| 0            | No digital clipping has occurred in the data path after the DSP. |
| 1            | Digital clipping has occurred in the data path after the DSP.    |
| Application: | <a href="#">“DSP Engine” on page 21</a>                          |

### 7.26.3 PCMx Overflow (Read Only)

Indicates the over-range status in the PCM data path.

| PCMxOVFL     | PCM Overflow Status:                                                                                         |
|--------------|--------------------------------------------------------------------------------------------------------------|
| 0            | No digital clipping has occurred in the data path of the PCM ("PCM Channel x Volume" on page 47) of the DSP. |
| 1            | Digital clipping has occurred in the data path of the PCM of the DSP.                                        |
| Application: | "DSP Engine" on page 21                                                                                      |

## 7.27 Battery Compensation (Address 2Fh)

| 7       | 6         | 5        | 4        | 3      | 2      | 1      | 0      |
|---------|-----------|----------|----------|--------|--------|--------|--------|
| BATTCMP | VPMONITOR | Reserved | Reserved | VPREF3 | VPREF2 | VPREF1 | VPREF0 |

### 7.27.1 Battery Compensation

Configures automatic adjustment of the speaker volume when VP deviates from VPREF[3:0].

| BATTCMP      | Automatic Battery Compensation                  |
|--------------|-------------------------------------------------|
| 0            | Disabled                                        |
| 1            | Enabled                                         |
| Application: | "Maintaining a Desired Output Level" on page 27 |

### 7.27.2 VP Monitor

Configures the internal ADC that monitors the VP voltage level.

| VPMONITOR | VP ADC Status |
|-----------|---------------|
| 0         | Disabled      |
| 1         | Enabled       |

#### Notes:

1. The internal ADC that monitors the VP supply is enabled automatically when BATTCMP is enabled, regardless of the VPMONITOR setting. Conversely, when BATTCMP is disabled, the ADC may be enabled by enabling VPMONITOR; this provides a convenient battery monitor without enabling battery compensation.
2. When enabled, VPMONITOR remains enabled regardless of the PDN bit setting.

### 7.27.3 VP Reference

Sets the desired VP reference used for battery compensation.

| VPREF[3:0]       | Desired VP used to calculate the required attenuation on the speaker output:<br>(for VA = 1.8 V) |
|------------------|--------------------------------------------------------------------------------------------------|
| 0000             | 1.5 V                                                                                            |
| 0001             | 2.0 V                                                                                            |
| 0010             | 2.5 V                                                                                            |
| 0011             | 3.0 V                                                                                            |
| 0100             | 3.5 V                                                                                            |
| 0101             | 4.0 V                                                                                            |
| 0110             | 4.5 V                                                                                            |
| 0111             | 5.0 V                                                                                            |
| (for VA = 2.5 V) |                                                                                                  |
| 1000             | 1.5 V                                                                                            |
| 1001             | 2.0 V                                                                                            |
| 1010             | 2.5 V                                                                                            |
| 1011             | 3.0 V                                                                                            |
| 1100             | 3.5 V                                                                                            |
| 1101             | 4.0 V                                                                                            |
| 1110             | 4.5 V                                                                                            |
| 1111             | 5.0 V                                                                                            |
| Application:     | "VP Battery Compensation" on page 27                                                             |

## 7.28 VP Battery Level (Address 30h) (Read Only)

| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| VPLVL7 | VPLVL6 | VPLVL5 | VPLVL4 | VPLVL3 | VPLVL2 | VPLVL1 | VPLVL0 |

### 7.28.1 VP Voltage Level (Read Only)

Indicates the unsigned VP voltage level.

| VPLVL[7:0] | VP Voltage                                                                             |
|------------|----------------------------------------------------------------------------------------|
| ...        |                                                                                        |
| 0101 1110  | 3.0 V (for VA = 2.0 V); apply formula using actual VA voltage to calculate VP voltage. |
| ...        |                                                                                        |
| 0111 0010  | 3.7 V (for VA = 2.0 V); apply formula using actual VA voltage to calculate VP voltage. |
| ...        |                                                                                        |
| Formula:   | VP Voltage = (Binary representation of VPLVL[7:0]) * VA / 63.3                         |

## 7.29 Speaker Status (Address 31h) (Read Only)

| 7        | 6        | 5        | 4        | 3       | 2        | 1        | 0        |
|----------|----------|----------|----------|---------|----------|----------|----------|
| Reserved | Reserved | SPKASHRT | SPKBSHRT | SPKR/HP | Reserved | Reserved | Reserved |

### 7.29.1 Speaker Current Load Status (Read Only)

Indicates whether or not any of the speaker outputs is shorted to ground.

| SPKxSHRT | Speaker Output Load  |
|----------|----------------------|
| 0        | No overload detected |
| 1        | Overload detected    |

### 7.29.2 SPKR/HP Pin Status (Read Only)

Indicates the status of the SPKR/HP pin.

| SPKR/HP | Pin State   |
|---------|-------------|
| 0       | Pulled Low  |
| 1       | Pulled High |

## 7.30 Charge Pump Frequency (Address 34h)

| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
|----------|----------|----------|----------|----------|----------|----------|----------|
| CHGFREQ3 | CHGFREQ2 | CHGFREQ1 | CHGFREQ0 | Reserved | Reserved | Reserved | Reserved |

### 7.30.1 Charge Pump Frequency

Sets the charge pump frequency on FLYN and FLYP.

| CHGFREQ[3:0] | N                                       |
|--------------|-----------------------------------------|
| 0000         | 0                                       |
| ...          |                                         |
| 0101         | 5                                       |
| ...          |                                         |
| 1111         | 15                                      |
| Formula:     | Frequency = $(64 \times F_s) / (N + 2)$ |

**Note:** The headphone output THD+N performance may be affected.

## 8. ANALOG PERFORMANCE PLOTS

### 8.1 Headphone THD+N versus Output Power Plots

Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave; measurement bandwidth is 10 Hz to 20 kHz;  $F_s = 48$  kHz.

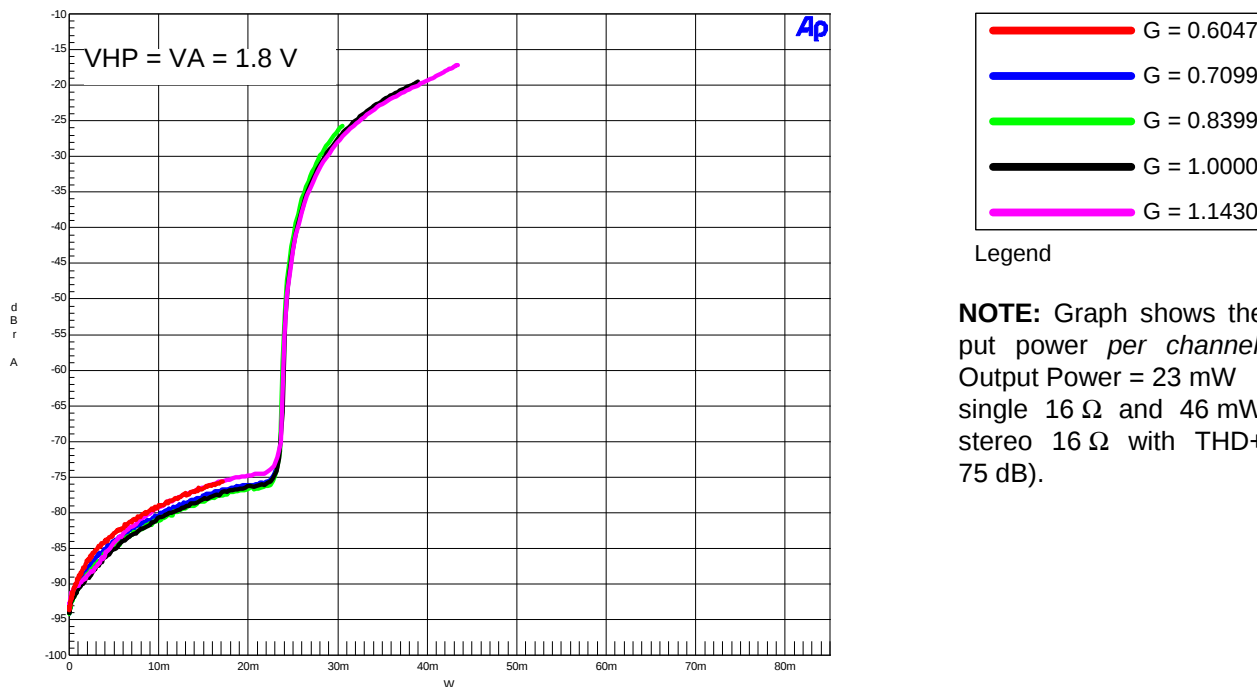


Figure 18. THD+N vs. Output Power per Channel at 1.8 V (16  $\Omega$  load)

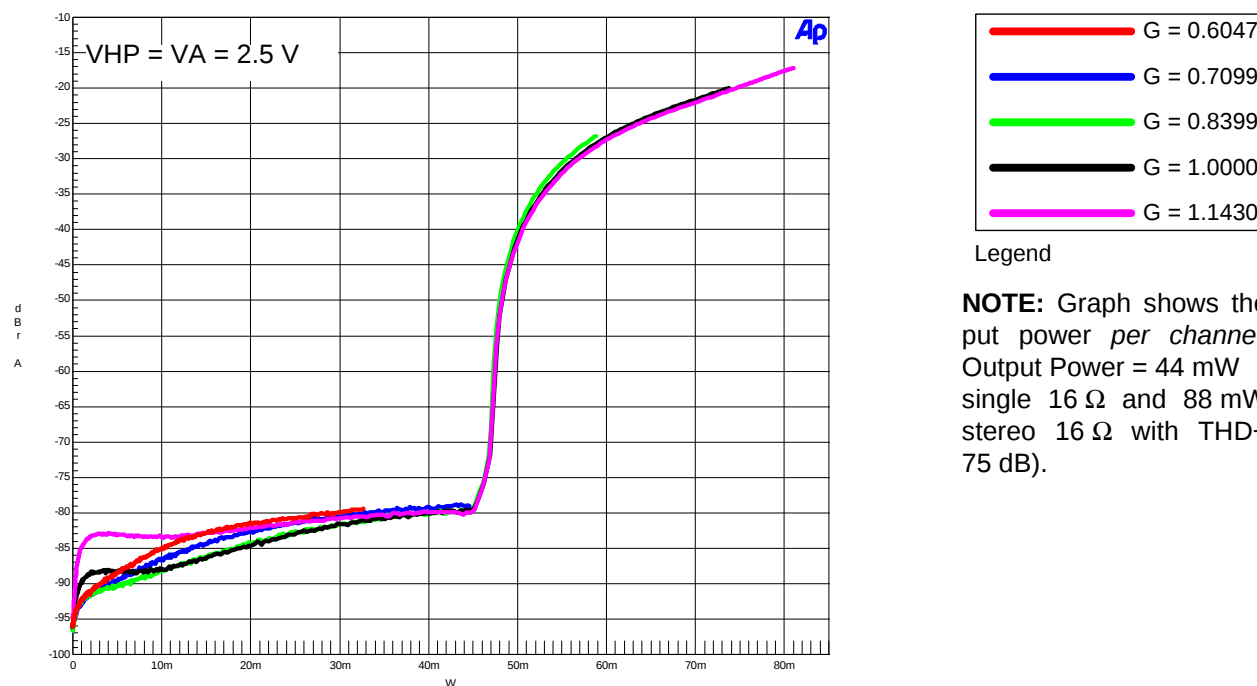
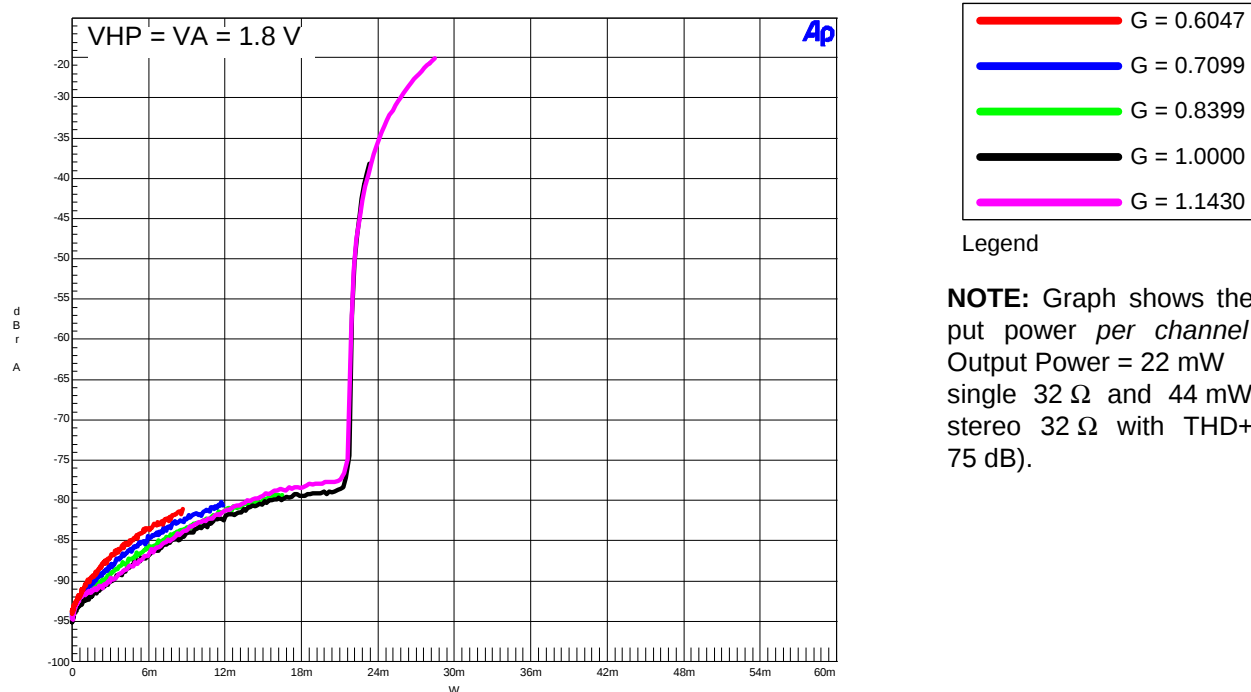
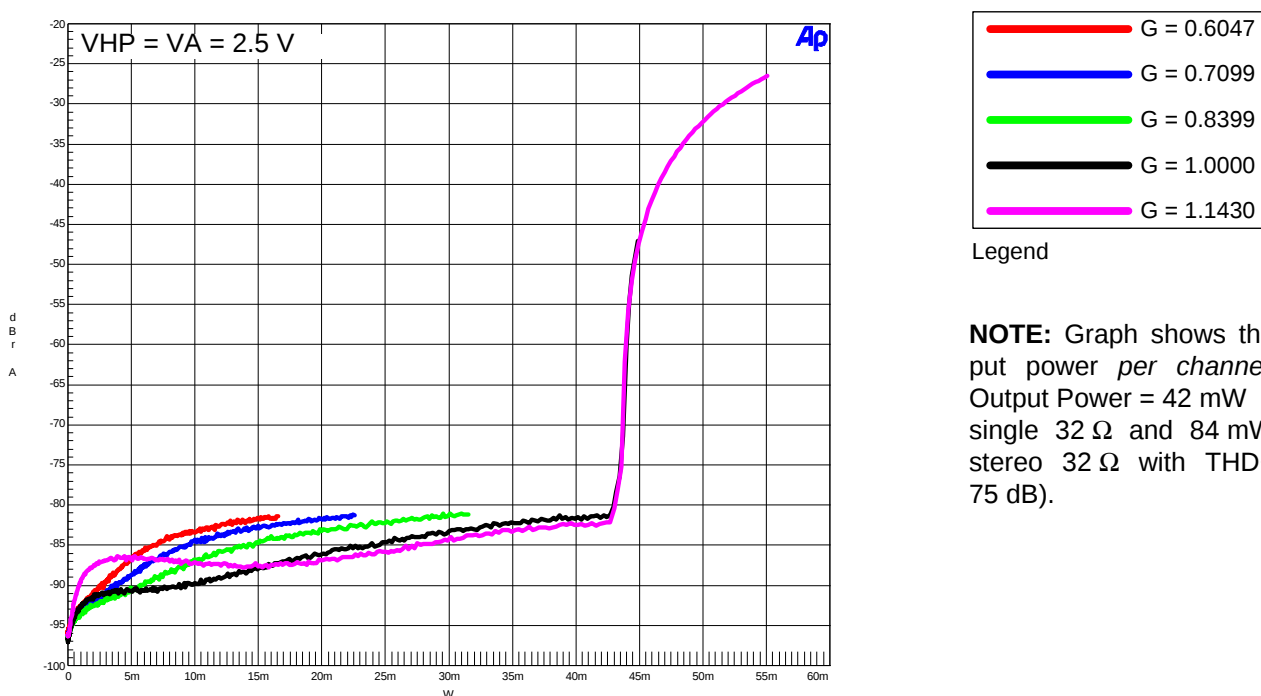


Figure 19. THD+N vs. Output Power per Channel at 2.5 V (16  $\Omega$  load)



**Figure 20. THD+N vs. Output Power per Channel at 1.8 V (32 Ω load)**



**Figure 21. THD+N vs. Output Power per Channel at 2.5 V (32 Ω load)**

## 9. EXAMPLE SYSTEM CLOCK FREQUENCIES \*The "MCLKDIV2" bit must be enabled.

### 9.1 Auto Detect Enabled

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 1024x      | 1536x   | 2048x*  | 3072x*  |
| 8                         | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 11.025                    | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 12                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 512x       | 768x    | 1024x*  | 1536x*  |
| 16                        | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 22.05                     | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 24                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 256x       | 384x    | 512x*   | 768x*   |
| 32                        | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 44.1                      | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 48                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 128x       | 192x    | 256x*   | 384x*   |
| 64                        | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 88.2                      | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 96                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

### 9.2 Auto Detect Disabled

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |        |         |         |         |         |
|---------------------------|------------|--------|---------|---------|---------|---------|
|                           | 512x       | 768x   | 1024x   | 1536x   | 2048x   | 3072x   |
| 8                         | -          | 6.1440 | 8.1920  | 12.2880 | 16.3840 | 24.5760 |
| 11.025                    | -          | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 12                        | 6.1440     | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |        |         |         |         |         |
|---------------------------|------------|--------|---------|---------|---------|---------|
|                           | 256x       | 384x   | 512x    | 768x    | 1024x   | 1536x   |
| 16                        | -          | 6.1440 | 8.1920  | 12.2880 | 16.3840 | 24.5760 |
| 22.05                     | -          | 8.4672 | 11.2896 | 16.9344 | 22.5792 | 33.8688 |
| 24                        | 6.1440     | 9.2160 | 12.2880 | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 256x       | 384x    | 512x    | 768x    |
| 32                        | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 44.1                      | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 48                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

| Sample Rate<br>LRCK (kHz) | MCLK (MHz) |         |         |         |
|---------------------------|------------|---------|---------|---------|
|                           | 128x       | 192x    | 256x    | 384x    |
| 64                        | 8.1920     | 12.2880 | 16.3840 | 24.5760 |
| 88.2                      | 11.2896    | 16.9344 | 22.5792 | 33.8688 |
| 96                        | 12.2880    | 18.4320 | 24.5760 | 36.8640 |

---

## 10. PCB LAYOUT CONSIDERATIONS

### 10.1 Power Supply, Grounding

As with any high-resolution converter, the CS43L22 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. [Figure 1 on page 9](#) shows the recommended power arrangements, with VA and VHP connected to clean supplies VD, which powers the digital circuitry, may be run from the system logic supply. Alternatively, VD may be powered from the analog supply via a ferrite bead. In this case, no additional devices should be powered from VD.

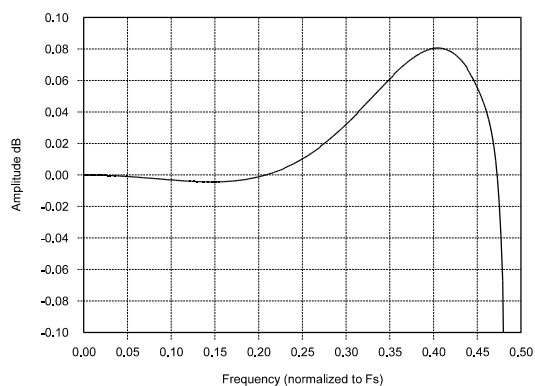
Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS43L22 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS43L22 to minimize inductance effects.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The VQ decoupling capacitors, particularly the 0.1  $\mu\text{F}$ , must be positioned to minimize the electrical path from AGND. The CDB43L22 evaluation board demonstrates the optimum layout and power supply arrangements.

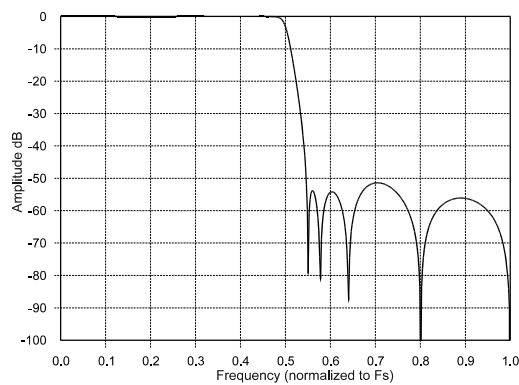
### 10.2 QFN Thermal Pad

The CS43L22 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CS43L22 evaluation board demonstrates the optimum thermal pad and via configuration.

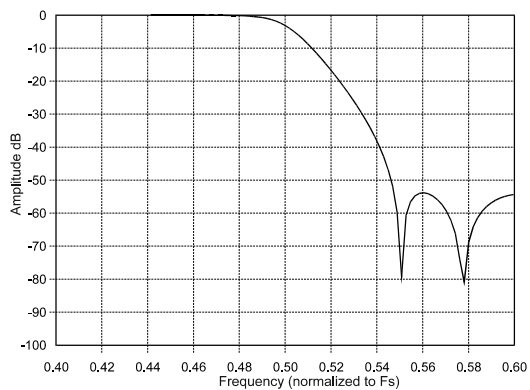
## 11.DIGITAL FILTER PLOTS



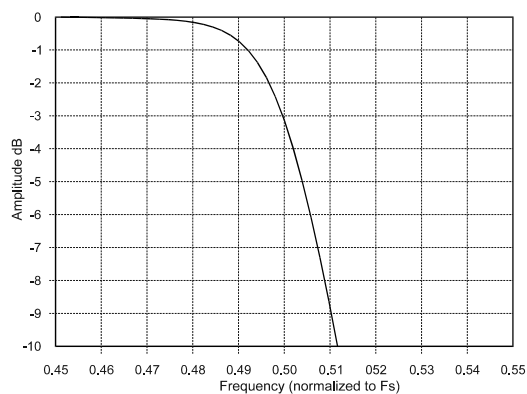
**Figure 22. Passband Ripple**



**Figure 23. Stopband**



**Figure 24. DAC Transition Band**



**Figure 25. Transition Band (Detail)**

---

## 12.PARAMETER DEFINITIONS

### Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

### Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

### Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

### Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

### Interchannel Gain Mismatch

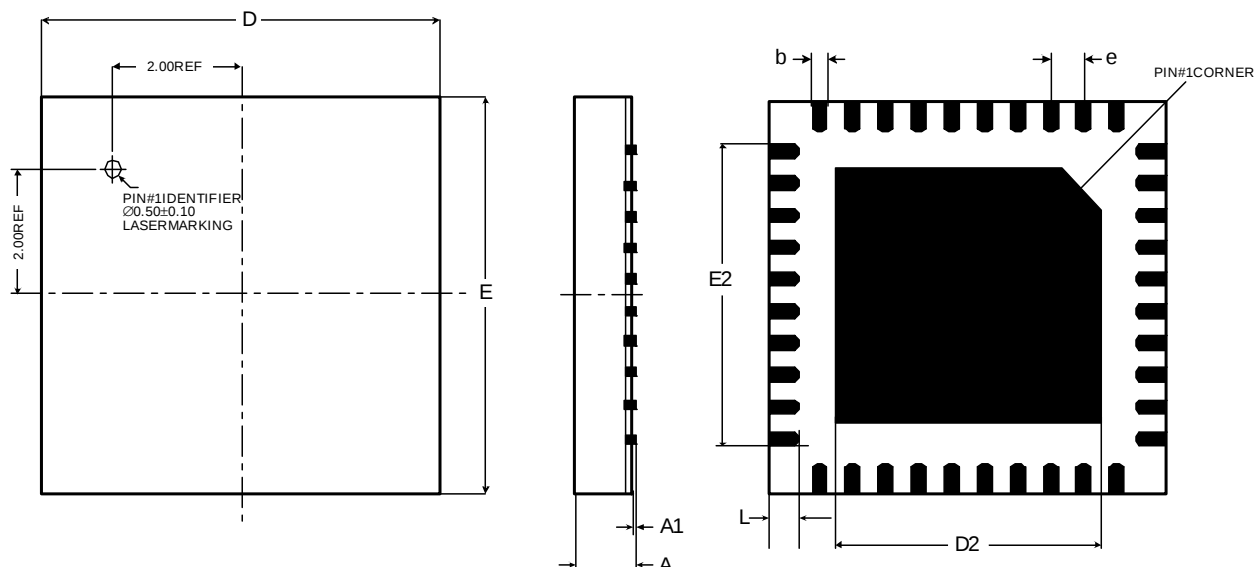
The gain difference between left and right channel pairs. Units in decibels.

### Gain Drift

The change in gain value with temperature. Units in ppm/°C.

## 13.PACKAGE DIMENSIONS

### 40L QFN (6 X 6 mm BODY) PACKAGE DRAWING



| DIM | INCHES     |        |        | MILLIMETERS |      |      | NOTE |
|-----|------------|--------|--------|-------------|------|------|------|
|     | MIN        | NOM    | MAX    | MIN         | NOM  | MAX  |      |
| A   | --         | --     | 0.0394 | --          | --   | 1.00 | 1    |
| A1  | 0.0000     | --     | 0.0020 | 0.00        | --   | 0.05 | 1    |
| b   | 0.0071     | 0.0091 | 0.0110 | 0.18        | 0.23 | 0.28 | 1,2  |
| D   | 0.2362 BSC |        |        | 6.00 BSC    |      |      | 1    |
| D2  | 0.1594     | 0.1614 | 0.1634 | 4.05        | 4.10 | 4.15 | 1    |
| E   | 0.2362 BSC |        |        | 6.00 BSC    |      |      | 1    |
| E2  | 0.1594     | 0.1614 | 0.1634 | 4.05        | 4.10 | 4.15 | 1    |
| e   | 0.0197 BSC |        |        | 0.50 BSC    |      |      | 1    |
| L   | 0.0118     | 0.0157 | 0.0197 | 0.30        | 0.40 | 0.50 | 1    |

#### JEDEC #: MO-220

Controlling Dimension is Millimeters.

1. Dimensioning and tolerance per ASME Y 14.5M-1995.
2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

## THERMAL CHARACTERISTICS

| Parameter                             |               | Symbol        | Min | Typ | Max | Units   |
|---------------------------------------|---------------|---------------|-----|-----|-----|---------|
| Junction to Ambient Thermal Impedance | 2 Layer Board | $\theta_{JA}$ | -   | 44  | -   | °C/Watt |
|                                       | 4 Layer Board | $\theta_{JA}$ | -   | 19  | -   | °C/Watt |

## 14.ORDERING INFORMATION

| Product  | Description                                                  | Package | Pb-Free | Grade      | Temp Range    | Container   | Order #      |
|----------|--------------------------------------------------------------|---------|---------|------------|---------------|-------------|--------------|
| CS43L22  | Low-Power Stereo DAC w/HP and Speaker Amps for Portable Apps | 40L-QFN | Yes     | Commercial | -40 to +85° C | Rail        | CS43L22-CNZ  |
|          |                                                              |         |         |            |               | Tape & Reel | CS43L22-CNZR |
| CDB43L22 | CS43L22 Evaluation Board                                     | -       | No      | -          | -             | -           | CDB43L22     |

## 15.REFERENCES

1. Philips Semiconductor, *The I<sup>2</sup>C-Bus Specification: Version 2.1*, January 2000.  
<http://www.semiconductors.philips.com>

## 16.REVISION HISTORY

| Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F2       | <p>Added AD0 characteristics to "I/O Pin Characteristics" on page 8.</p> <p>Added a description of the AD0 pin to "I<sup>2</sup>C Control" on page 33.</p> <p>Added AD0 detail to Figure 16. Control Port Timing, I<sup>2</sup>C Write on page 33 and Figure 17. Control Port Timing, I<sup>2</sup>C Read on page 33.</p> <p>Updated the first paragraph in "Register Quick Reference" on page 35 and "Register Description" on page 37 to allow for data sheet-specified control-writes to reserved registers.</p> <p>Updated Note 3 on page 11.</p> <p>Removed I<sup>2</sup>C address heading row from "Register Quick Reference" on page 35.</p> |

## Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.  
To find the one nearest you, go to [www.cirrus.com](http://www.cirrus.com).

### IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, indemnification, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, AUTOMOTIVE SAFETY OR SECURITY DEVICES, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

I<sup>2</sup>C is a trademark of Philips Semiconductor.