Single Phase PWM Controller with Light Load Efficiency Optimization

General Description

The RT8123A is a high efficiency single phase synchronous buck DC/DC controller with 5V/12V supply voltage. At light load condition, the IC automatically operates in the pulse skip mode to reduce switching frequency so as to improve conversion efficiency. As the load current increases, the RT8123A leaves the pulse skip mode and operates in the continuous conduction mode with fixed-frequency PWM.

The RT8123A has embedded MOSFET gate driver with high driving capability, supporting driving voltage up to 12V for high output current application. Other features include power good indication, external error-amp compensation, over voltage protection, over current protection,, enable/ disable control and internal Soft-Start. With the above functions, the IC provides customers a cost-effective solution for high efficiency power conversion. The RT8123A is available in a WQFN-16L 3x3 package.

Ordering Information

RT8123A□□

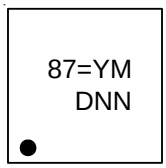
- Package Type
  QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free))

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



87= : Product Code

YMDNN : Date Code

Features

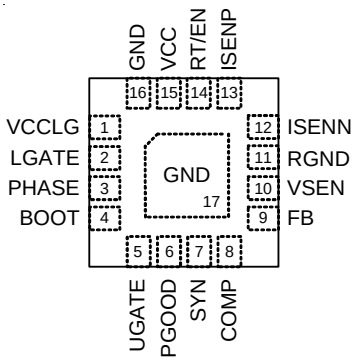
- **High Performance Operational Error Amplifier**
- **Internal Soft-Start/Stop**
- **±0.5% Internal Voltage Accuracy, 0.8V Voltage Reference**
- **OCP accuracy, Four Re-entry Times Before Latch**
- **"Lossless" Differential Inductor Current Sensing**
- **Internal High Precision Current Sensing Amplifier**
- **Oscillator Frequency Range of 100kHz – 1000kHz**
- **20ns Adaptive FET Non-Overlap Time of Internal Gate Driver**
- **5V to 12V Operation**
- **Support VIN from 1.5V to 19V**
- **VOUT from 0.8V to 3.3V (5V with 12 VCC)**
- **Chip Enable Through RT/EN pin**
- **Latched Over Voltage Protection (OVP)**
- **Internally Fixed OCP Threshold**
- **Guaranteed Startup Into Pre-Charged Loads**
- **Thermally Compensated Current Monitoring**
- **Thermal Shutdown Protection**
- **Integrated MOSFET Drivers**
- **Integrated BOOST Diode with Internal R_{BST} = 2.2Ω**
- **Automatic Power Saving Mode to Maximize Efficiency During Light Load Operation**
- **Sync Function**
- **Remote Ground Sensing**

Applications

- Memory and Termination Supply
- Subsystem Power Supply (MCH, IOCH, PCI)
- CPU and DSP Power Supply
- Distributed Power Supply
- General DC/DC Converter

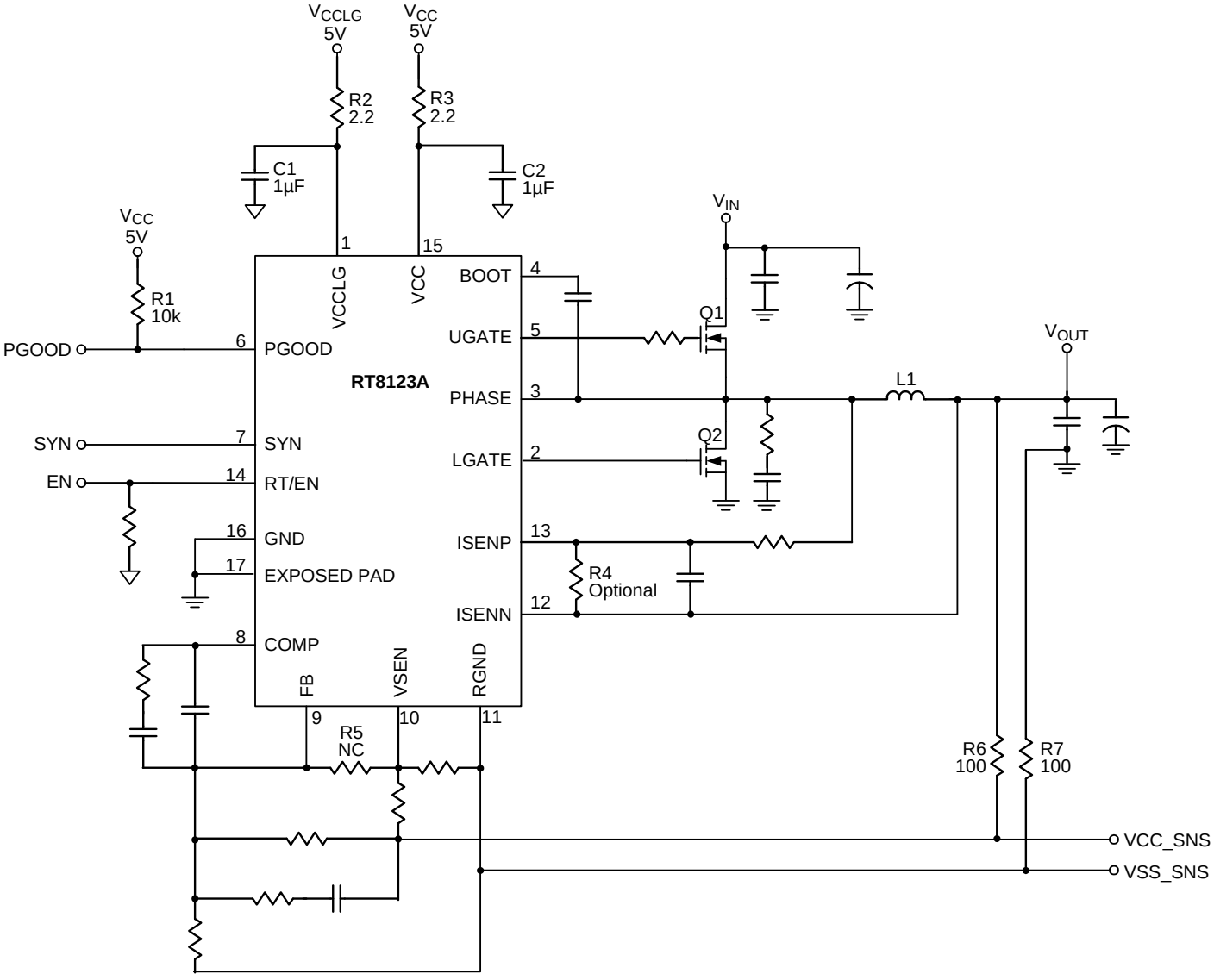
Pin Configurations

(TOP VIEW)



WQFN-16L 3x3

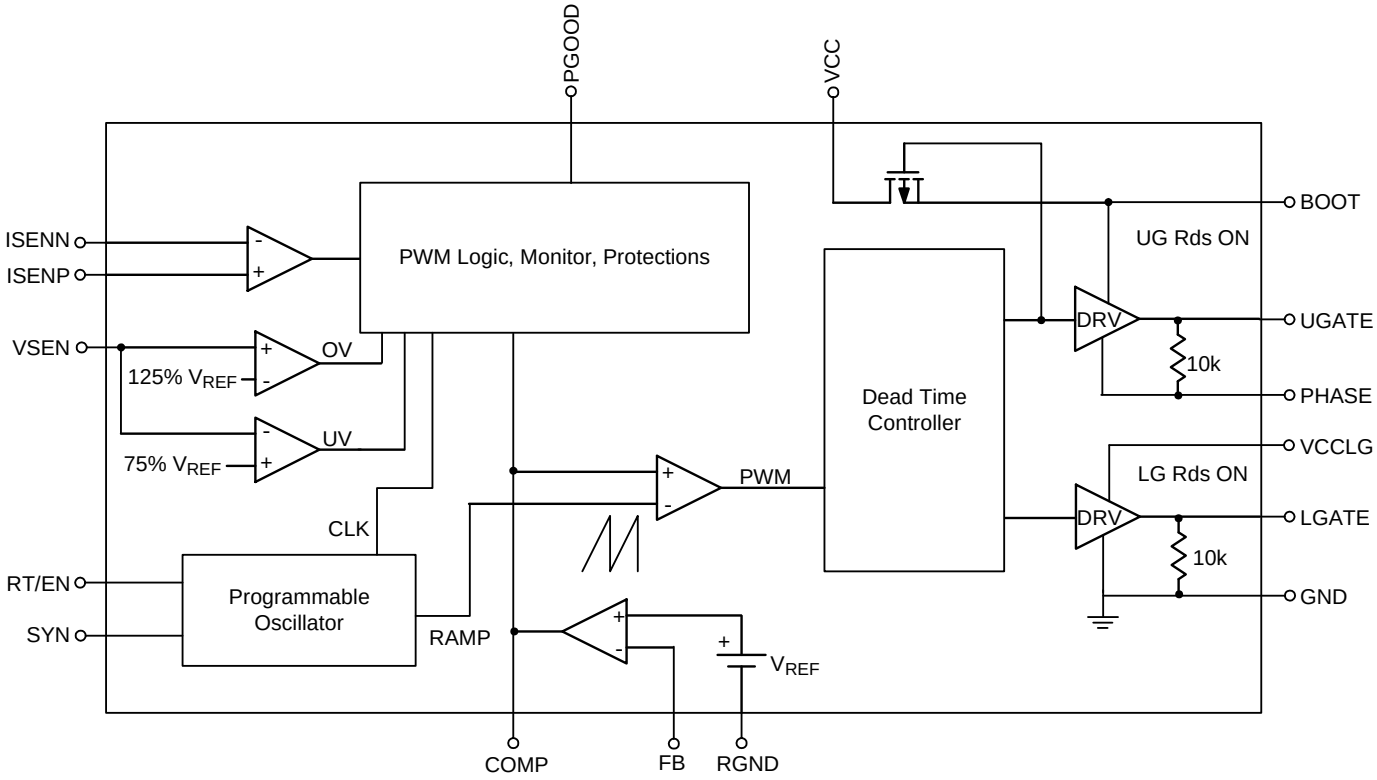
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCCLG	Low-Side Driver Section Power Supply. Operative voltage is 5V to 12V bus. Filter with 1μF MLCC to GND.
2	LGATE	Low-Side Driver Output. Connect directly to the low-side MOSFET gate. A small series resistor can be useful to reduce dissipated power especially in high frequency applications.
3	PHASE	High-Side Driver Return Path. Connect to the high-side MOSFET source. This pin is also monitored for the adaptive dead-time management.
4	BOOT	High-Side Driver Supply. This pin supplies the high-side floating driver. Connect through the C_{BOOT} capacitor to the PHASE pin. The pin is internally connected through a boot diode to the VCCLG pin. A 2.2Ω series resistor is also provided.
5	UGATE	High-Side Driver Output. Connect to high-side MOSFET gate. A small series resistor may help in reducing the PHASE pin negative spike as well as cooling the device.
6	PGOOD	Power Good. It is an open-drain output set free after SS as long as the output voltage monitored through VSEN is within specifications. If not used it can be left floating.
7	SYN	Synchronization Pin. The controller synchronizes on the falling edge of a square wave provided to this pin. Short to GND if not used.
8	COMP	Error Amplifier Output. Connect with an RF-CF to FB. The device cannot be disabled by grounding this pin.
9	FB	Error Amplifier Inverting Input. Connect with a resistor RFB to VSEN and with an RF-CF to COMP.
10	VSEN	Output Voltage Monitor. It manages OVP and UVP protections and PGOOD. Connect to the positive side of the load for remote sensing.
11	RGND	Remote Ground Sense. Connect to the negative side of the load for remote sensing.
12	ISENN	Current Sense Negative Input. Connect to the output-side of the main inductor.
13	ISENP	Current Sense Positive Input. Connect through an R-C filter to the phase-side of the main inductor.
14	RT/EN	Internally Set to 1.24V, It Allows Programming the Switching Frequency f_{SW} of The Device. Switching frequency can be increased according to the resistor connected to GND with a gain of 10kHz/μA. If floating, the switching frequency is 200kHz.
15	VCC	Device Power Supply. The embedded bootstrap diode is internally connected to this pin. Operative voltage is 5V to 12V bus. Filter with 1μF MLCC to GND.
16	GND	All Internal References, Logic and Driver Return Path are Referenced to this Pin. Connect to the PCB GND ground plane and filter to VCC and VCCLG.
17 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- VCC, VCCLG to GND ---------- –0.3V to 15V
- BOOT to GND
  - DC ---------- –0.3V to 40V
  - < 100ns ---------- –0.3V to 45V
- BOOT to PHASE
  - DC ---------- –0.3V to 15V
  - < 100ns ---------- –0.3V to 20V
- PHASE to GND
  - DC ---------- –5V to 25V
  - < –100ns ---------- –10V to 30V
- RGND to GND ---------- –0.7V to 0.7V
- UGATE to GND
  - DC ---------- –0.3V to 40V
  - < 100ns ---------- –10V to 45V
- UGATE to PHASE
  - DC ---------- –0.3V to 15V
  - < –100ns ---------- –5V to 20V
- LGATE to GND
  - DC ---------- –0.3V to 15V
  - < –100ns ---------- –5V to 20V
- ISENP, ISENN to GND ---------- –0.3V to 6.5V
- Other Input, Output or I/O Voltage ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN-16L 3x3 ---------- 3.33W
- Package Thermal Resistance (Note 2)
  - WQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 1kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 13.2V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = V_{CCLG} = 5V to 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Operating						
VCC, VCCLG Bias Voltage	V_{CC}, V_{CCLG}		4.5	--	13.2	V
Supply Current	I_{CC}	UGATE, LGATE open	--	--	5	mA
	I_{CCLG}	UGATE, LGATE open	--	3.5	5	
Shutdown Current	I_{CC_SHDN}	RT = GND	--	--	400	μA
	I_{CCLG_SHDN}	RT = GND	--	--	200	
POR Threshold	V_{CC_th}	VCC Rising	--	--	4.5	V
POR Hysteresis	V_{CC_hys}		--	0.3	--	V
POR Threshold	V_{CCLG_th}	VCCLG Rising	--	--	4.2	V
POR Hysteresis	V_{CCLG_hys}		--	0.15	--	V
Error Amplifier COMP						
Open Loop DC Gain	ADC	(Note 5)	--	80	--	dB
Gain Bandwidth	GBW	(Note 5)	--	15	--	MHz
Slew Rate	I_{EA_SLEW}	COMP with 100pF to ground, (Note 5)	--	8	--	V/μs
VREF						
Internal Reference Voltage			0.796	0.8	0.804	V
Oscillator						
Frequency	f_{OSC}	RT/EN = Open	180	200	220	kHz
OSC Gain		Note 5	--	10	--	kHz/μA
Disable OSC		RT/EN Falling	--	--	0.75	V
Modulators						
Minimum On-time			--	90	--	ns
Minimum Off-time			250	350	450	ns
Magnitude of the PWM Ramp		RT/EN = Open	--	1.5	--	V
Maximum Duty cycle		RT/EN = Open	--	95	--	%
ASM frequency			25	--	--	kHz
Soft-Start						
Soft-Start Time			--	5.12	--	ms
Soft-Off						
VOUT Discharge Resistor		RT/EN ties to ground	--	20	--	Ω
Over Current Protection						
OC Threshold	V_{OC_th}	ISENP-ISENN; 4x Masking	17	20	23	mV
		ISENP-ISENN; Immediate Action	--	30	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Synchronization Pin						
Synchronization Input	V_{IL}		--	--	1	V
	V_{IH}		2.5	--	--	
Protection and PGOOD						
Output Voltage		Sink 1mA	--	--	0.4	V
OVP Threshold	V_{OV}	VSEN Rising	117	125	130	%
		Un-latch, VSEN Falling	40	50	60	
UVP Threshold	V_{UV}	VSEN Falling	70	75	80	%
PGOOD High Delay		Note 5	--	--	50	μs
PGOOD Low Delay		Note 5	--	--	1	μs
Driver						
UGATE Driver Source	$R_{UGATEsr}$	I_{UGATE} = 150mA, V_{CC} = 12V	--	2.5	5	Ω
UGATE Driver Sink	$R_{UGATEsk}$	V_{UGATE} – V_{PHASE} = 0.1V, V_{CC} = 12V	--	2	2.5	Ω
LGATE Driver Source	$R_{LGATEsr}$	I_{LGATE} = 150mA, V_{CCLG} = 12V	--	2	3	Ω
LGATE Driver Sink	$R_{LGATEsk}$	V_{LGATE} = 0.1V, V_{CCLG} = 12V	--	1	1.5	Ω
Dead time		From LGATE falling to UGATE rising	--	30	--	ns
		From UGATE falling to LGATE rising	--	30		ns
Boost Switch Ron	R_{BOOT}	VCC to BOOT, I_{BOOT} = 10mA, V_{CC} = 12V	--	40	80	Ω
Thermal Shutdown						
Thermal Shutdown	T_{SD}		150	180	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	50	--	°C

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

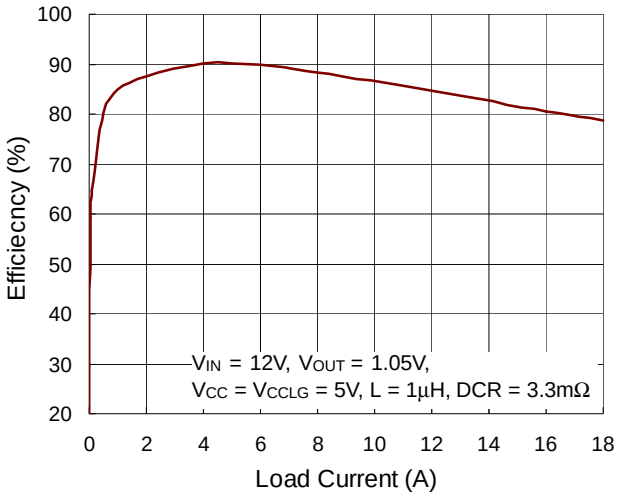
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

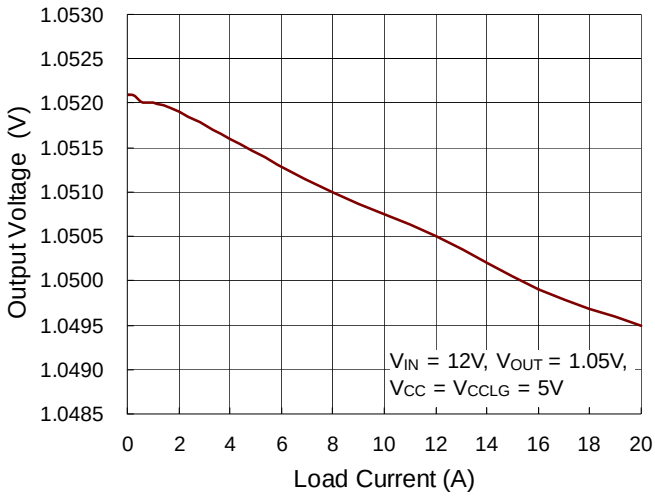
Note 5. Guaranteed by design.

Typical Operating Characteristics

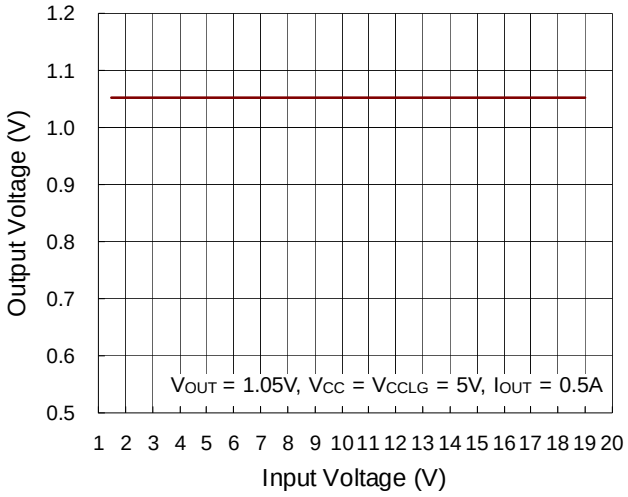
Efficiency vs. Load Current



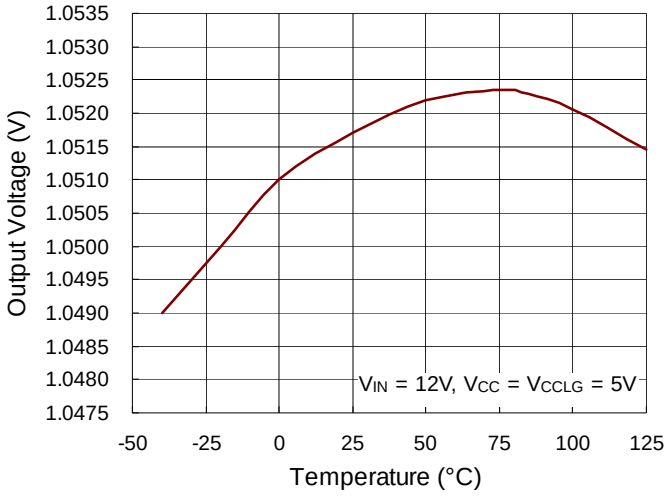
Output Voltage vs. Load Current



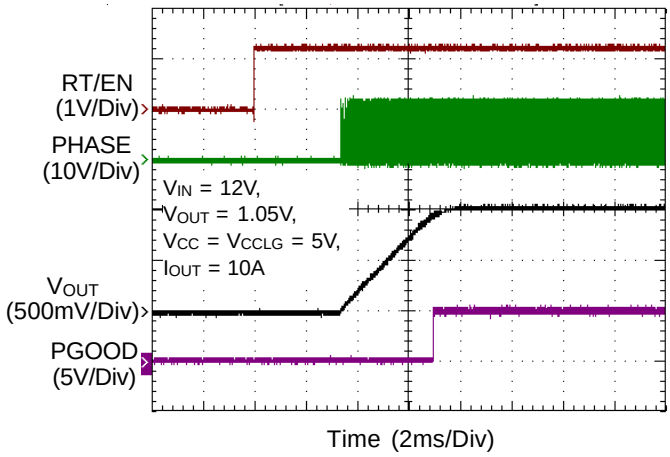
Output Voltage vs. Input Voltage



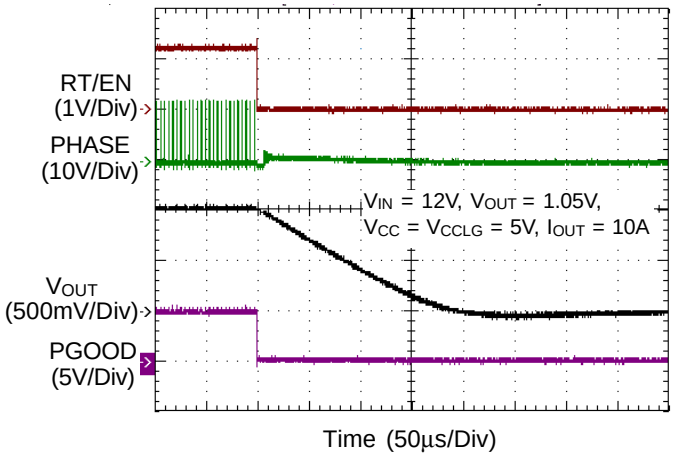
Output Voltage vs. Temperature



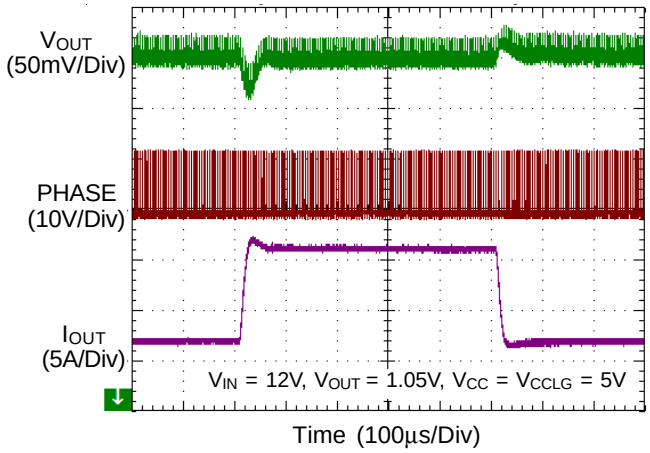
Power On from RT/EN



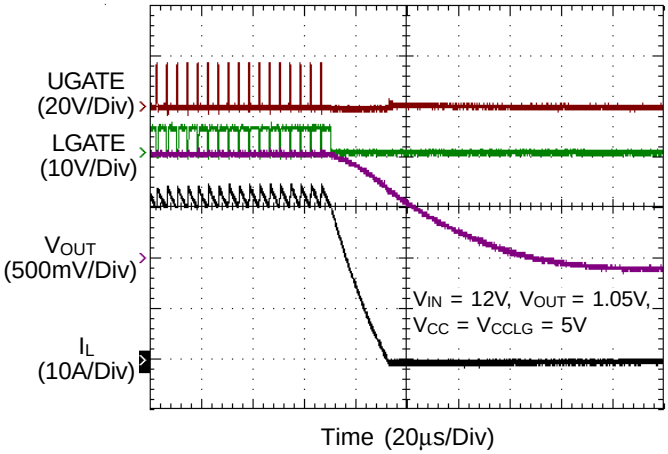
Power Off from RT/EN



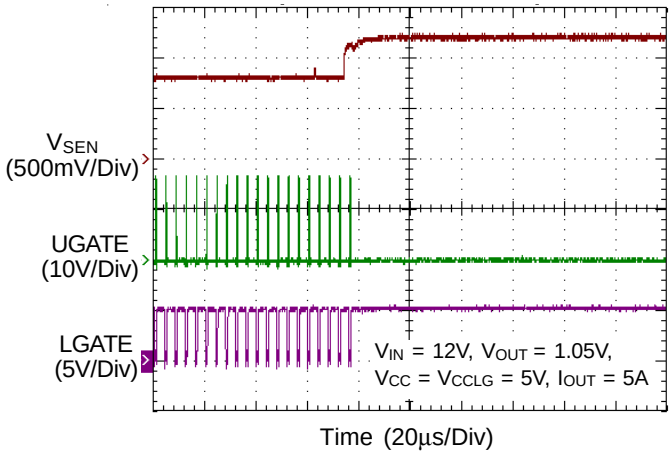
Load Transient Response



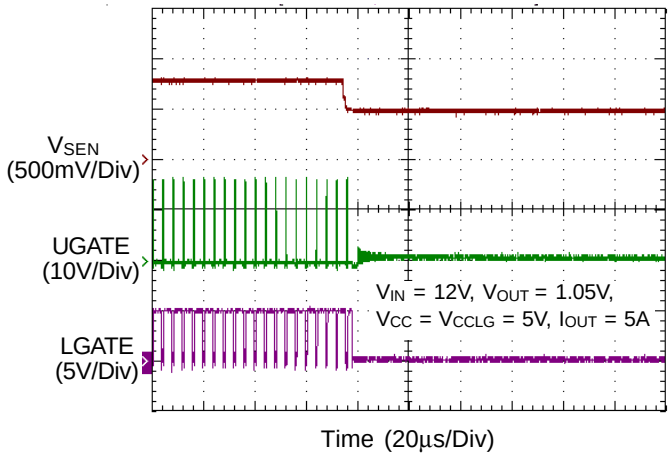
Over Current Protection



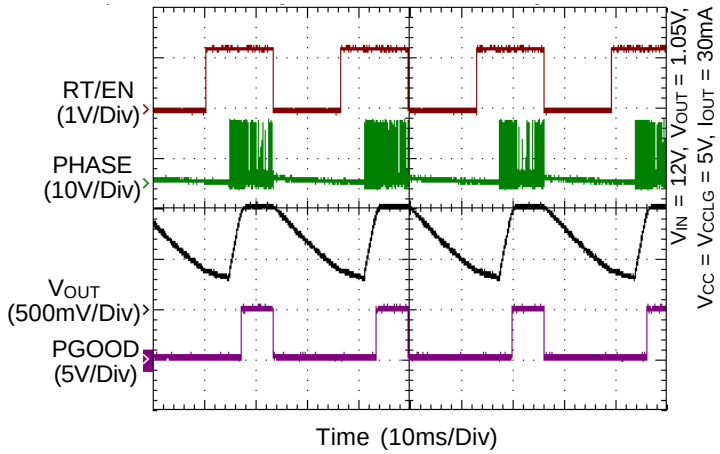
Over Voltage Protection



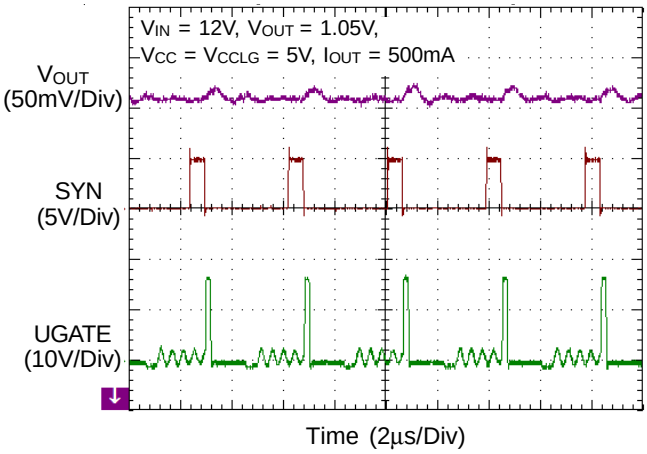
Under Voltage Protection



Pre-Bias Startup



Synchronization



Application Information

Supply Voltage and Power On Reset

The RT8123A requires an external bias supply for VCC and VCCLG. VCC powers the high-side integrated MOSFET driver and the control circuit. VCCLG biases the low-side integrated MOSFET driver. It's preferred and recommended to add a resistor (2.2 to 10Ω) between VCC and VCCLG pins and decoupling capacitors on both pins to ground.

The Power On Reset (POR) circuit monitors the supply voltage at VCC and VCCLG pins. If VCC and VCCLG are both exceed the POR rising threshold voltage, the controller is reset and preparing the PWM for operation. If VCC and VCCLG fall below the POR falling threshold during normal operation, all MOSFETs stop switching. The POR rising and falling threshold has a hysteresis to prevent noise caused reset.

Soft-Start

The RT8123A provides internal soft-start function to prevent the large inrush current and output voltage overshoot when the converter starts up. The Soft-Start (SS) automatically begins once the VCC, VCCLG both exceeds their POR thresholds and RT/EN pin is set free. During Soft-Start, the internal Soft-Start capacitor is charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the feedback voltage at the FB pin, causing PWM pulse width increasing slowly to reduce the output surge current. The internal 0.8V reference takes over the loop control once the internal ramping up voltage is higher than 0.8V. The Soft-Start ramp will wait a fixed delay time at Soft-Start beginning, and the PGOOD will indicate high after 30us delay time once the output voltage is within PGOOD window (±10 % of reference voltage 0.8V).

A power on sequence should be concerned. When RT/EN is set free with VCC/VCCLG but VIN is not present, the VOUT voltage cannot be generated and the COMP will be pulled high during UV blanking time then into hiccup mode. Once VCC/VCCLG both exceeds POR threshold and VIN comes in the Soft-Start period where COMP is pulled high, Soft-Start begins but OCP or OVP may be triggered fault latch to cause power on failed. For successful power up, to make sure the correct sequence of VIN, VCC/VCCLG and RT/EN is needed.

Power Good Output

The PGOOD is an open-drain type output and requires a pull-up resistor. PGOOD is actively held low in soft-start, shutdown and if the OVP or UVP is triggered. It is released when the voltage on the VSEN pin within ±10% of reference voltage (0.8V).

Switching Frequency

Higher PWM switching frequency enhances better transient response and smaller component size, trading off efficiency due to higher switching losses.

The switching frequency can be programmed by a resistor (R_{RT}) which connecting between RT/EN pin and ground. Figure 1 shows the typical operation frequency vs. R_{RT} for quick reference.

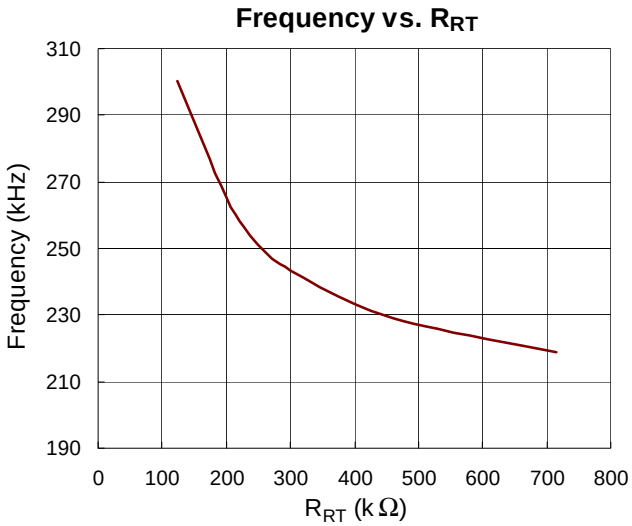


Figure 1. Operation Frequency vs. R_{RT}

Synchronization Function

The RT8123A provides the synchronization function that allows the different converters can share the same input filter for reducing the input RMS current and reducing the total input capacitors.

Synchronization can be programmed through the SYN pin by external PWM signal with a fixed delay time such as PHASE, UGATE etc. The UGATE of RT8123A will track

the falling edge of external PWM signal on SYN pin, and the synchronize frequency range is 100% to 130% of RT8123A's setting frequency.

Over Voltage Protection (OVP)

The output voltage can be continuously monitored for over voltage. If the voltage on VSEN pin exceeds than OVP threshold (125% of V_{REF}), the over voltage protection is triggered and the LGATE low-side gate driver is forced high. This activates the low-side MOSFET switch, which rapidly discharges the output capacitor and pulls the input voltage downward. When the VSEN pin voltage falls below 0.4V, LGATE will go low to stop the discharge.

The RT8123A is latched once OVP is triggered and can only be released by toggling VCC, VCCLG or RT/EN. There is a fixed delay time built into the over voltage protection circuit to prevent false transition.

Pre-OVP Function

When RT/EN signal is low, the pre-OVP circuit senses the voltage on VSEN pin. Once the VSEN voltage exceeds Pre-OVP threshold, LGATE will be forced high to discharge the output voltage for protecting the load. Pre-OVP protection is not latch mode. Once the VSEN voltage is less than Pre-OVP threshold, LGATE will go low to stop discharge immediately.

Under Voltage Protection (UVP)

The output voltage can be continuously monitored for under voltage. If the voltage on VSEN pin is less than 75% of V_{REF}, under voltage protection is triggered, then both UGATE and LGATE gate drivers are forced low. The UVP will be ignored during Soft-Start period. Toggle VCC, VCCLG or RT/EN to reset the UVP fault latch and restart the controller.

Over Current Protection (OCP)

The RT8123A uses continuous inductor current sensing to make the controller less noise sensitive. Low offset amplifier is used for over current detection. The ISENP and ISENN denote the positive and negative input of the current sense amplifier.

The RT8123A observes the differential voltage V_X, across the ISENP and ISENN pins for inductor current information.

There are two over current thresholds (V_{OC_th1} = 20mV and V_{OC_th2} = 30mV) designed for different over current condition. If the differential voltage across ISENP and ISENN (V_X) exceeds than 20mV (but below than 30mV) for four switching cycles, V_{OC_th1} will be triggered. Both UGATE and LGATE gate drivers are forced low to turn off MOSFETs and latched. Once the differential voltage V_X exceeds than 30mV, V_{OC_th2} will be triggered. Both UGATE and LGATE gate drivers are forced low and latched immediately.

The value of current sensing network is calculated as below formula for meet inductor time constant.

$$\frac{L}{DCR} = (R_{CS1} \,//\, R_{CS2}) \times C$$

Therefore, the OCP thresholds can be calculated as,

$$V_{OC\_th1} = \frac{20mV}{DCR} \times \frac{R_{CS1} + R_{CS2}}{R_{CS2}}$$

$$V_{OC\_th2} = \frac{30mV}{DCR} \times \frac{R_{CS1} + R_{CS2}}{R_{CS2}}$$

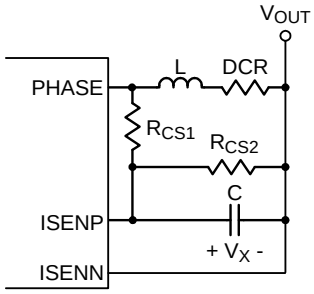


Figure 2. Current Sensing Network

Output Voltage Setting

The RT8123A allows the output voltage of the DC/DC converter to be adjusted from 0.8V to 80% of VIN via an external resistor divider as shown in Figure 3. It will try to maintain the feedback pin at internal reference voltage.

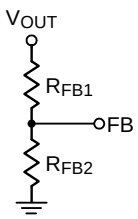


Figure 3. Output Voltage Setting

The output voltage can be set according to :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

Compensation Network Design

The RT8123A is a voltage mode synchronous Buck controller. To compensate a typical voltage mode buck converter, there are two ordinary compensation schemes, well known as type-II compensator and type-III compensator. The choice of using type-II or type-III compensator will be up to platform designers, and the main concern will be the position of the capacitor ESR zero and mid-frequency to high frequency gain boost. Typically, the ESR zero of output capacitor will tend to stabilize the effect of output LC double poles, hence the position of the output capacitor ESR zero in frequency domain may influence the design of voltage loop compensation. If $f_{Z(ESR)}$ is < $1/2f_C$, where f_C denotes 0dB crossing frequency, type-II compensation will be sufficient for voltage stability. If $f_{Z(ESR)}$ is > $1/2f_C$ (or higher gain and phase margin is required at mid frequency to high-frequency), then type-III compensation may be a better solution for voltage loop compensation.

The frequency of the double-pole is determined as follows.

$$f_{P(LC)} = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

The frequency of the ESR zero is determined as follows.

$$f_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

A typical type-II compensation network is shown in Figure 4.

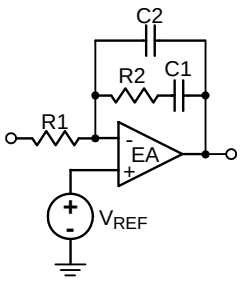


Figure 4. Type-II Compensation Network

After determining the phase margin at crossover frequency, the position of zero and pole produced by type-II compensation network, F_{Z1} and F_{P2}, can then be determined. The bode plot of type-II compensation is shown in Figure 5.

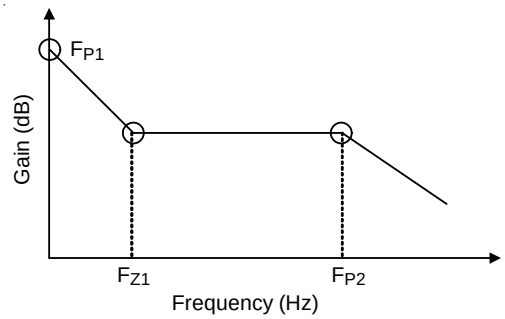


Figure 5. Bode Plot of the Type-II Compensation

The frequencies of poles and zero are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Determining the 0dB crossing frequency (f_C, control loop bandwidth) is the first step of compensator design. Usually, the f_C is set to 0.1 to 0.3 times of the switching frequency. The second step is to calculate the open loop modulator gain and find out the gain loss at f_C. The third step is to design a compensator gain that can compensate the modulator gain loss at f_C. The final step is to design f_{Z1} and f_{P2} to allow the loop sufficient phase margin. f_{Z1} is designed to cancel one of the double-pole of modulator. Usually, place f_{Z1} before $f_{P(LC)}$. f_{P2} is usually placed below the switching frequency (typically, 0.5 to 1 times of the switching frequency) to cancel high frequency noise.

A typical type-III compensation contains two zeros and two poles, where the extra one zero and one pole compared with type-II compensation are added for stabilizing the system when ESR zero is relatively far from LC double-pole in frequency domain. Figure 6 and Figure 7 show the typical circuit and bode plot of the type-III compensation.

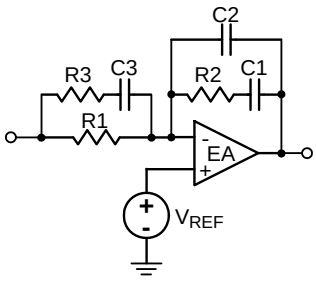


Figure 6. Type-III Compensation Network

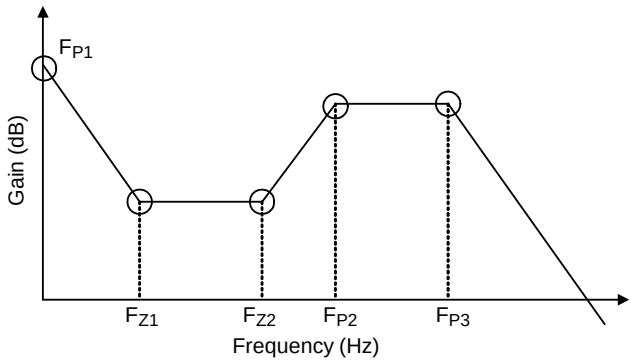


Figure 7. Bode Plot of the Type-III Compensation

A well-designed compensator regulates the output voltage according to the reference voltage V_{REF} with fast transient response and good stability. In order to achieve fast transient response and accurate output regulation, an adequate compensator design is necessary. The goal of the compensation network is to provide adequate phase margin (usually greater than 45°) and the highest bandwidth (0dB crossing frequency, f_C) possible. It is also recommended to manipulate the loop frequency response such that its gain crosses 0dB with a slope of −20dB/dec. According to Figure 7, the frequencies of poles and zeros are :

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3}$$

$$f_{P1} = 0$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

$$f_{P3} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

Generally, f_{Z1} and f_{Z2} are designed to cancel the double-pole of the modulator. Usually, place f_{Z1} at a fraction of $f_{P(LC)}$, and place f_{Z2} at $f_{P(LC)}$. f_{P2} is usually placed at $f_{Z(ESR)}$ to cancel the ESR zero, and f_{P3} is placed below the switching frequency to cancel high frequency noise.

Inductor Selection

The inductor plays an importance role in step-down converters because it stores the energy from the input power rail and then releases the energy to the load. From the viewpoint of efficiency, the dc resistance (DCR) of the inductor should be as small as possible to minimize the conduction loss. In addition, the inductor covers a significant proportion of the board space, so its size is also important. Low profile inductors can save board space especially when the height has a limitation. However, low DCR and low profile inductors are usually cost ineffective. Additionally, larger inductance results in lower ripple current, which translates into the lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is chosen such that the ripple current ranges between 20% to 40% of the full load current. The inductance can be calculated using the following equation :

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

where k is the ratio between inductor ripple current and rated output current.

Input Capacitor Selection

Voltage rating and current rating are the key parameters when selecting an input capacitor. Conservatively speaking, an input capacitor should have a voltage rating 1.5 times greater than the maximum input voltage to be considered a safe design. The input capacitor is used to supply the input RMS current, which can be approximately calculated using the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select a proper capacitor for the RMS current rating. Using more than one capacitor with low Equivalent Series Resistance (ESR) in parallel to form a capacitor bank is a good design. Placing the ceramic capacitor close to the drain of the high-side MOSFET can also be helpful in reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the buck topology. In steady state condition, the ripple current flowing into/out of the capacitor results in voltage ripple. The output voltage ripples contains two components, ΔV_{OUT_ESR} and ΔV_{OUT_C}.

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$$

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

When load transient occurs, the output capacitor supplies the load current before controller can respond. Therefore, the ESR will dominate the output voltage sag during load transient. The output voltage sag can be calculated using the following equation :

$$V_{OUT\_SAG} = ESR \times \Delta V_{OUT}$$

For a given output voltage sag specification, the ESR value can be determined.

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient.

Therefore ESL contributes to part of the voltage sag. Using a capacitor with low ESL will obtain better transient performance. Generally, using several capacitors connected in parallel will also have better transient performance than just one single capacitor with the same total ESR.

Unlike electrolytic capacitors, the ceramic capacitor has relatively low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, it is suggested to use a mixed combination of electrolytic capacitor and ceramic capacitor for achieving better transient performance.

MOSFET Selection

The majority of power loss in the step-down power conversion is due to the loss in the power MOSFETs. For low voltage high current applications, the duty cycle of the high-side MOSFET is small. Therefore, the switching loss of the high-side MOSFET is of concern. Power MOSFETs with lower total gate charge are preferred in such kind of application. However, the small duty cycle means the low-side MOSFET is on for most of the switching cycle. Therefore, the conduction loss tends to dominate the total power loss of the converter. To improve the overall efficiency, MOSFETs with low $R_{DS(ON)}$ are preferred in the circuit design. In some cases, more than one MOSFET are connected in parallel to further decrease the on-state resistance. However, this depends on the low-side MOSFET driver capability and the budget.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-16L 3x3 packages, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (30°C/W) = 3.33W for WQFN-16L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

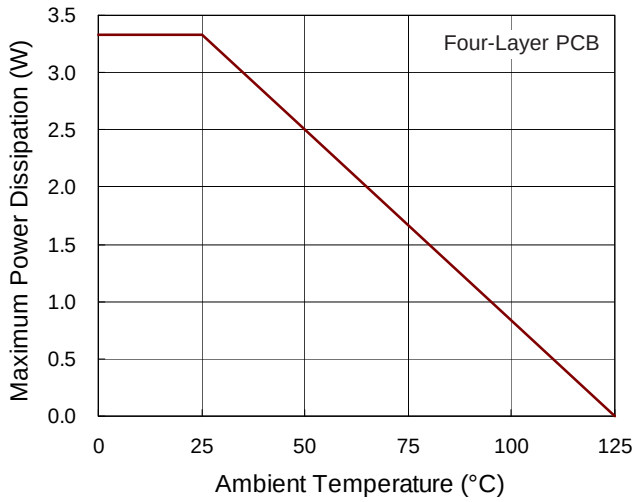
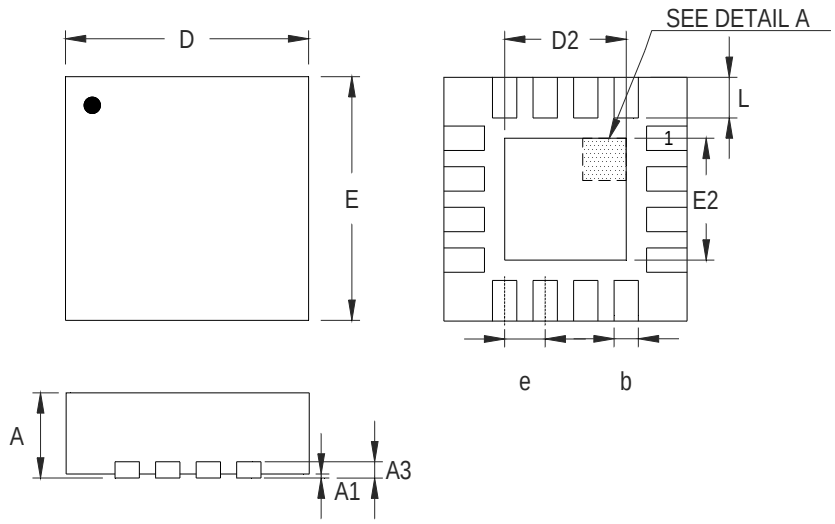
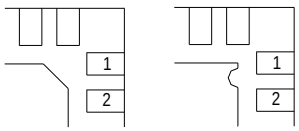


Figure 8. Derating Curve of Maximum Power Dissipation

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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