MP2663

5.2V System, 500mA, I²C-Controlled Battery Charger with Power Path Management for Single-Cell Li-ion Battery

DESCRIPTION

The MP2663 is a highly integrated, single-cell Li-ion/Li-polymer battery charger with system power path management for space-limited, portable applications. The MP2663 uses input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger features pre-charge, constant current (CC) and constant voltage (CV) regulation, charge termination, and charge status.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2663 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged by excessively high current. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold, which prevents the Li-ion battery from being over-discharged. An integrated I²C control interface allows the MP2663 to program the charging parameters, such as input current limit, input voltage regulation limit, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2663 is available in a 9-pin 1.55mmx1.55mm WLCSP package.

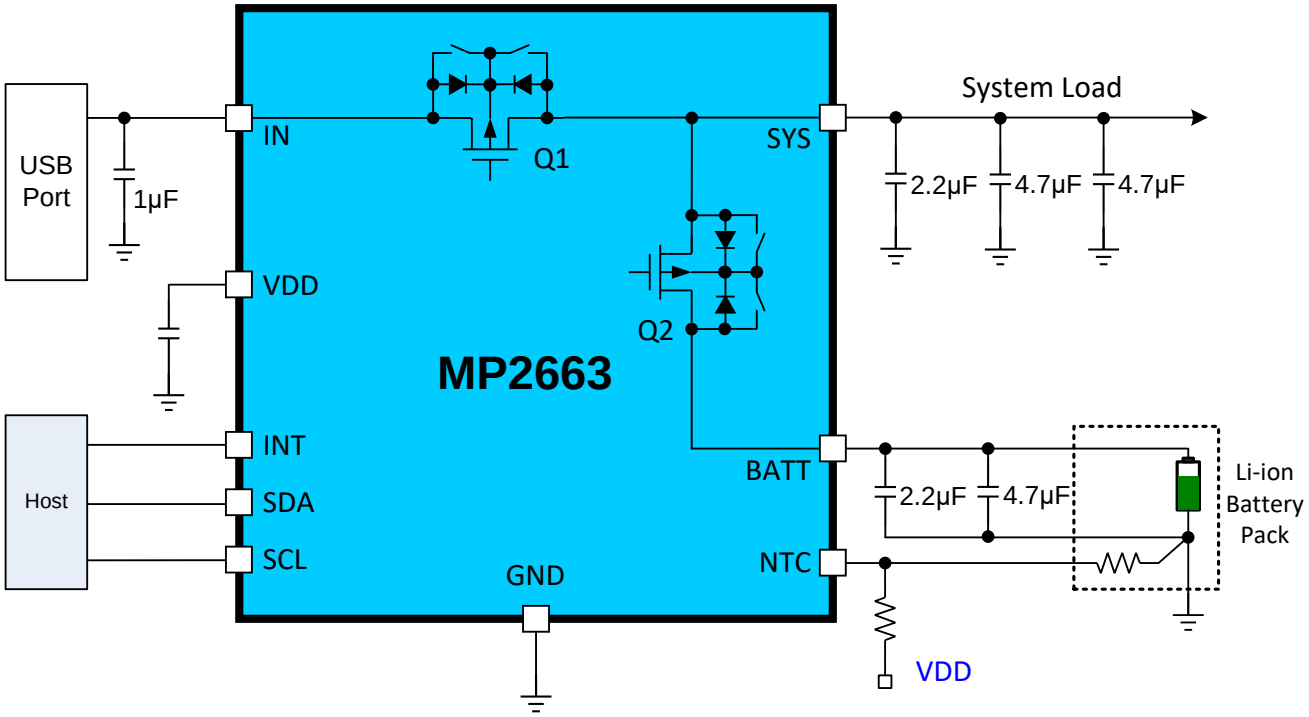
FEATURES

- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I²C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (OTP)
- Shipping Mode via Manual Function
- Built-In Battery Disconnection Function
- Thermal Limiting Regulation On-Chip
- Available in a WLCSP-9 (1.55mmx1.55mm) Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smart Watches

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2663GC-xxxx**	WLCSP-9 (1.55mmx1.55mm)	*See Below*

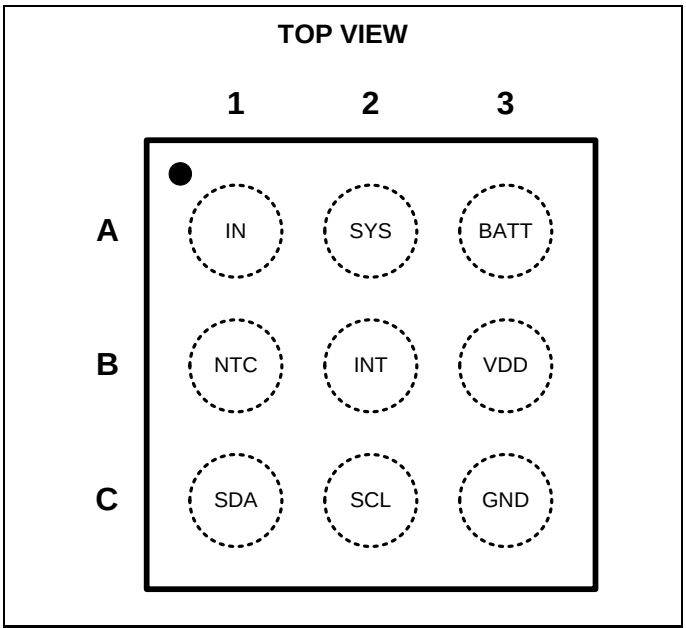
* For Tape & Reel, add suffix –Z (e.g.: MP2663GC-xxxx–Z).
**"xxxx" is the register setting option. The factory default is "0000." This content can be viewed in the I²C register map. Please contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

HLY
LLL

HL: Product code of MP2663GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



WLCSP-9 (1.55mmx1.55mm)

PIN FUNCTIONS

Package Pin #	Name	I/O	Description
A1	IN	Power	**Input power.** Place a ceramic capacitor from IN to GND as close to the IC as possible.
A2	SYS	Power	**System power supply.** Place a ceramic capacitor from SYS to GND as close to the IC as possible.
A3	BATT	Power	**Battery.** Place a ceramic capacitor from BATT to GND as close to the IC as possible.
B1	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VDD to NTC to GND. The charge is suspended when NTC is out of range.
B2	INT	O	**Open-drain interrupt output.** INT can send the charging status and fault interruption to the host. INT is also used to disconnect the system from the battery. Pull INT from high to low for >6s to turn the battery MOSFET off. Pull INT from high to low for >1.5s to turn the battery MOSFET on.
B3	VDD	I	**Internal control power supply.** Connect a ceramic cap (0.1μF) from VDD to GND. No external load is allowed.
C1	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
C2	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
C3	GND	Power	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +13V
All other pins to GND ..... -0.3V to +6.0V
Continuous power dissipation (T_A = +25°C) (2) 1.1W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .. 4.35V to 5.5V (USB input)
I_{IN} ..... Up to 455mA
I_{BATT} .....Up to 3A (5)
I_{CHG} ..... Up to 455mA
V_{BATT_REG} ..... Up to 4.545V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
WLCSP-9 (1.55mmx1.55m)	114	12	... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Guaranteed by design.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input operation voltage	V_{IN}		4.35	5	5.5	V
BATT input voltage (6)	V_{BATT}				4.5	V
Input over-voltage protection threshold	V_{IN_OVLO}	Input rising threshold	5.85	6	6.15	V
Input over-voltage protection threshold hysteresis				350		mV
Input under-voltage lock-out threshold	V_{IN_UVLO}	Input falling threshold	3.6	3.71	3.8	V
Input under-voltage lock-out threshold hysteresis				180		mV
Input vs. battery voltage headroom threshold	V_{HDRM}	Input rising vs. battery	100	130	160	mV
Input vs. battery voltage headroom threshold hysteresis				85		mV
Battery under-voltage lockout threshold	V_{BATT_UVLO}	I²C programmable range	2.4		3.1	V
		Falling, Reg01 bit[2:0] = 101	2.7	2.9	3.1	V
Battery under voltage threshold hysteresis		V_{BATT_UVLO} = 2.9V		190		mV
Battery over-voltage protection threshold	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		125		mV
Battery over-voltage protection hysteresis				55		mV
Power Path Management						
System regulation voltage	V_{SYS_REG}	V_{IN} = 5.5V, I_{SYS} = 10mA, I_{CHG} = 0A	5.1	5.2	5.3	V
Input current limit	I_{IN_LIM}	I²C programmable range	85		455	mA
		Reg00[3:0] = 000 - 85mA	65	75	85	mA
		Reg00[3:0] = 010 - 130mA	102	116	130	
		Reg00[3:0] = 100 - 265mA	230	247	265	
		Reg00[3:0] = 111 - 455mA	400	429	455	
Input minimum voltage regulation	V_{IN_MIN}	I²C programmable range	3.88		5.08	V
		I²C setting, V_{IN_MIN} = 3.88V		3.88		
IN to SYS switch on resistance	R_{ON_Q1}	V_{IN} = 5V, I_{SYS} = 100mA		330	400	mΩ
Input quiescent current	I_{IN_Q}	V_{IN} = 5.5V, CE = L, charge enabled, I_{CHG} = 0A, ISYS = 0A		630		µA
		V_{IN} = 5.5V, CE = H, charge disabled		470		

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CE = L, I_{SYS} = 0A, V_{BATT} = 4.3V		33		µA
		V_{IN} = 0V, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V, disable PCB OTP function, not including the current from the external NTC resistor		11		
		V_{IN} = 0V, CE = H, I_{SYS} = 0A, V_{BATT} = 4.35V, enable PCB OTP function, not including the current from external NTC resistor		21		
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, shipping mode, INT pulled up to VDD		4.5		µA
Batt FET on resistance	R_{ON_Q2}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100	150	mΩ
Batt FET discharge current limit	I_{DSCHG}	I²C programmable range	400			mA
Batt FET switch leakage		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, disconnect mode			1	µA
SYS reverse to BATT switch leakage		V_{SYS} = 4.65V, V_{IN} = 4.5V, V_{BATT} = GND, CE = H			1	µA
Enter shipping mode by INT (6)	t_{SHEN_DGL}	INT pull-low lasting time to turn off the battery MOSFET		6		s
Exit shipping mode by INT (6)	t_{SHEX_DGL}	In shipping mode, INT pull-low lasting time to turn on the battery MOSFET		1.5		s
Battery Charger						
Battery charge voltage regulation	V_{BATT_REG}	I²C programmable range	3.600		4.545	V
		Reg04[7:2] = 100001	4.075	4.095	4.115	V
		Reg04[7:2] = 101000	4.179	4.2	4.221	
		Reg04[7:2] = 110010	4.328	4.35	4.372	
Fast charge current	I_{CC}	V_{IN} = 5.5V, V_{BATT} = 3.8V, I²C programmable range	8		535 (6)	mA
		V_{IN} = 5.5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 8mA		13		
		V_{IN} = 5.5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 76mA		77		
		V_{IN} = 5.5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 127mA	120	127	134	
		V_{IN} = 5.5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 399mA	376	402	426	
Junction temperature regulation (6)	T_{J_REG}	Reg06[1:0] = 11 - 120°C		120		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pre-charge current	I_{PRE}	I²C programmable range	6		27	mA
		Reg03h[1:0] = 00	2.5	4.7		
		Reg03h[1:0] = 10	14	18	22	
Charge termination current threshold	I_{TERM}	$I_{CC\_SETTING}$ ≤ 263mA, (Reg02 bit[4] = 0), Reg03[1:0] = 00	5	6.8	9	mA
		$I_{CC\_SETTING}$ ≤ 263mA, (Reg02 bit[4] = 0), Reg03[1:0] = 01	10	13	17	
		$I_{CC\_SETTING}$ ≤ 263mA, (Reg02 bit[4] = 0), Reg03[1:0] = 10	16	20	24	
		$I_{CC\_SETTING}$ ≤ 263mA, (Reg02 bit[4] = 0), Reg03[1:0] = 11	22	27	32	
		$I_{CC\_SETTING}$ ≥ 280mA, (Reg02 bit[4] = 1), Reg03[1:0] = 00	10	13.8	18	
		$I_{CC\_SETTING}$ ≥ 280mA, (Reg02 bit[4] = 1), Reg03[1:0] = 01	22	27	32	
		$I_{CC\_SETTING}$ ≥ 280mA, (Reg02 bit[4] = 1), Reg03[1:0] = 10	34	41	49	
		$I_{CC\_SETTING}$ ≥ 280mA, (Reg02 bit[4] = 1), Reg03[1:0] = 11	46	55	64	
Charge termination current threshold hysteresis	I_{TERM_HYS}	$I_{CC\_SETTING}$ ≤ 263mA, (Reg02 bit[4] = 0), Reg03[1:0] = 10	7.5	11	15.5	mA
		$I_{CC\_SETTING}$ ≥ 280mA, (Reg02 bit[4] = 1), Reg03[1:0] = 10	19	24.5	31	
Pre-charge to fast charge threshold	V_{BATT_PRE}	V_{BATT} rising, set V_{BATT_LOW} = 3.0V	2.8	3.0	3.1	V
Pre-charge to fast charge threshold hysteresis				92		mV
Battery auto-recharge voltage threshold	V_{RECH}	Below V_{BATT_REG}, Reg04[0] = 0	120	160	200	mV
		Below V_{BATT_REG}, Reg04[0] = 1	260	300	350	
Thermal Protection						
Thermal shutdown threshold (6)	T_{J_SHDN}	Rising		150		°C
Thermal shutdown hysteresis (6)				20		°C
NTC output current	I_{NTC}	CE = L, NTC = 3V	-100	0	100	nA
NTC cold temp rising threshold	V_{COLD}	As percentage of V_{DD}	63	66	67	%
NTC cold temp rising threshold hysteresis				28		mV
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{DD}	31	33	35	%
NTC hot temp falling threshold hysteresis				70		mV
NTC hot temp falling threshold for PCB OTP	V_{HOT_PCB}	As a percentage of V_{DD}	30	32	34	%
NTC hot temp falling threshold hysteresis for PCB OTP				92		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
INT Pin Characteristics (6)						
Low logic voltage threshold	V_{IL}				0.5	V
High logic voltage threshold	V_{IH}		1.3			V
I²C Interface (SDA, SCL) (6)						
Input high threshold level		V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Clock Frequency and Watchdog Timer						
Clock frequency	F_{CLK}			125		kHz
Watchdog timer	t_{WDT}	Reg05h bit[5:4] = 11		163		s

NOTE:

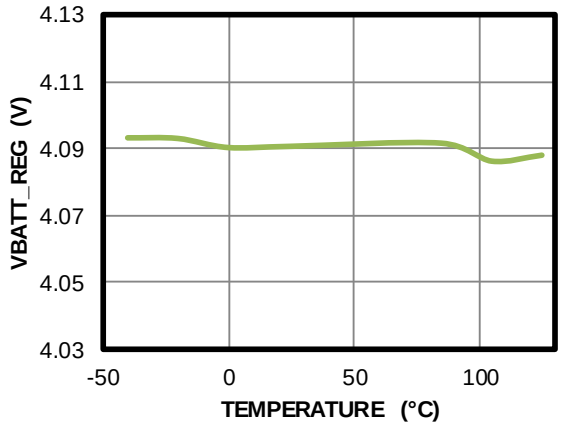
6) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 127mA, V_{IN_MIN} = 3.88V, unless otherwise noted.

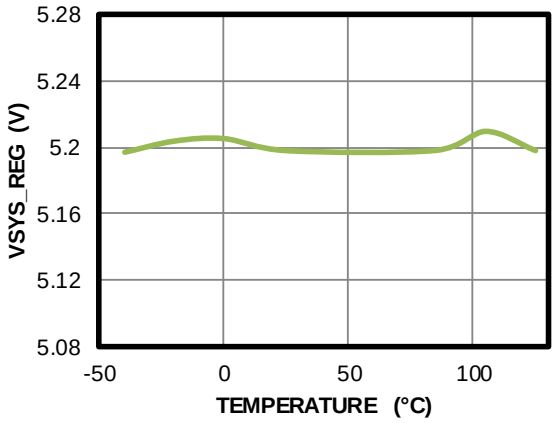
Battery Regulation Voltage vs. Temperature

V_{BATT_REG} = 4.095V



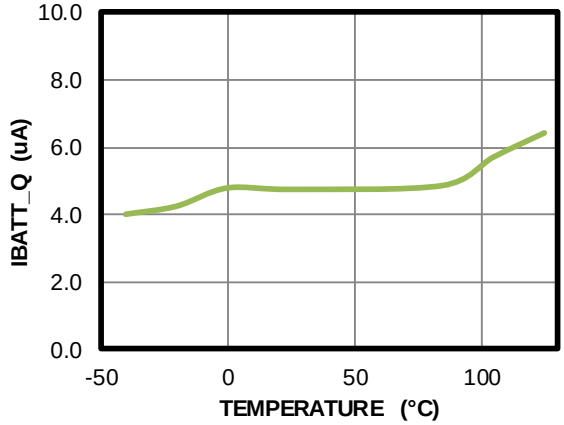
System Regulation Voltage vs. Temperature

V_{IN} = 5.5V, V_{SYS_REG} = 5.2V



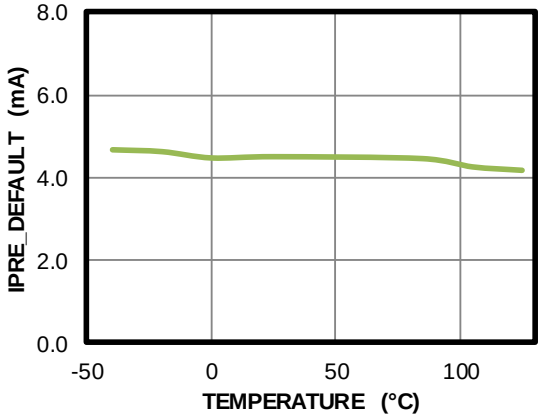
Battery Current under Shipping Mode vs. Temperature

I_{BATT_Q} = 4.5µA



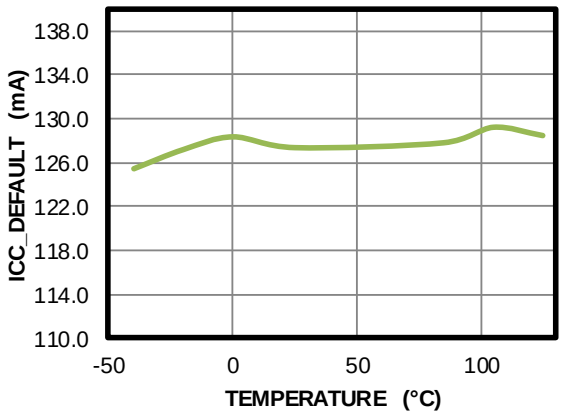
Pre-Charge Current vs. Temperature

I_{PRE} = 6mA



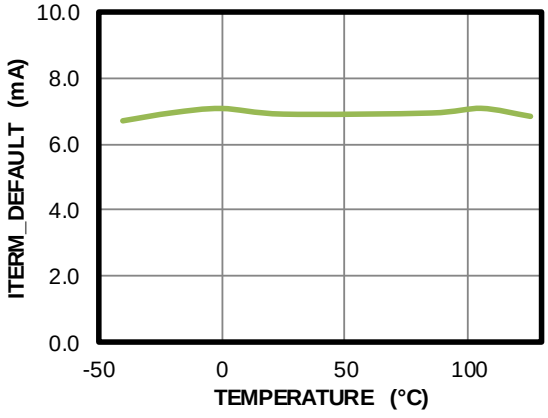
CC Charge Current vs. Temperature

V_{IN} = 5.5V, I_{CC} = 127mA



Battery Termination Current vs. Temperature

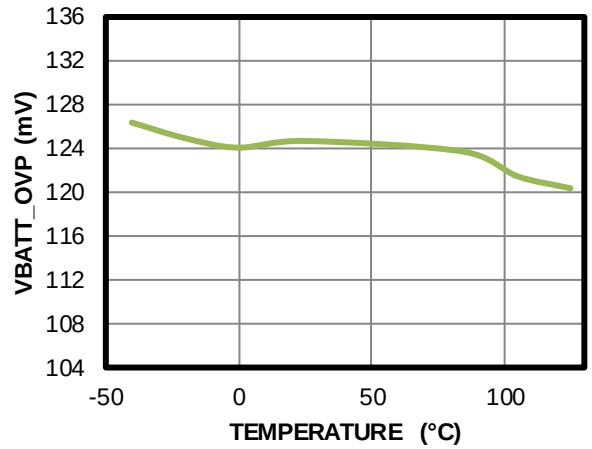
I_{TERM} = 6mA



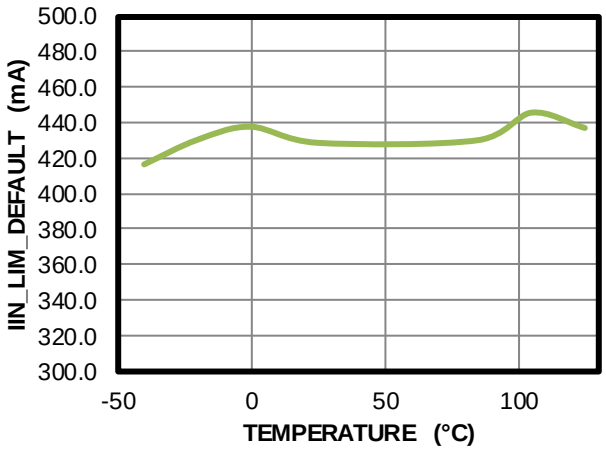
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 127mA, V_{IN_MIN} = 3.88V, unless otherwise noted.

Battery OVP Voltage vs. Temperature

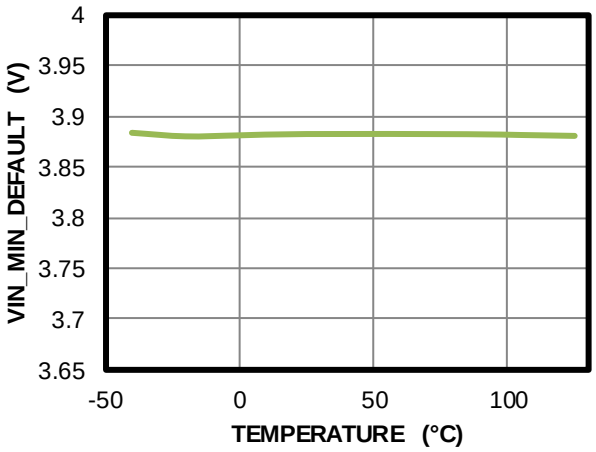


I_{Limit_455mA} vs. Temperature



Input Regulation Voltage vs. Temperature

V_{IN_MIN} = 3.88V

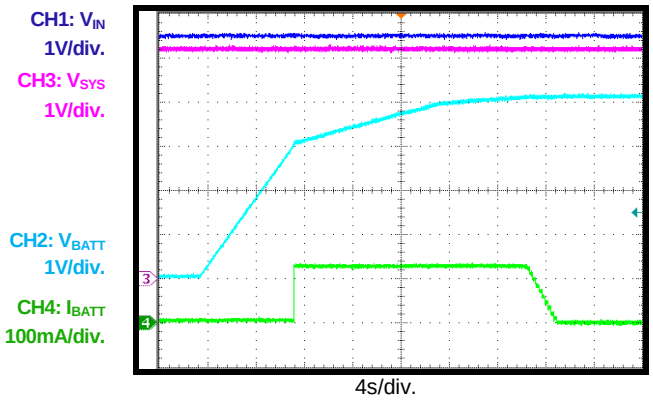


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 127mA, V_{IN_MIN} = 3.88V, unless otherwise noted.

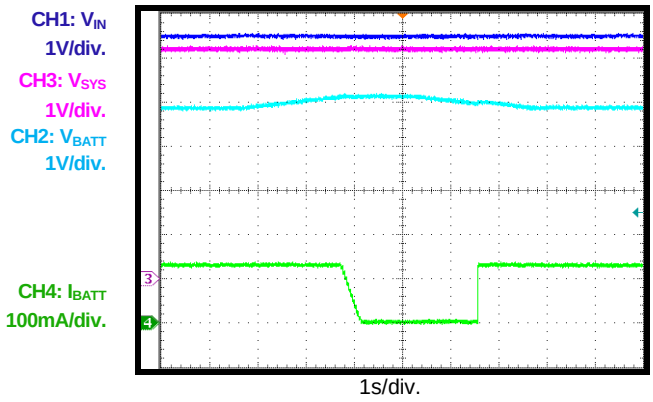
Battery Charge Curve

I_{SYS} = 0A



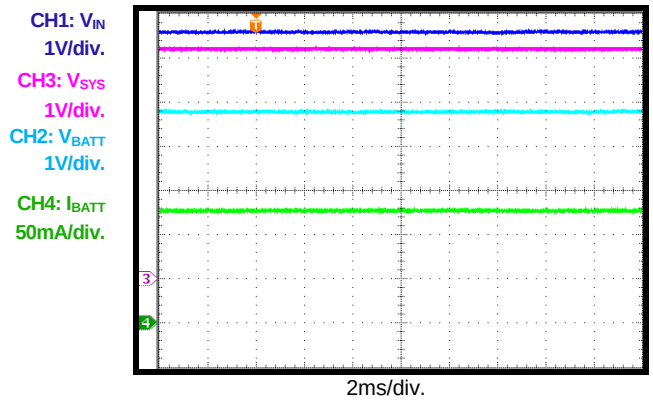
Auto Recharge

I_{SYS} = 0A



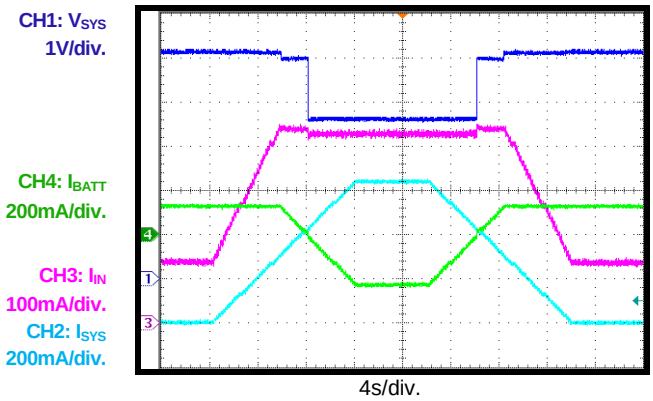
CC Charge Steady State

V_{BATT} = 3.7V, I_{SYS} = 200mA



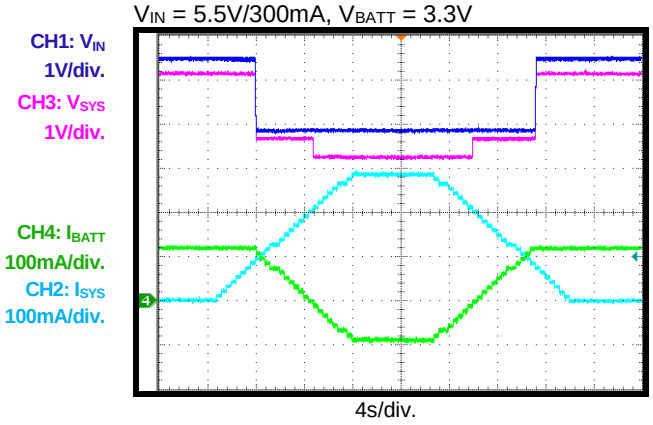
Input Current Limit-Based PPM

V_{BATT} = 3.7V



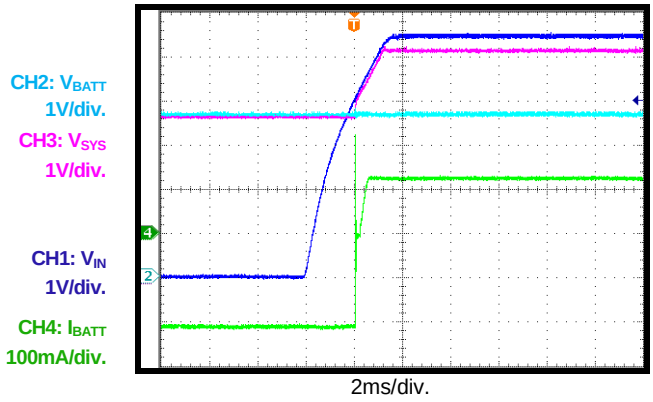
Input Voltage Regulation-Based PPM

V_{IN} = 5.5V/300mA, V_{BATT} = 3.3V



Power On

V_{BATT} = 3.7V, I_{SYS} = 200mA

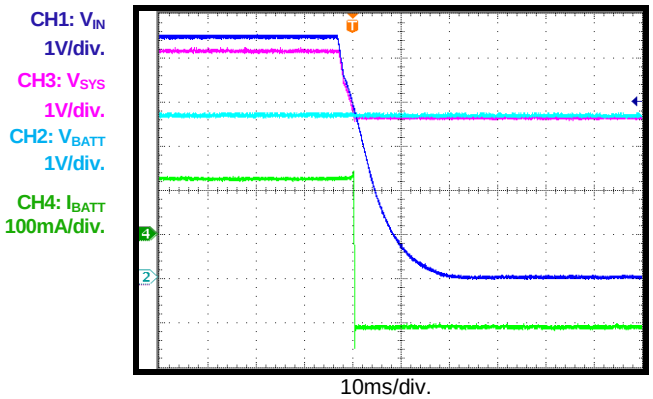


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 127mA, V_{IN_MIN} = 3.88V, unless otherwise noted.

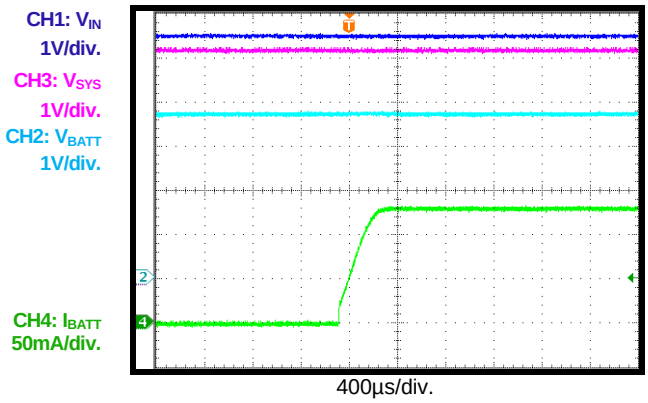
Power Off

V_{BATT} = 3.7V, I_{SYS} = 200mA



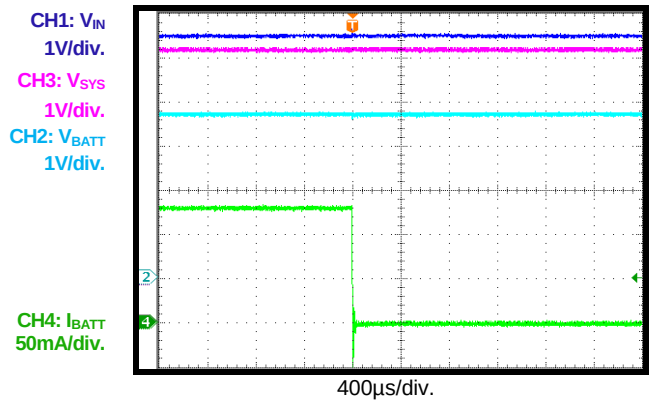
Charge Enable

V_{BATT} = 3.7V, I_{SYS} = 200mA



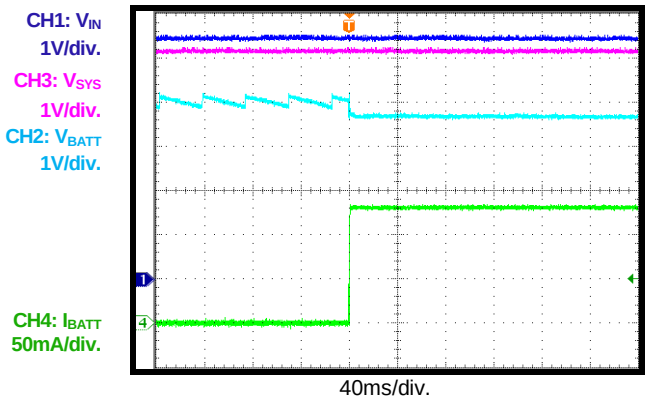
Charge Disable

V_{BATT} = 3.7V, I_{SYS} = 200mA



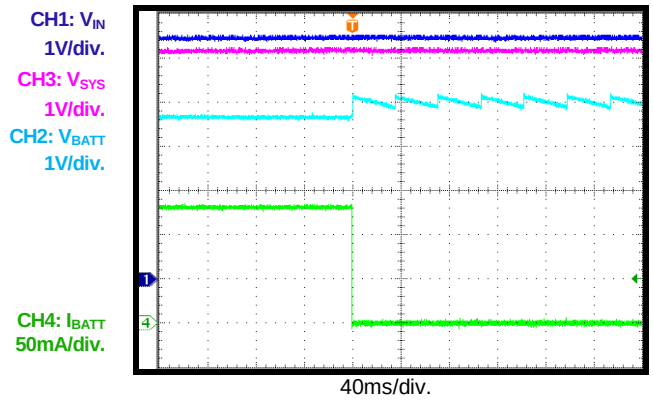
BATT Insertion

V_{BATT} = 3.7V, I_{SYS} = 0A



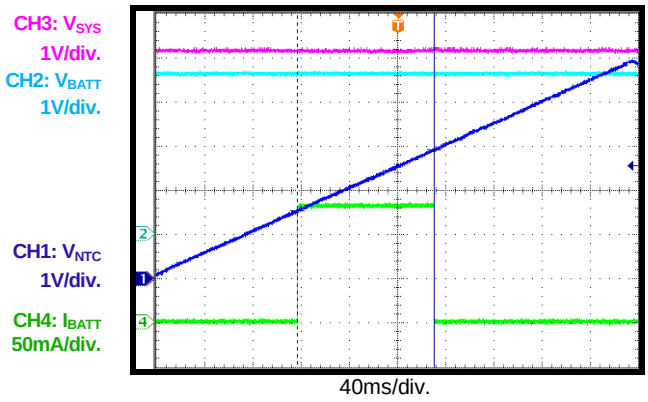
BATT Removal

V_{BATT} = 3.7V, I_{SYS} = 0A



NTC Rising

V_{BATT} = 3.7V, I_{SYS} = 0A

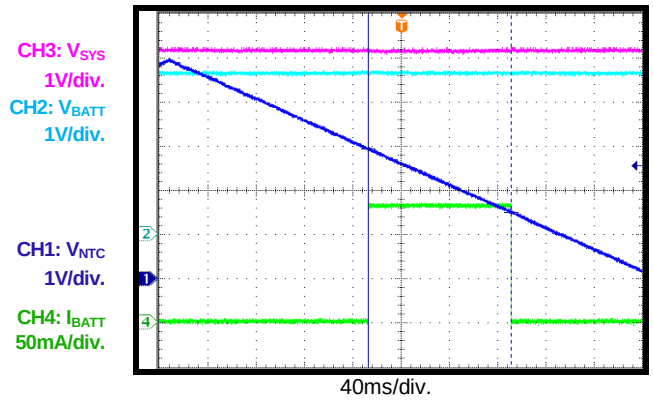


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5.5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 127mA, V_{IN_MIN} = 3.88V, unless otherwise noted.

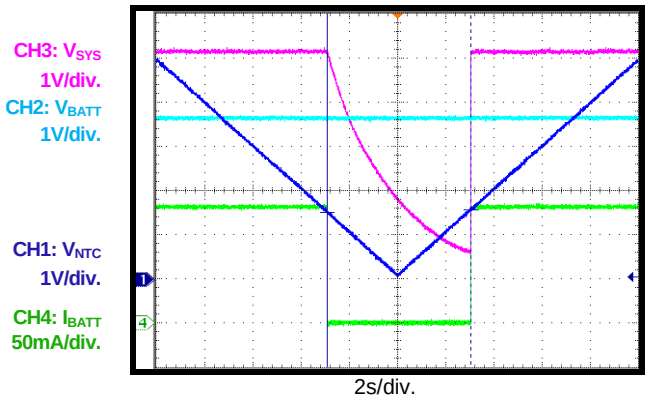
NTC Falling

V_{BATT} = 3.7V, I_{SYS} = 0A



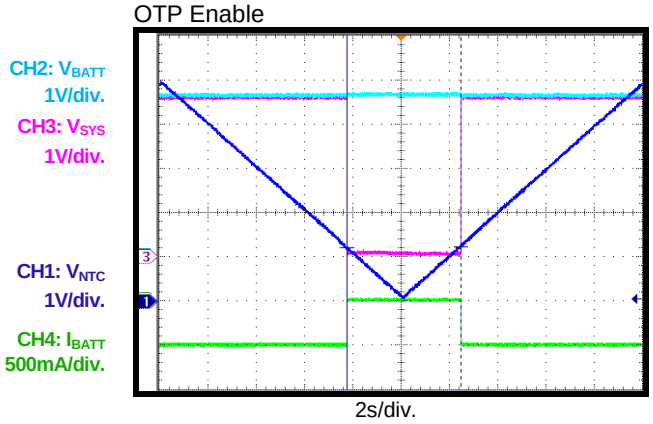
PCB OTP @ Charge Mode

V_{BATT} = 3.7V, I_{SYS} = 0A, PCB OTP Enable



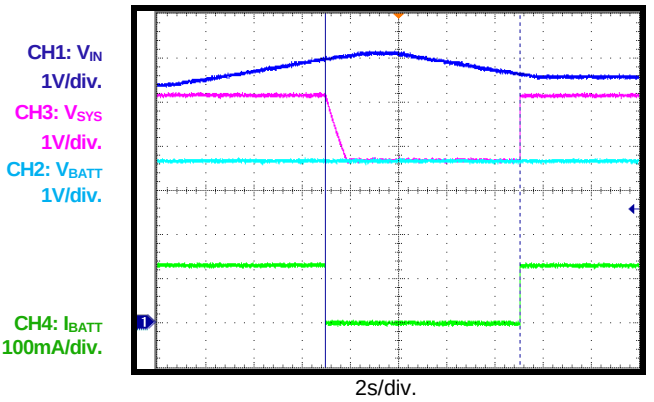
PCB OTP @ Discharge Mode

V_{IN} = 0V, V_{BATT} = 3.7V, I_{SYS} = 500mA, PCB OTP Enable



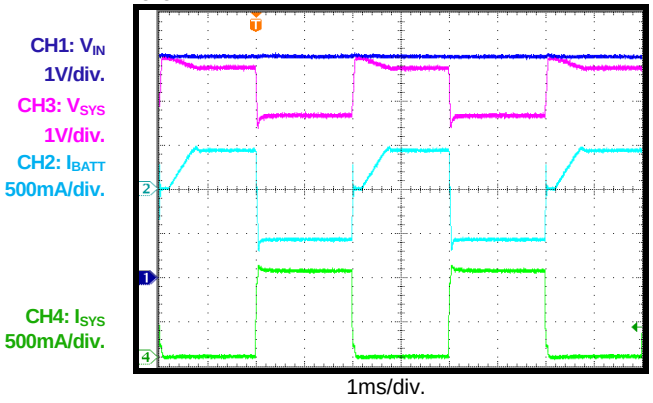
VIN OVP Operation

V_{BATT} = 3.7V, I_{SYS} = 0A



SYS Load Transient

V_{IN} = 5V, V_{BATT} = 3.8V, I_{CHG} = 535mA, I_{SYS} = 0 - 1A



BLOCK DIAGRAM

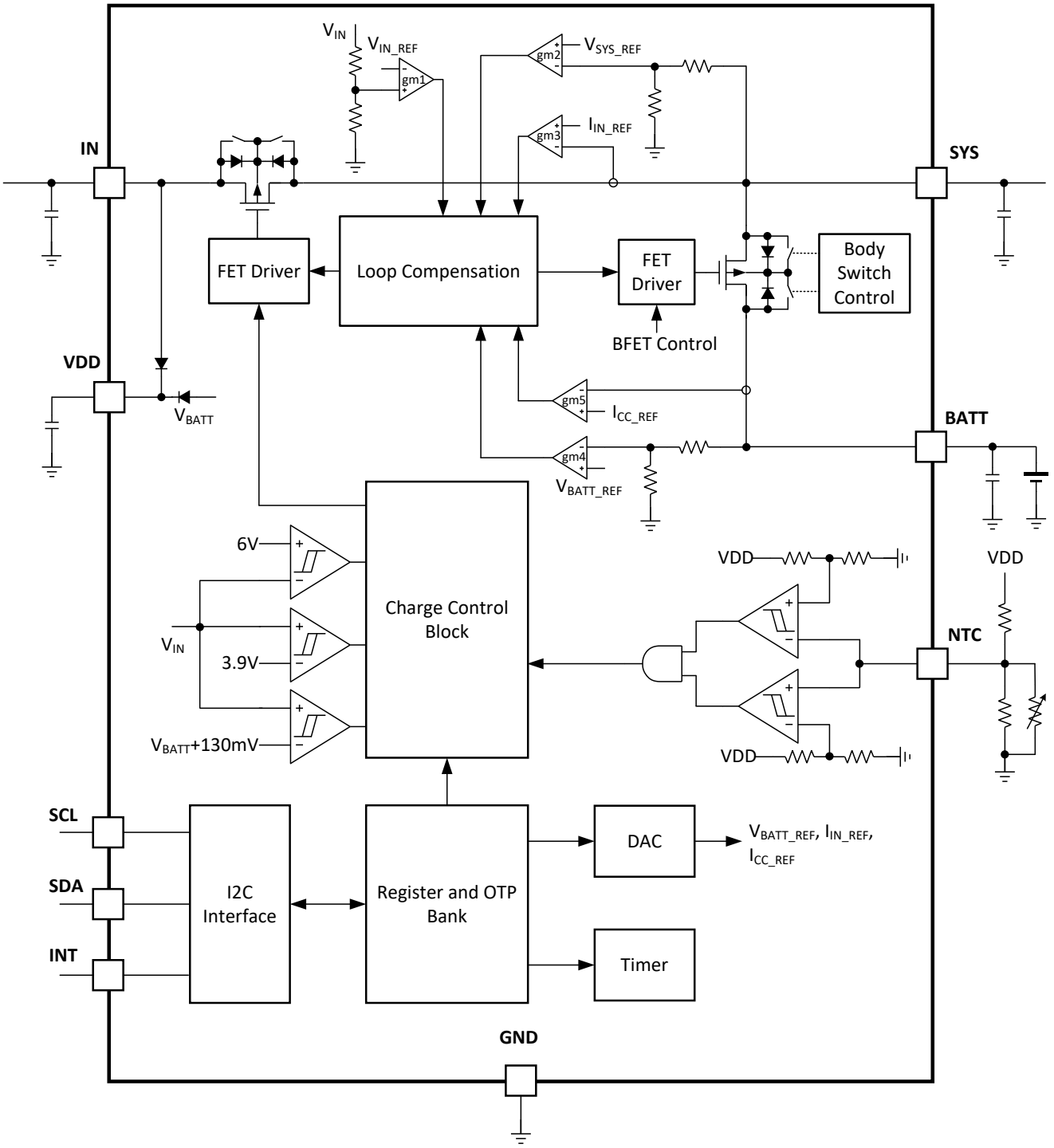


Figure 1: Functional Block Diagram

OPERATION

The MP2663 is an I²C-controlled, single-cell, Li-ion or Li-polymer battery charger with complete power path management. The full charge function features pre-charge, constant current (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If there is conflict in meeting both the system load and battery charging current, the IC reduces the charging current automatically or uses the battery as a supplemental power to satisfy the system load.

The IC integrates a 330mΩ LDO MOSFET between IN and SYS, and a 100mΩ battery FET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery MOSFET works as a full-featured linear charger with pre-charge, constant-current and constant-voltage charge, charge termination, auto-recharge, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I²C interface. The IC limits the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

In supplement mode, the 100mΩ battery MOSFET is fully turned on to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 100mΩ battery MOSFET is also fully turned on, allowing the battery to power up the system.

When the system load is satisfied, the remaining current is used to charge the smart power path management battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 2 shows the power path management structure of the MP2663.

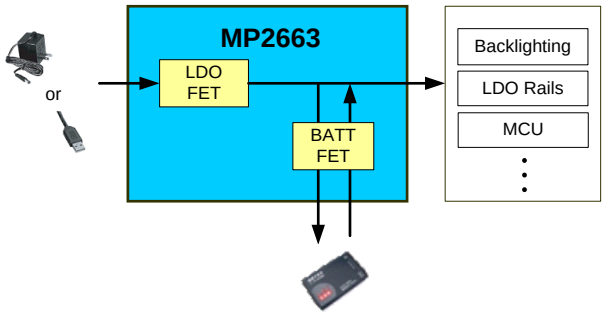


Figure 2: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BATT. When IN or BATT rises above its respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery MOSFET driver are active. The I²C interface is ready for communication, and all registers are reset to the default value. The host can access all registers.

Input OVP and UVLO

The MP2663 has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage exits the normal input voltage range, the Q1 MOSFET is turned off immediately.

When the input voltage is identified as a good source, a 200μs immunity timer becomes active. If the input power is still sufficient until the 200μs timer expires, the system starts up. Otherwise, Q1 remains off.

Figure 3 depicts the operation profile.

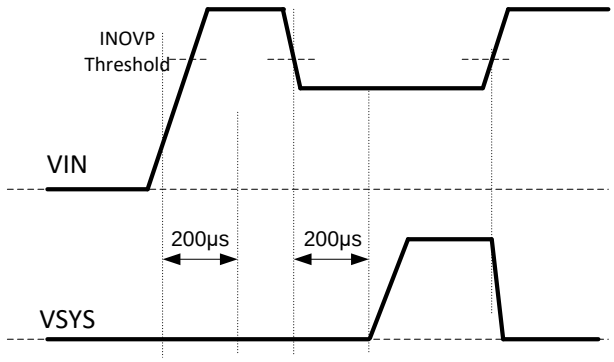


Figure 3: Input Power Detection Operation Profile

Power Path Management

The IC employs the direct power path structure with the battery MOSFET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start

up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO MOSFET.

As shown in Figure 2, the direct power structure is composed of a frond-end LDO MOSFET between IN and SYS and a battery MOSFET between SYS and BATT. The LDO MOSFET and battery MOSFET can be controlled via the I²C (see Table 1).

Table 1: MOSFET Control by I²C

MOSFET On/Off Changed by Control	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 1
LDO FET	Off	x
Battery FET (charging)	x	Off
Battery FET (discharging)	x	x

NOTE: x indicates that the value does not matter.

The input LDO (using an LDO MOSFET) provides power to the system, which drives the system load directly and charges the battery through the battery MOSFET.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO MOSFET is fully on with the input current limit.

Battery Charge Profile

The IC provides three main charging phases: pre-charge, fast-current charge, and constant-voltage charge (see Figure 4).

1. Phase 1 (pre-charge): The IC is able to safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to fast-charge threshold (V_{BATT_PRE}). The pre-charge current is programmable via Reg03 bit[1:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle is ceased, and a corresponding timeout fault signal is asserted.
2. Phase 2 (constant-current charge): When the battery voltage exceeds V_{BATT_PRE}, the IC enters a constant-current (fast charge) phase. The fast charge current can be programmable via Reg02 bit[4:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the pre-programmable charge full voltage (V_{BATT_REG}) set via Reg04h bit[7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

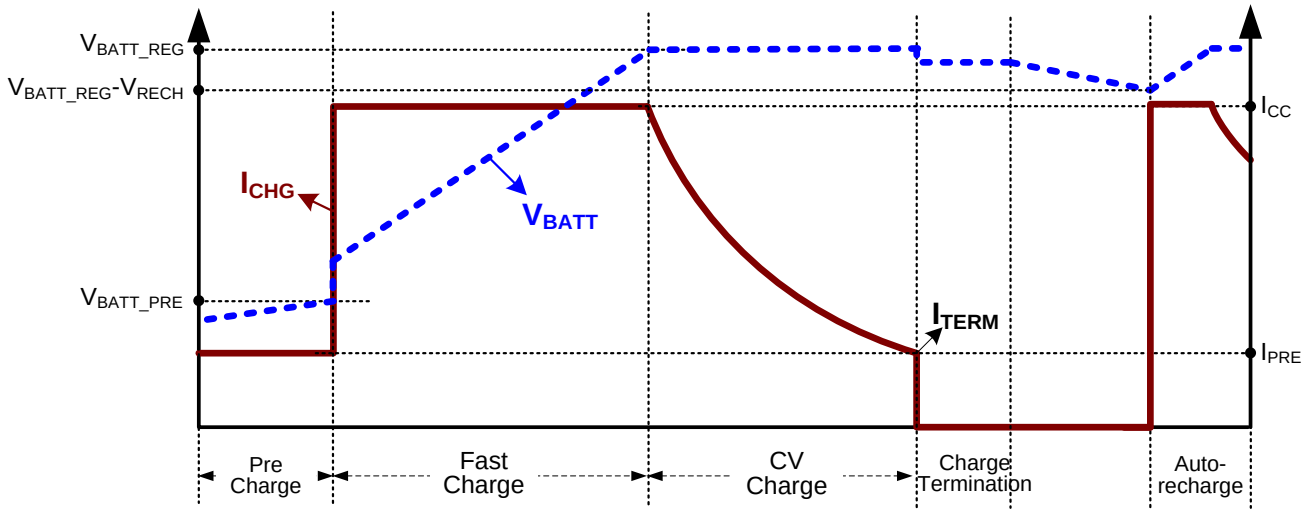


Figure 4: Battery Charge Profile

Assuming the termination function (EN_TERM) is set via Reg05h bit[6] = 1, the charge cycle is considered completed when the following conditions are valid:

- The charge current (I_{CHG}) reaches the end of charge (EOC) current threshold (I_{TERM}), and the 2.5ms delay timer is initiated.
- During the 2.5ms delay period, I_{BATT} is always smaller than I_{TERM} + I_{TERM_HYS}.

The charge status is marked as complete once the 2.5ms delay timer expires.

The charge current is terminated at the same time if TERM_TMR set via Reg05[0] = 0; otherwise, the charge current continues tapering off.

If EN_TERM = 0, the termination function is disabled, and the above actions will not occur. During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current or the input voltage reach their limits during the CV charge, the charge full termination is not influenced when the charge current is not so close to the EOC current specification.

A new charge cycle starts when the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by I²C
- Auto-recharge kicks in

Under the following conditions:

- No thermistor fault at NTC
- No safety timer fault
- No battery over voltage
- Battery MOSFET is not forced to turn off

Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold, and V_{IN} is still in the operating range, the IC begins another new charging cycle automatically without having to restarting a charging cycle manually.

The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 130mV higher than V_{BATT_REG}. When the battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

Input Current and Input Voltage Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I²C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage limit is reached, the Q1 MOSFET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system drops to the minimum value of 5.085V or V_{IN} - 160mV, the charge current is reduced to prevent the system voltage from dropping further. When V_{IN} < V_{SYS_REG}, the charge current will not be reduced, even when V_{SYS} is less than 5.085V, as long as the condition V_{IN} - 160mV remains (where 160mV refers to the voltage drop across the reverse-blocking MOSFET due to I_{CHG} + I_{SYS}).

Voltage-based DPM regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity. V_{IN_MIN} sets via the I²C should be at least 400mV higher than V_{BATT_REG} to ensure the stable operation of the regulator.

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero, and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off.

Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, ideal diode mode is enabled. The battery MOSFET is regulated to maintain V_{BATT} - V_{SYS} at 22.5mV. If the supplement current I_{DCHG} * R_{ON_BATT} is higher than 22.5mV, the battery MOSFET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BATT} + 20mV, ideal diode mode is disabled.

Figure 5 and Figure 6 show the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, the IC operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.

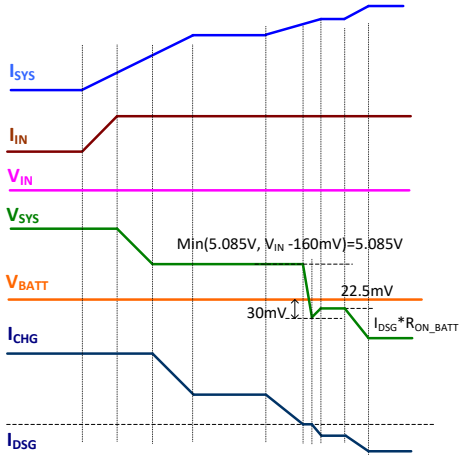


Figure 5: DPM and Battery Supplement Operation Profile (V_{IN} > V_{SYS_REG})

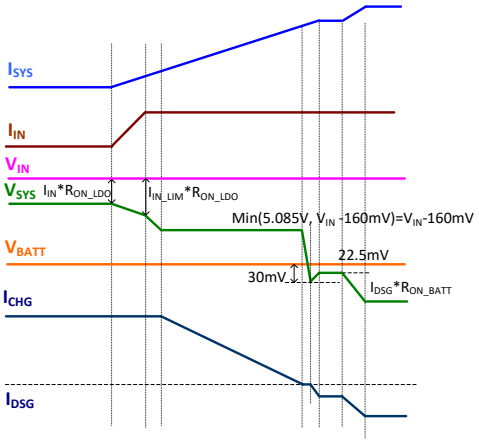


Figure 6: DPM and Battery Supplement Operation Profile (V_{IN}<V_{SYS_REG})

Battery Regulation Voltage

The battery voltage for the constant-voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the BATT voltage is between V_{BATT_REG} - V_{RECH} and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the pre-set limit of T_{J_REG} (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via Reg06 bit[1:0].

When the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot. In the MP2663, the I²C default setting is to enable the battery NTC monitor. The function can be changed through the I²C (see Table 2)

Table 2: NTC Function Selection Table

I²C Control		Function
EN_NTC	EN_PCB OTP	
0	x	Disable
1	1	NTC
1	0	PCB OTP

When PCB OTP is selected, if the NTC voltage is lower than the NTC hot threshold, both the LDO MOSFET and battery MOSFET are off. The PCB OTP fault sets the NTC_FAULT status (Reg08h bit[1]) to 1 to indicate the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back to the safe range.

Safety Timer

The IC provides both a pre-charge and fast-charge safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is one hour when battery voltage is below V_{BATT_PRE}. The fast-charge safety timer starts when the battery enters fast charging. The fast-charge safety timer can be programmed through the I²C. The safety timer feature can be disabled via the I²C.

The following actions can restart the safety timer:

- A new charge cycle is kicked in
- Reg05h bit[7] is written from 0 to 1 (charge enable)
- Reg05h bit[3] is written from 0 to 1 (safety timer enable)
- Reg01h bit[7] is written from 0 to 1 (software reset)

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, the IC starts in the watchdog timer expiration state, or default mode. All the registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (Reg05 bit[5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the Reg01 bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no V_{IN}, the watchdog timer is suspended.

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no V_{IN}
- Register Reg01h bit[7] is reset

Battery Discharge Function

If the battery is connected and the input source is missing, the battery MOSFET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery MOSFET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (default 800mA), the battery MOSFET is turned off after a 60μs delay, and the MP2663 enters hiccup mode in over-current protection (OCP). The discharge current can be programmed high to 3.2A through the I²C. If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery MOSFET is turned off and starts hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (default 2.9V), the battery MOSFET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The MP2663 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, the system SCP for the IN to SYS path and the BATT to SYS path is active. I_{DSCHG} is decreased to half of the original value.

1) IN to SYS path: Once I_{IN} is over the protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit is not reached. If the setting input current limit is reached, I_{IN} is regulated at I_{IN_LMT}. Hiccup mode also starts after a 60µs delay. The interval of the hiccup mode is 800µs.

2) BATT to SYS path: Once I_{BATT} is over the 3.7A protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60µs delay. The interval of the hiccup mode is 800µs.

For details, please refer to flow chart in Figure 13.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation.

Interrupt to Host (INT)

The IC also has an alert mechanism, which can output an interrupt signal via INT to notify the system of the operation by outputting a 256µs low-state INT pulse. All of the below events can trigger the INT output:

- Good input source detected
- UVLO or input over-voltage protection (OVP)
- Charge completed
- Charging status change
- Any fault in Reg08h (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in Reg09h. After the IC exits the fault state, the fault bit can be released to 0 after the host reads Reg09h. The NTC fault is not latched and always reports the current thermistor conditions.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode. The MP2663 provides two methods for entering shipping mode (see Table 3):

1. During normal operation, the battery MOSFET is turned on, and FET_DIS bit is 0. Set FET_DIS bit to 1. The MP2663 enters shipping mode, the battery MOSFET turns off and the FET_DIS bit refreshes to 0.
2. Pull INT down by pushing the push button for 6s during normal operation. The MP2663 enters shipping mode, and the battery MOSFET turns off.

There are two methods for exiting shipping mode. The first method is to pull down INT for 1.5s. The MP2663 exits shipping mode, and the battery MOSFET turns on (see Figure 7). The second method is to plug in V_{IN}. The system voltage starts up from V_{IN} immediately, and the MP2663 exits shipping mode after 1.5s. During the 1.5s time period, charging is disabled, and supplement mode is disabled (see Figure 8).

NOTE: It is not recommended to enter shipping mode when V_{IN} is present.

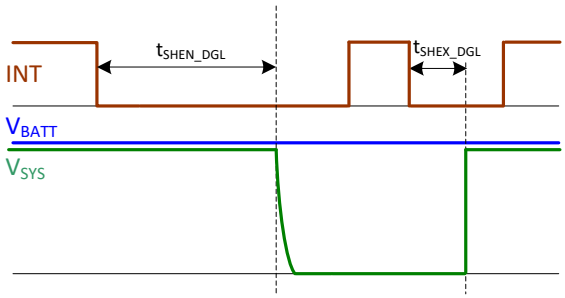


Figure 7: Shipping Mode Function via INT

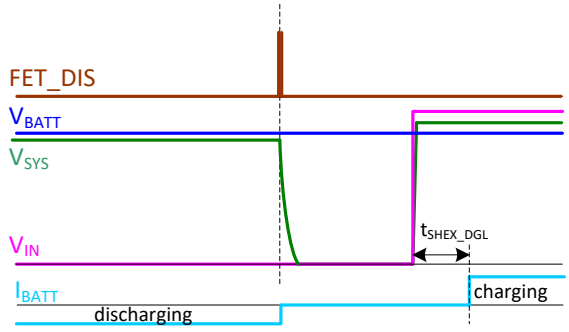


Figure 8: Enter Shipping Mode via Writing FET_DIS, Exit Shipping Mode via V_{IN} Plug-In

Table 3: Shipping Mode Control

MOSFET On/Off Changed By Control	Enter Shipping Mode		Exit Shipping Mode	
	SET FET_DIS to 1	INT H to L for 6s	INT H to L for 1.5s	VIN Plug-In
LDO FET	x	x	x	ON
Battery FET (charging)	OFF	OFF	ON	ON (1.5s later)
Battery FET (discharging)	OFF	OFF	ON	ON (1.5s later)

NOTE: "x" indicates that the value does not matter.

I²C REGISTER MAP

IC Address: 09H (Reserved some trim options)

Input Source Control Register/Address: 00H (Default: 0000 0111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_HIZ (7)	0	Y	Y	r/w	0: disable 1: enable	Default: disable (0)
6	V_{IN_MIN} [3]	0	Y	Y	r/w	640mV	Offset: 3.88V Range: 3.88V - 5.08V Default: 3.88V (0000)
5	V_{IN_MIN} [2]	0	Y	Y	r/w	320mV	
4	V_{IN_MIN} [1]	0	Y	Y	r/w	160mV	
3	V_{IN_MIN} [0]	0	Y	Y	r/w	80mV	
2	I_{IN_LIM} [2]	1	Y	Y	r/w	000: 85mA 001: 130mA 010: 175mA 011: 220mA 100: 265mA 101: 310mA 110: 355mA 111: 455mA	Default: 455mA (111)
1	I_{IN_LIM} [1]	1	Y	Y	r/w		
0	I_{IN_LIM} [0]	1	Y	Y	r/w		

Power-On Configuration Register/Address: 01H (Default: 0000 1101)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Register reset	0	Y	Y	r/w	0: keep current setting 1: reset	Keep current register setting (0)
6	I²C watchdog timer reset	0	Y	Y	r/w	0: normal 1: reset	Normal (0)
5	Reserved	0	Y	Y	r/w		
4	Reserved	0	Y	Y	r/w		
3	CEB	1	Y	Y	r/w	0: charge enable 1: charge disabled	Charge disabled (1)
2	V_{BATT_UVLO} [2]	1	Y	Y	r/w	0.4V	Offset: 2.4V Range: 2.4V - 3.1V Default: 2.9V (101)
1	V_{BATT_UVLO} [1]	0	Y	Y	r/w	0.2V	
0	V_{BATT_UVLO} [0]	1	Y	Y	r/w	0.1V	

NOTE:

7) This bit only controls the on and off function of the LDO MOSFET.

Charge Current Control Register/Address: 02H (Default: 0000 0111)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	Y	Y	r/w		
6	Reserved	0	Y	Y	r/w		
5	Reserved	0	Y	Y	r/w		
4	I_{CC} [4]	0	Y	Y	r/w	272mA	Offset: 8mA Range: 8mA - 535mA Default: 127mA (00111)
3	I_{CC} [3]	0	Y	Y	r/w	136mA	
2	I_{CC} [2]	1	Y	Y	r/w	68mA	
1	I_{CC} [1]	1	Y	Y	r/w	34mA	
0	I_{CC} [0]	1	Y	Y	r/w	17mA	

Pre-Charge/Discharge Current/Address: 03H (Default: 0001 1100)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	Y	Y	r/w		
6	I_{DSCHG}[3]	0	Y	Y	r/w	1600mA	Offset: 200mA Range: 400mA - 3.2A Valid range: 0001 - 1111 Default: 800mA (0011)
5	I_{DSCHG}[2]	0	Y	Y	r/w	800mA	
4	I_{DSCHG}[1]	1	Y	Y	r/w	400mA	
3	I_{DSCHG}[0]	1	Y	Y	r/w	200mA	
2	EN_PCB OTP	1	Y	Y	r/w	0: enable 1: disable	Disable (1)
1	I_{PRE} [1]	0	Y	Y	r/w	14mA	Offset: 6mA Range: 6mA - 27mA Default: 6mA (00) I_{PRE}[1:0] also sets the termination current
0	I_{PRE} [0]	0	Y	Y	r/w	7mA	

Charge Voltage Control Register/Address: 04H (Default: 1000 0110)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG} [5]	1	Y	Y	r/w	480mV	Offset: 3.60V Range: 3.60V - 4.545V Default: 4.095V (100001)
6	V_{BATT_REG} [4]	0	Y	Y	r/w	240mV	
5	V_{BATT_REG} [3]	0	Y	Y	r/w	120mV	
4	V_{BATT_REG} [2]	0	Y	Y	r/w	60mV	
3	V_{BATT_REG} [1]	0	Y	Y	r/w	30mV	
2	V_{BATT_REG} [0]	1	Y	Y	r/w	15mV	
1	V_{BATT_PRE}	1	Y	Y	r/w	0: 2.8V 1: 3.0V	3.0V (1)
0	V_{RECH}	0	Y	Y	r/w	0: 150mV 1: 300mV	150mV (0)

Charge Termination/Timer Control Register/Address: 05H (Default: 0100 1010)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	Y	Y	r/w		
6	EN_TERM	1	Y	Y	r/w	0: disable 1: enable	Enable (1)
5	WATCHDOG [1]	0	Y	Y	r/w	00: disable timer 01: 40s 10: 80s 11: 160s	Disable timer (00)
4	WATCHDOG [0]	0	Y	Y	r/w		
3	EN_TIMER	1	Y	Y	r/w	0: disable 1: enable	Enable timer (1)
2	CHG_TMR [1]	0	Y	Y	r/w	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	5hrs (01)
1	CHG_TMR [0]	1	Y	Y	r/w		
0	TERM_TMR	0	Y	Y	r/w	0: disable 1: enable	(0)

Miscellaneous Operation Control Register/Address: 06H (Default: 0000 1011)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	Y	Y	r/w		
6	Reserved	0	Y	Y	r/w		
5	FET_DIS (8)	0	Y	Y	r/w	0: enable 1: turn off	Enable (0)
4	Reserved	0	Y	Y	r/w		
3	EN_NTC	1	Y	Y	r/w	0: disable 1: enable	Enable (1)
2	Reserved	0	Y	Y	r/w		
1	T_{J_REG} [1]	1	Y	Y	r/w	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Default: 120°C (11)
0	T_{J_REG} [0]	1	Y	Y	r/w		

NOTE:
8) This bit controls the on and off function of the battery MOSFET, including charge and discharge.

System Status Register/Address: 07H (Default: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	N	N	r		
6	Rev [1]	0	N	N	r	Revision number	00
5	Rev [0]	0	N	N	r		
4	CHG_STAT [1]	0	N	N	r	00: not charging 01: pre-charge 10: charge 11: charge done	Not charging (00)
3	CHG_STAT [0]	0	N	N	r		
2	PPM_STAT	0	N	N	r	0: no PPM 1: in PPM	No PPM (0) (no power-path management occurs)
1	PG_STAT	0	N	N	r	0: power fail 1: power good	No power good (0)
0	THERM_STAT	0	N	N	r	0: no thermal regulation 1: in thermal regulation	Normal (0)

FAULT REGISTER/ ADDRESS: 08H (DEFAULT: 0000 0000)

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	0	N	N	r		
6	WATCHDOG_ FAULT	0	N	N	r	0: normal 1: watchdog timer expiration	Normal (0)
5	VIN_FAULT	0	N	N	r	0: normal 1: input fault (OVP or bad source)	Normal (0)
4	THEM_SD	0	N	N	r	0: normal 1: thermal shutdown	Normal (0)
3	BAT_FAULT	0	N	N	r	0: normal 1: battery OVP	Normal (0)
2	STMR_FAULT	0	N	N	r	0: normal 1: safety timer expiration	Normal (0)
1	NTC_FAULT [1]	0	N	N	r	0: normal 1: NTC hot	Normal (0)
0	NTC_FAULT [0]	0	N	N	r	0: normal 1: NTC cold	Normal (0)

OTP MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x02	N/A			I_{CC}: **8mA - 535mA / 17mA** step				
0x03	N/A					EN_PCB_OTP	I_{PRE}	
0x04	V_{BATT_REG}: **3.6V - 4.545V / 15mV** step						N/A	
0x05	N/A		WATCHDOG		N/A			

OTP DEFAULT

OTP Items	Default
I_{CC}	127mA
I_{PRE}	6mA
V_{BATT_REG}	4.095V
WATCHDOG	Disable timer
EN_PCB OTP	Disable

STATE CONVERSION CHART

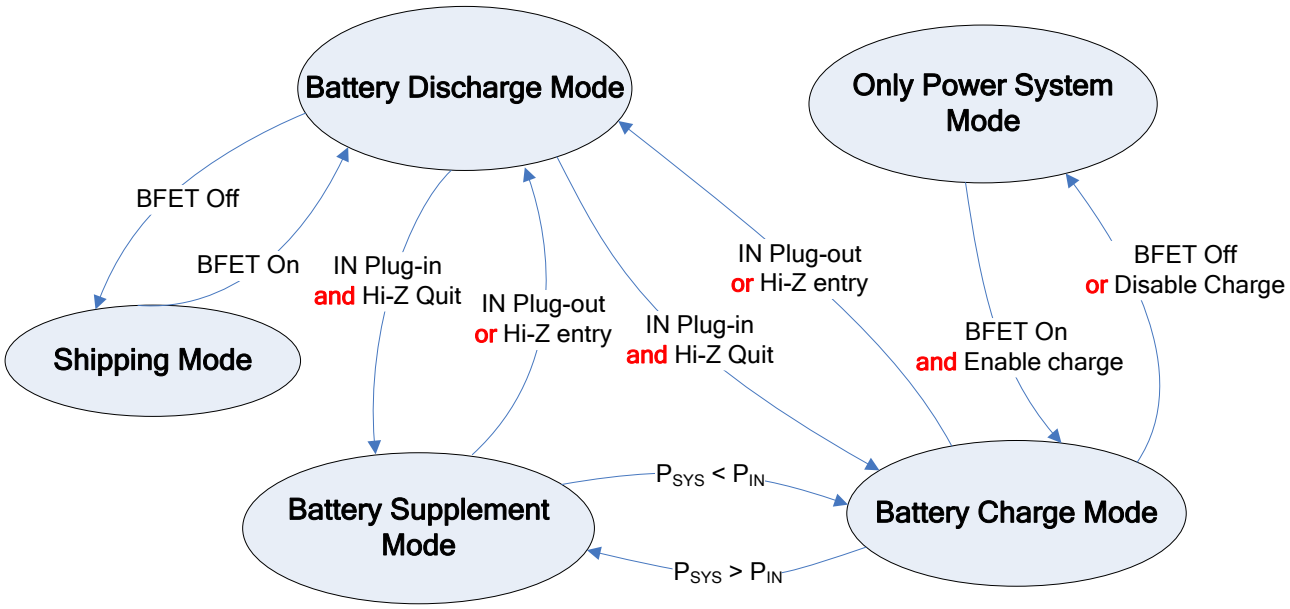


Figure 9: State Machine Conversion

CONTROL FLOW CHART

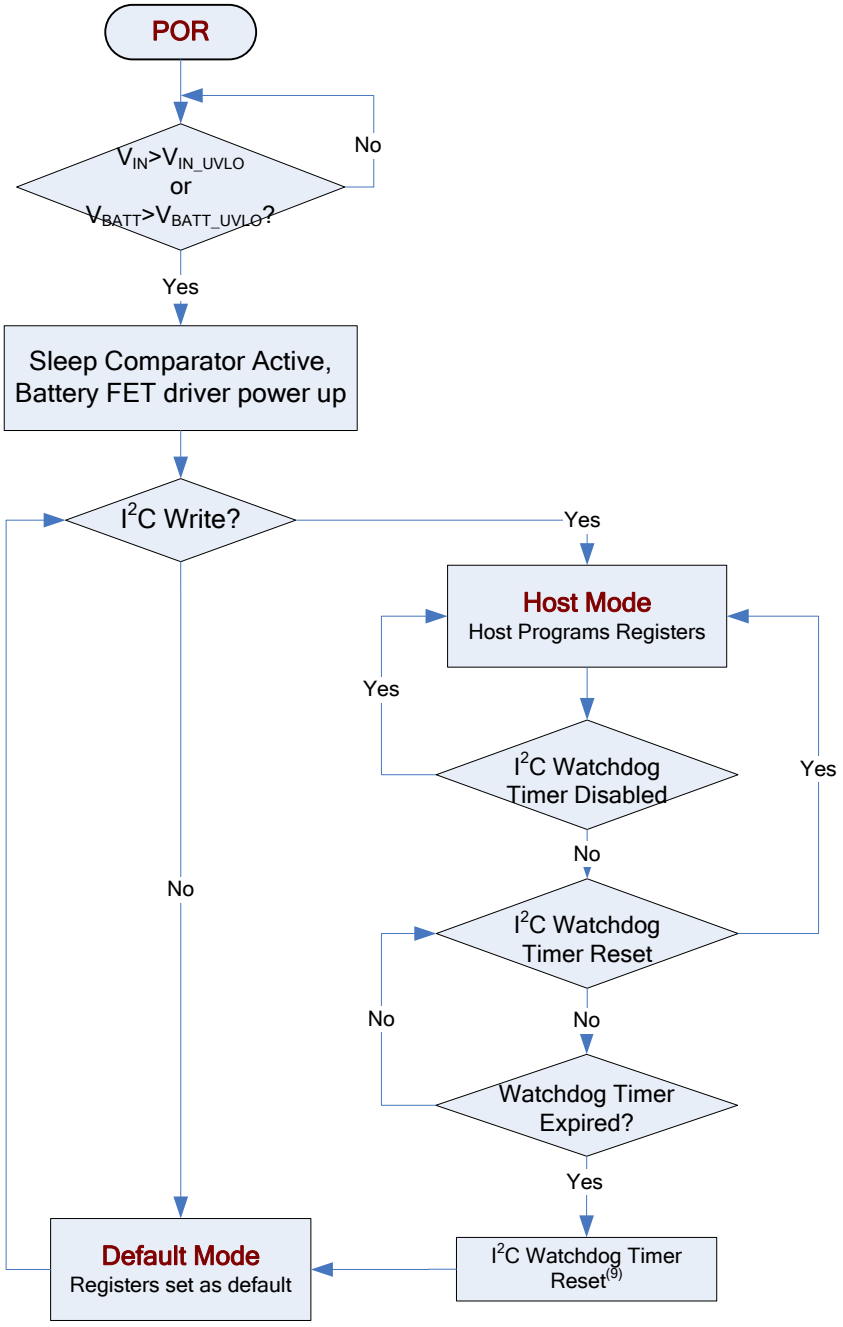


Figure 10: Default Mode and Host Mode Selection (10)

NOTES:

9) Once the watchdog timer expires, the I²C watchdog timer must be reset , or the watchdog timer is not valid in the next cycle.

10) The watchdog timer is held when V_{IN} is not present.

CONTROL FLOW CHART *(continued)*

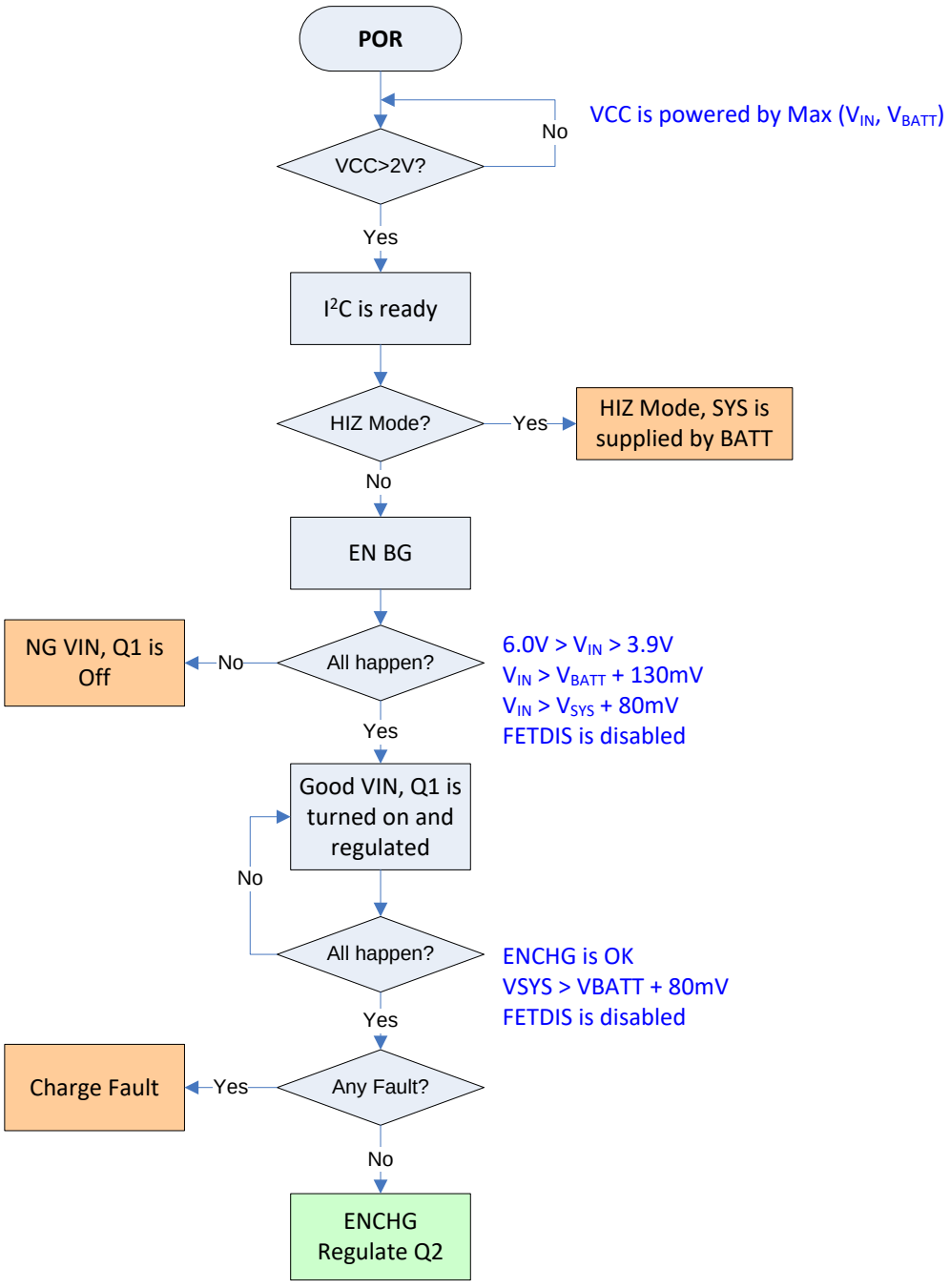


Figure 11: Input Power Start-up Flow Chart

CONTROL FLOW CHART *(continued)*

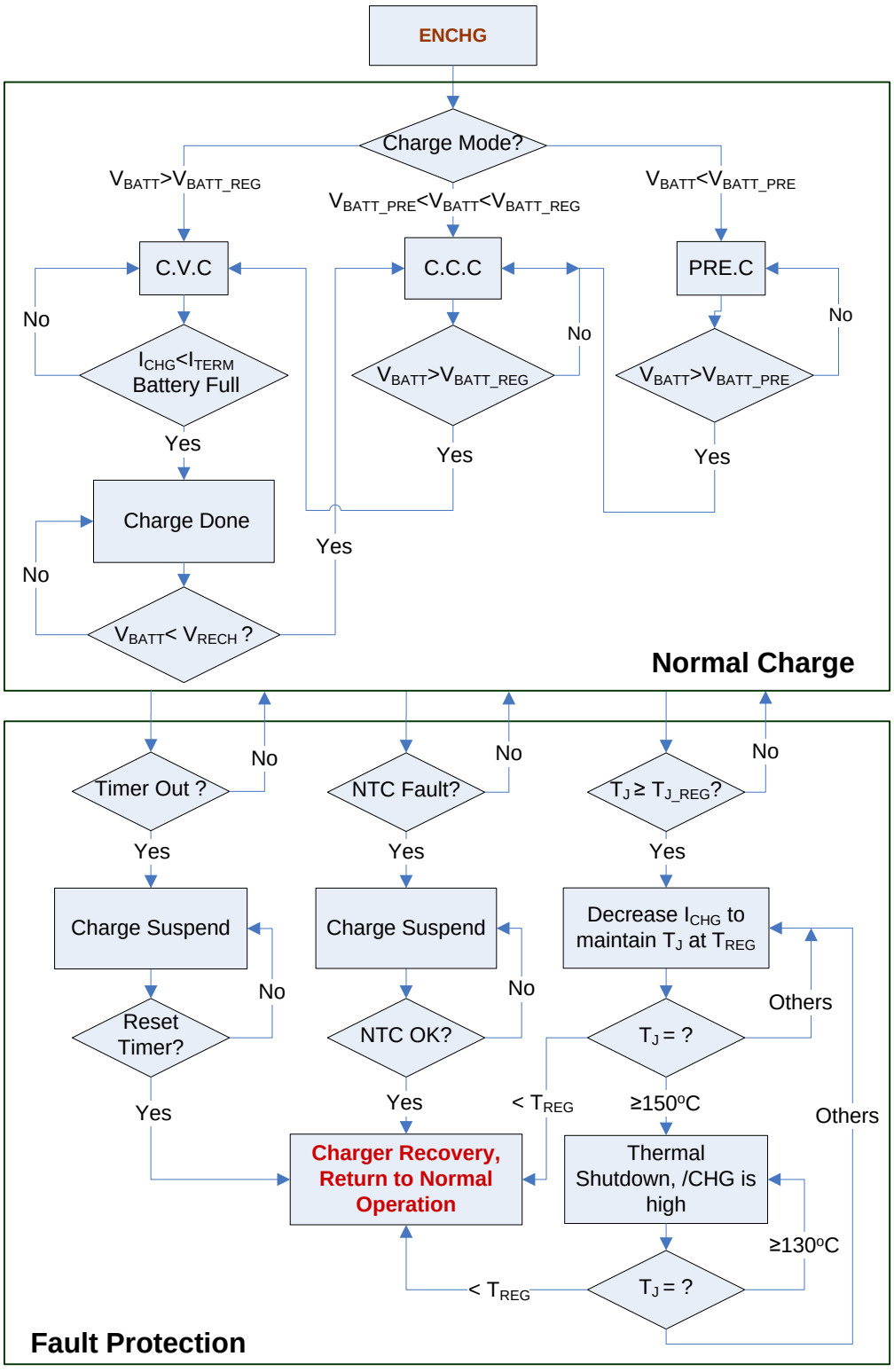


Figure 12: Charging Process

CONTROL FLOW CHART *(continued)*

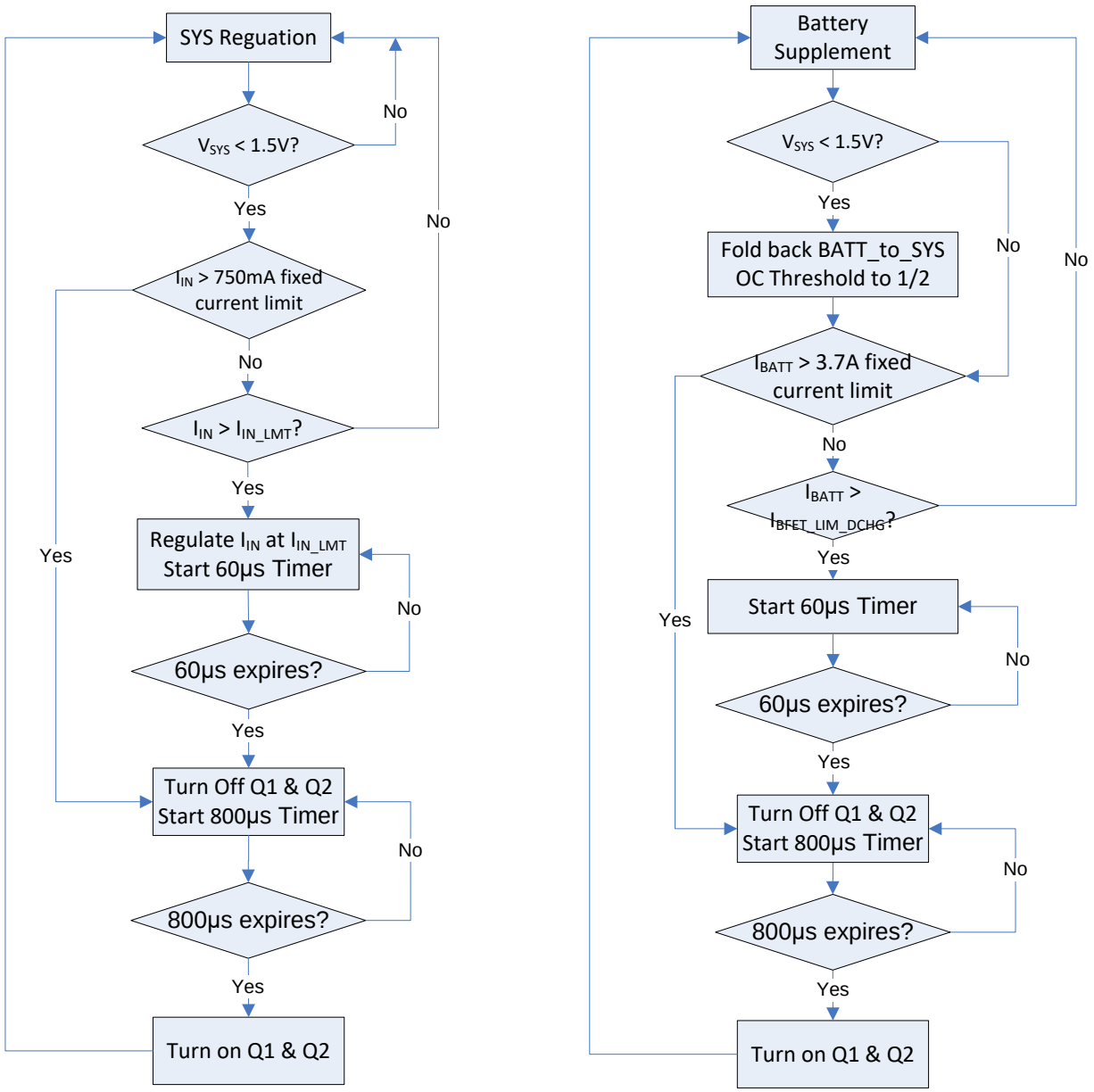


Figure 13: System Short-Circuit Protection

APPLICATION INFORMATION

Selecting a Resistor for the NTC Sensor

NTC uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be programmed independently (see Figure 14). In other words, the IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors.

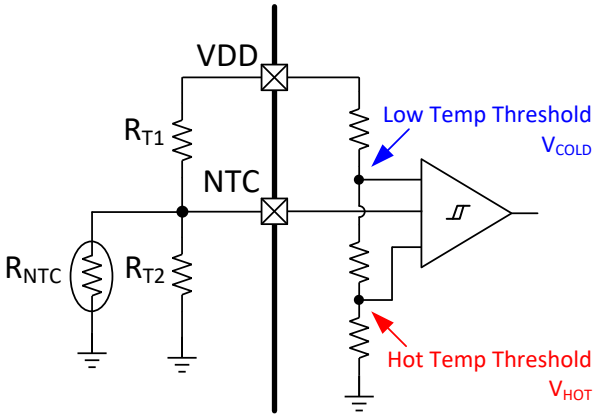


Figure 14: NTC Function Block

For a given NTC thermistor, R_{T1} and R_{T2} values depend on the type of NTC resistor used and can be calculated with Equation (1) and Equation (2):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD}V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1\text{-}V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at a high temperature of the required temperature operation range, and R_{NTCL} is the value of the NTC resistor at a low temperature.

For example, for the thermistor NCP18XH103, R_{NTCL} is 27.219kΩ at 0°C, and R_{NTCH} is 4.161kΩ at 50°C. Equation (1) and Equation (2) determine that R_{T1} = 7.44kΩ and R_{T2} = 30.79kΩ (assuming that the NTC window is between 0°C and 50°C and using the V_{COLD} and V_{HOT} values from the EC table on page 8).

External Capacitor Selection

Like most low-dropout regulators, the MP2663 requires external capacitors for regulator stability and voltage spike immunity. The MP2663 is designed specifically for portable applications requiring minimal board space and small components. These capacitors must be selected correctly for optimal performance.

Input Capacitor

An input capacitor is required for stability. Connect a 1µF (minimum) capacitor between IN to GND for stable operation over the full load current range. It is acceptable to have more output capacitance than input as long as the input is at least 1µF.

Output Capacitor

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor (dielectric type X5R or X7R) >2.2µF is suitable in the MP2663 application circuit. For this device, the output capacitor should be connected between SYS and GND with a thick trace and small loop area.

BATT to GND Capacitor

A capacitor from BATT to GND is necessary for the MP2663. A ceramic capacitor (dielectric type X5R or X7R) >2.2µF is suitable for the MP2663 application circuit.

VDD to GND Capacitor

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND very close to the IC.
3. Keep the GND for the I2C wire clean and far from GND.
4. Place the I²C wire in parallel.

TYPICAL APPLICATION CIRCUIT

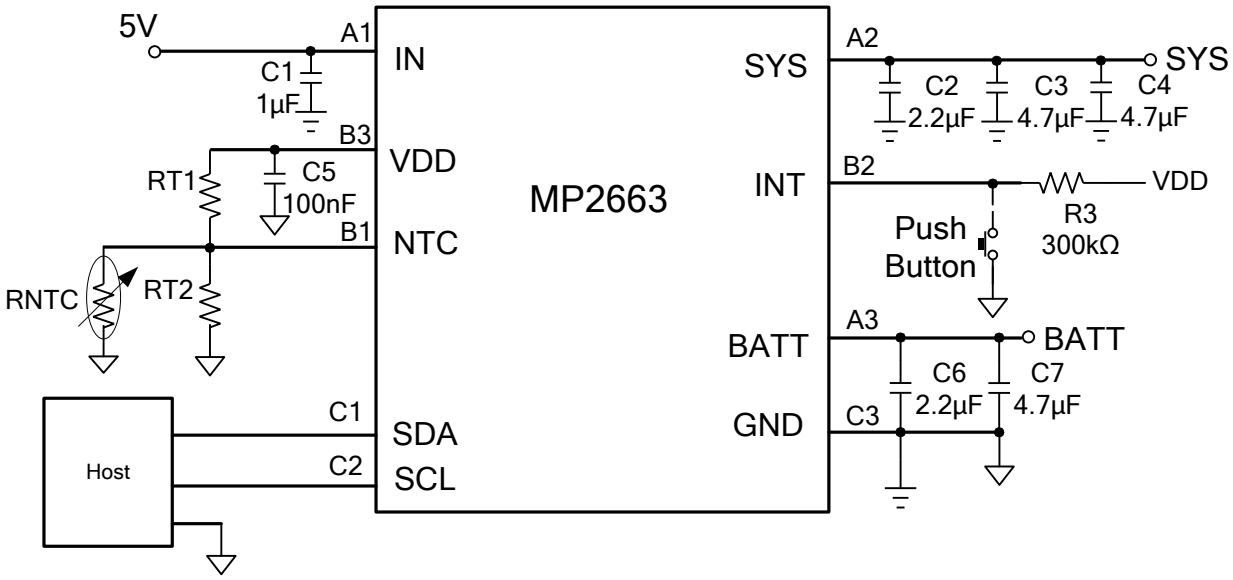


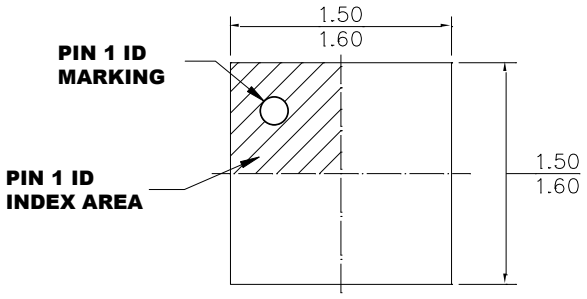
Figure 14: MP2663 Typical Application Circuit with 5V Input

Table 4: The Key BOM of Figure 14

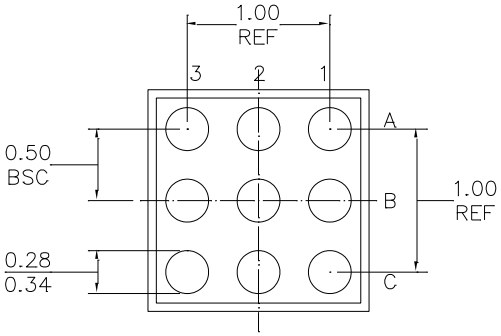
Qty	Ref	Value	Description	Package	Manufacture
1	C1	1µF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
2	C2, C6	2.2µF	Ceramic Capacitor;16V; X5R or X7R	0603	Any
1	C3, C4, C7	4.7µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C5	100nF	Ceramic Capacitor;16V; X5R or X7R	0603	Any

PACKAGE INFORMATION

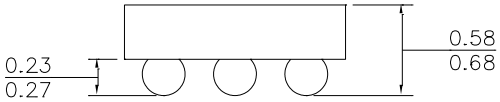
WLCSP-9 (1.55mmx1.55mm)



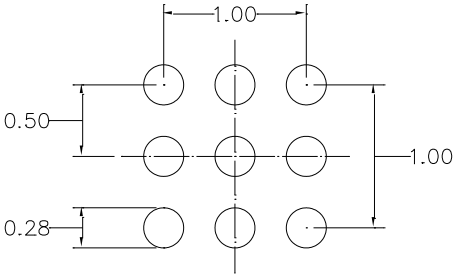
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.