

SN54ABT648, SN74ABT648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCB3016 D3706, JANUARY 1991

- State-Of-The-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Drive Outputs (–32-mA I_{OH} , 64-mA I_{OL})
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Package Options Include Plastic “Small Outline” Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CLKAB or CLKBA). Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'ABT648.

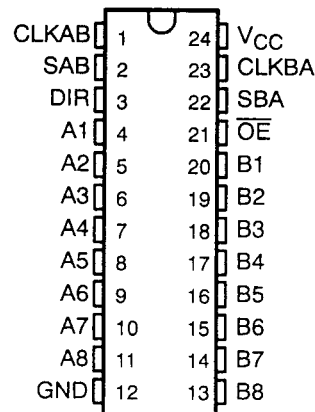
Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus will receive data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data may be stored in one register and/or B data may be stored in the other register.

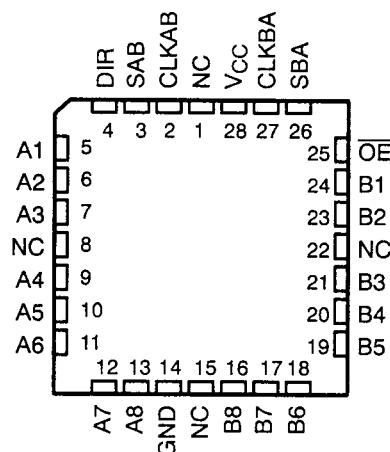
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54ABT648 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT648 is characterized for operation from -40°C to 85°C .

SN54ABT648 ... JT PACKAGE
SN74ABT648 ... DW OR NT PACKAGE
(TOP VIEW)



SN54ABT648 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCT PREVIEW

EPIC-IIB is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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WITH 3-STATE OUTPUTS

PRODUCT PREVIEW

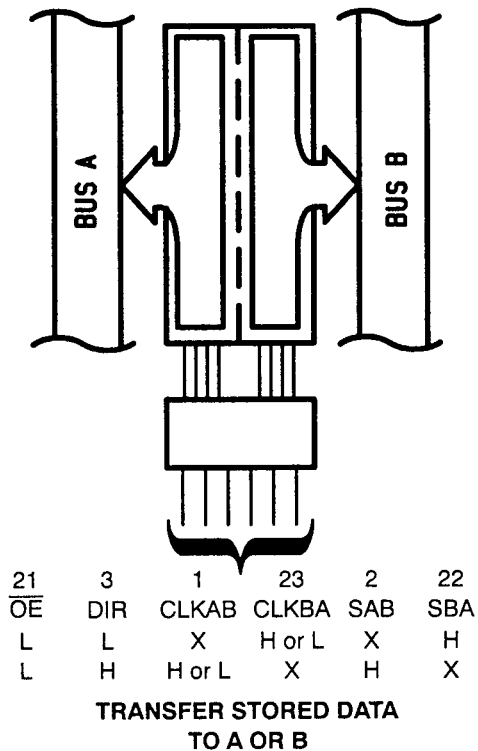
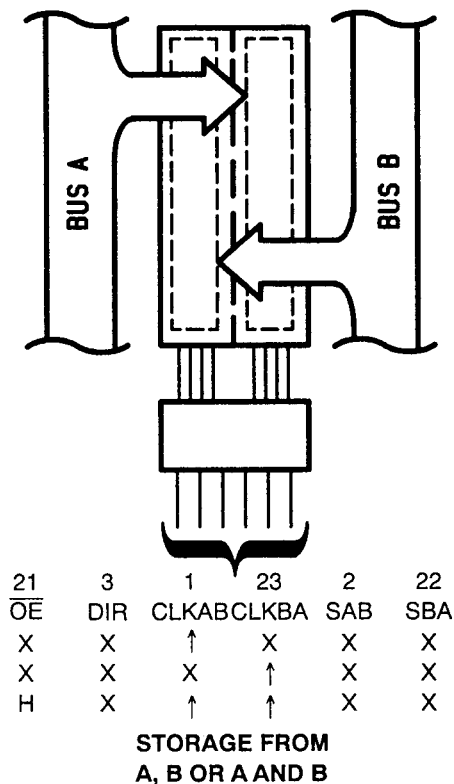
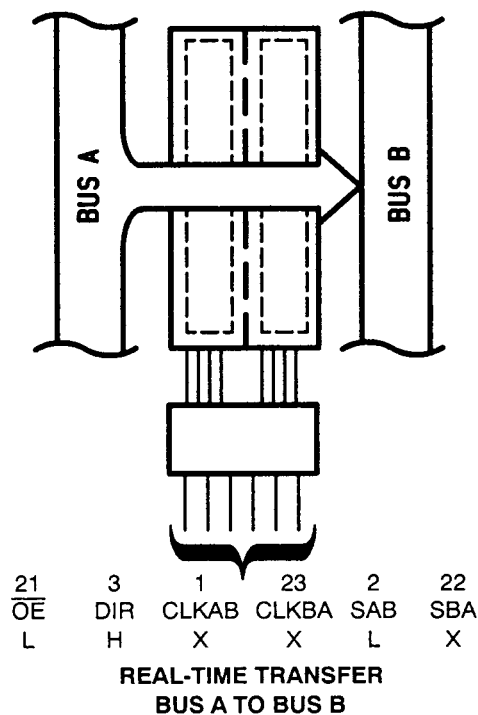
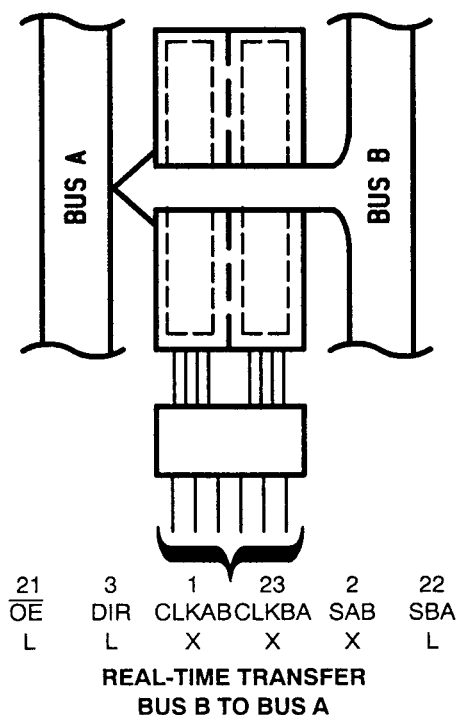


Figure 1. Bus-Management Functions

SN54ABT648, SN74ABT648

OCTAL BUS TRANSCEIVERS AND REGISTERS

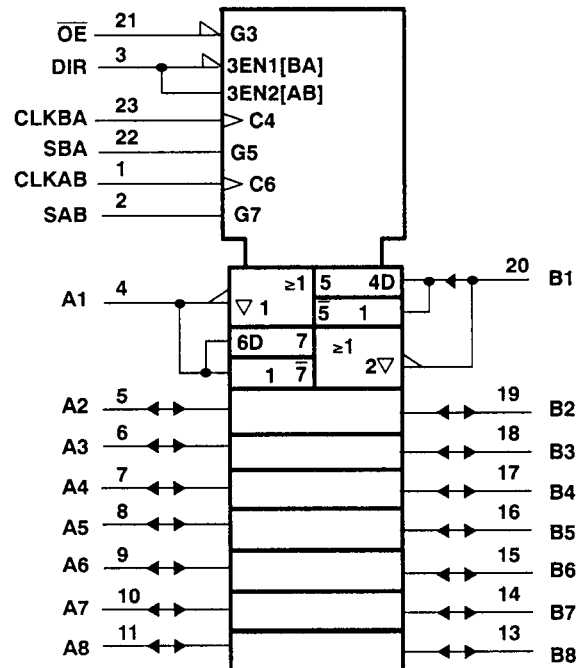
WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified [†]	Store A, B unspecified [†]
X	X	X	↑	X	X	Unspecified [†]	Input	Store B, A unspecified [†]
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X	Input	Input	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X	Input	Output	Store $\overline{A}$ Data to B Bus

[†] The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

logic symbol ‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for JT, DW, and NT packages.

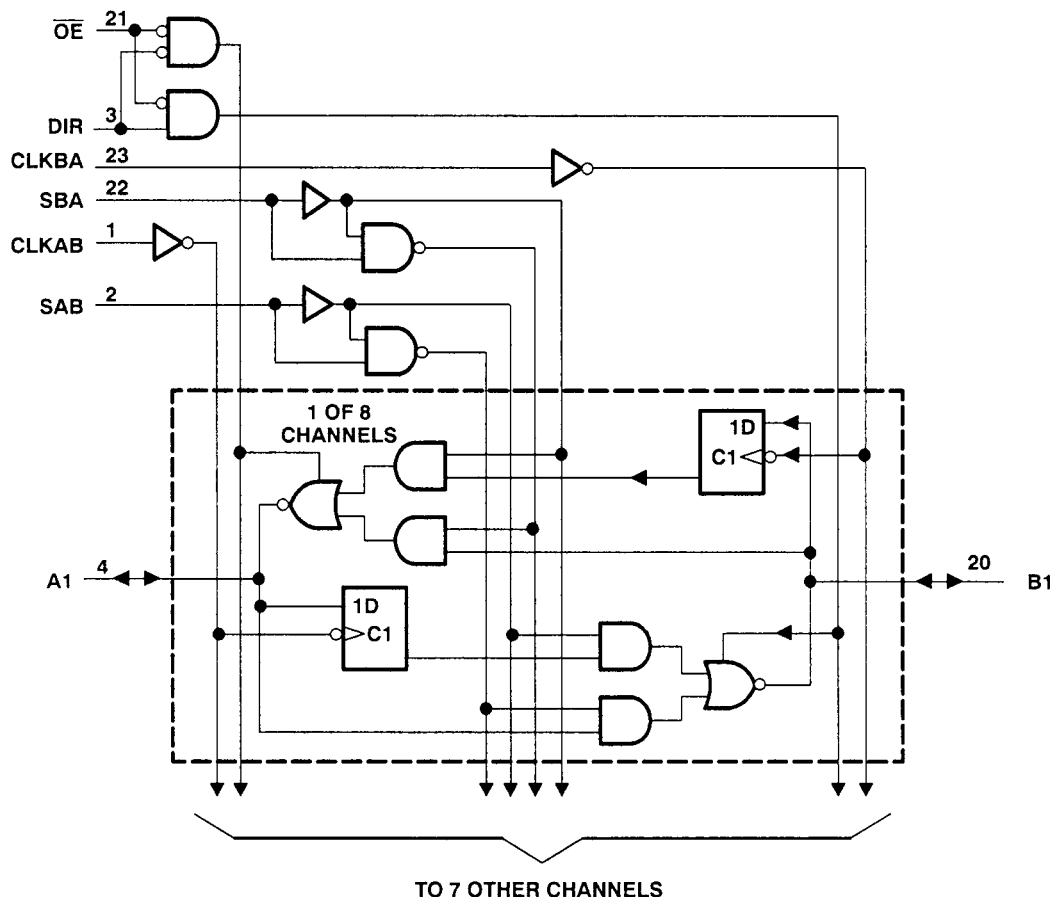
PRODUCT PREVIEW

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OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	−1.2 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1)	−1.2 V to 5.5 V
Voltage applied to any output in the high state or power-off state, V_O	−0.5 V to 5.5 V
Current into any output in the low state, I_O	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−18 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Storage temperature range	−65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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OCTAL BUS TRANSCEIVERS AND REGISTERS

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recommended operating conditions

		SN54ABT648		SN74ABT648		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		−24		−32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		5		5	ns/V
T _A	Operating free-air temperature	−55	125	−40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT648		SN74ABT648		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA			−1.2		−1.2		−1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = −3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = −3 mA	3			3		3		
	V _{CC} = 4.5 V, I _{OH} = −32 mA	2			2		2		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 48 mA				0.55				V
	V _{CC} = 4.5 V, I _{OL} = 64 mA						0.55		
I _I	V _{CC} = 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZH} ‡	V _{CC} = 5.5 V, V _O = 2.7 V			50		50		50	μA
I _{OZL} ‡	V _{CC} = 5.5 V, V _O = 0.5 V			−50		−50		−50	μA
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	−50	−100	−180	−50	−180	−50	−180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		1	50		50		μA
		Outputs low		24	30		30		mA
		Outputs disabled		0.5	50		50		μA
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	Control inputs	V _I = 2.5 V or 0.5 V							pF
C _{io}	A or B ports	V _O = 2.5 V or 0.5 V							pF

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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