

7 Channel DC/DC Converters

General Description

The RT9917 is a complete power-supply solution for digital still cameras and other hand-held devices.

It integrates :

CH1 : Boost DC-DC converter with load disconnect controller (SW1).

CH2 : Selectable Boost/Buck DC-DC converter

CH3 : Step-down DC-DC converter with internal compensation.

CH4 : Step-down DC-DC converter with internal compensation.

CH5 : DC/DC converter with HV NMOS, internal compensation and load disconnect (SW5) for CCD positive supply.

CH6 : DC/DC converter with HV PMOS for CCD negative supply.

CH7 : WLED driver with HV NMOS, internal compensation and allow for PWM dimming.

SW1 : Load disconnect controller for CH1.

SW5 : Load disconnect switch for CH5.

Ordering Information

RT9917 □ □

Package Type
QW : WQFN-40L 5x5 (W-Type)

Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

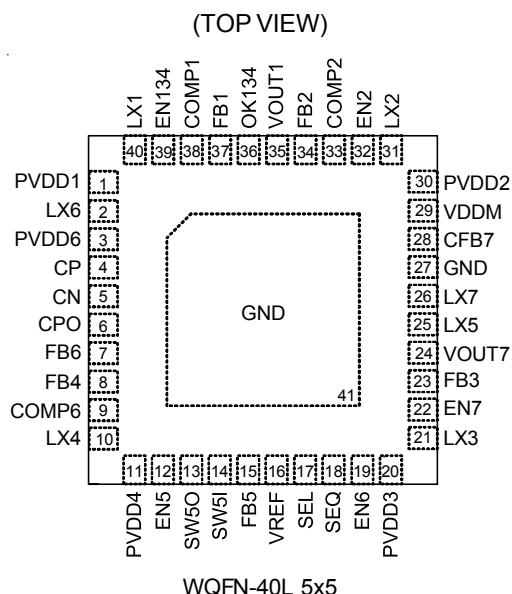
Features

- 1 Channel Boost/Buck Selectable by SEL Pin
- 2 Selectable On/Off Sequence Set by SEQ Pin
- 4 Channels with Internal Compensation
- Provide Charge Pump Voltage to Enhance NMOS Gate Driving Capability for Alkaline Battery Input
- All Power Switches Integrated
- Syn Step-Down DC/DC Converter
 - ▶ Up to 95% Efficiency
 - ▶ 100% (MAX) Duty Cycle
- Syn Step-Up DC/DC Converter
 - ▶ Adjustable Output Voltage
 - ▶ Up to 95% Efficiency
- Open LED Protection
- Transformerless Inverting Converter for CCD
- Fixed 1MHz Switching Frequency
- Compact 40-Lead WQFN Package
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

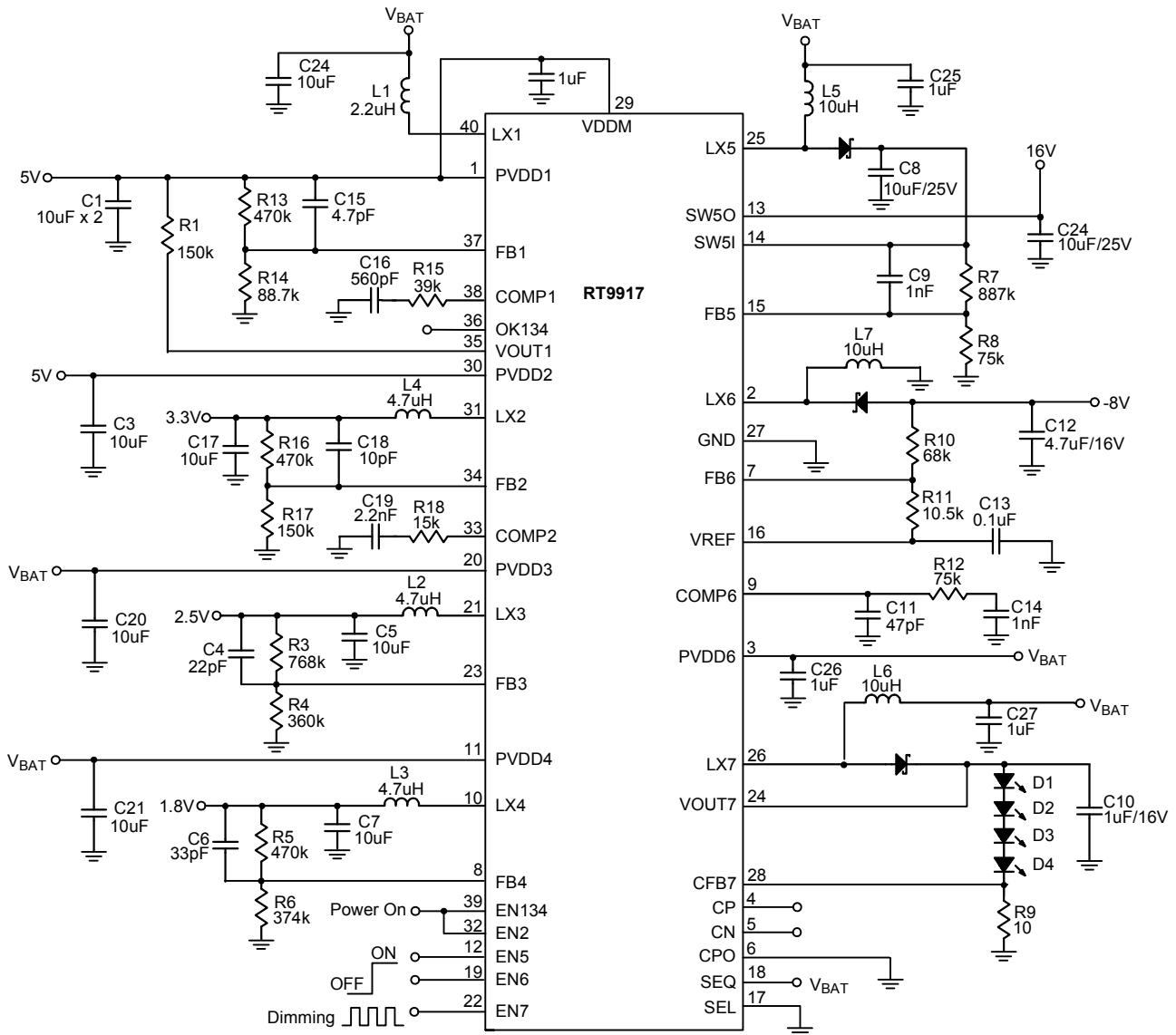
- Digital Still Camera
- PDA
- Portable Device

Pin Configurations



Typical Application Circuit

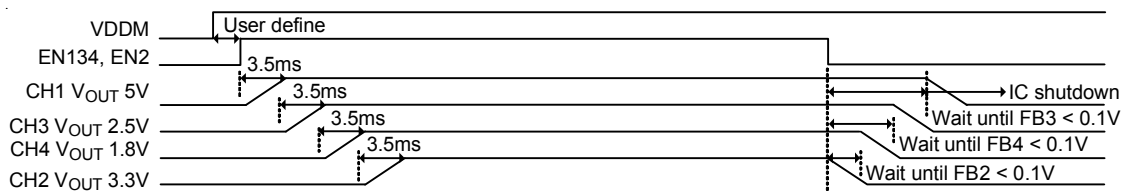
For Li-ion : CH2 3.3V is from V_{OUT} of CH1



Timing Diagram

Power On Sequence : CH1 Boost 5V → CH3 Buck 2.5V → CH4 Buck 1.8V → CH2 Buck 3.3V

Power Off Sequence : CH2 Buck 3.3V → CH4 Buck 1.8V → CH3 Buck 2.5V → CH1 Boost 5V



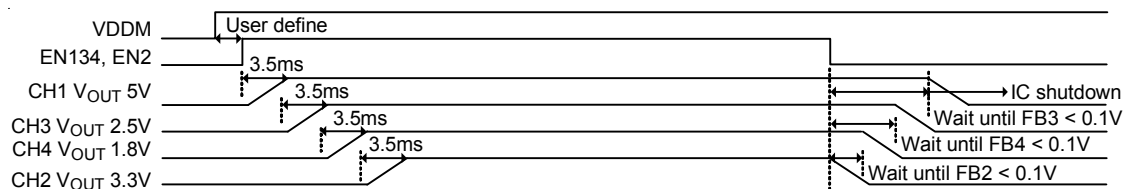
The schematic diagram illustrates the RT9917 LED driver IC, which is a multi-channel, constant-current LED driver. The IC is shown with its pin connections and associated passive components.

Pin Connections and Components:

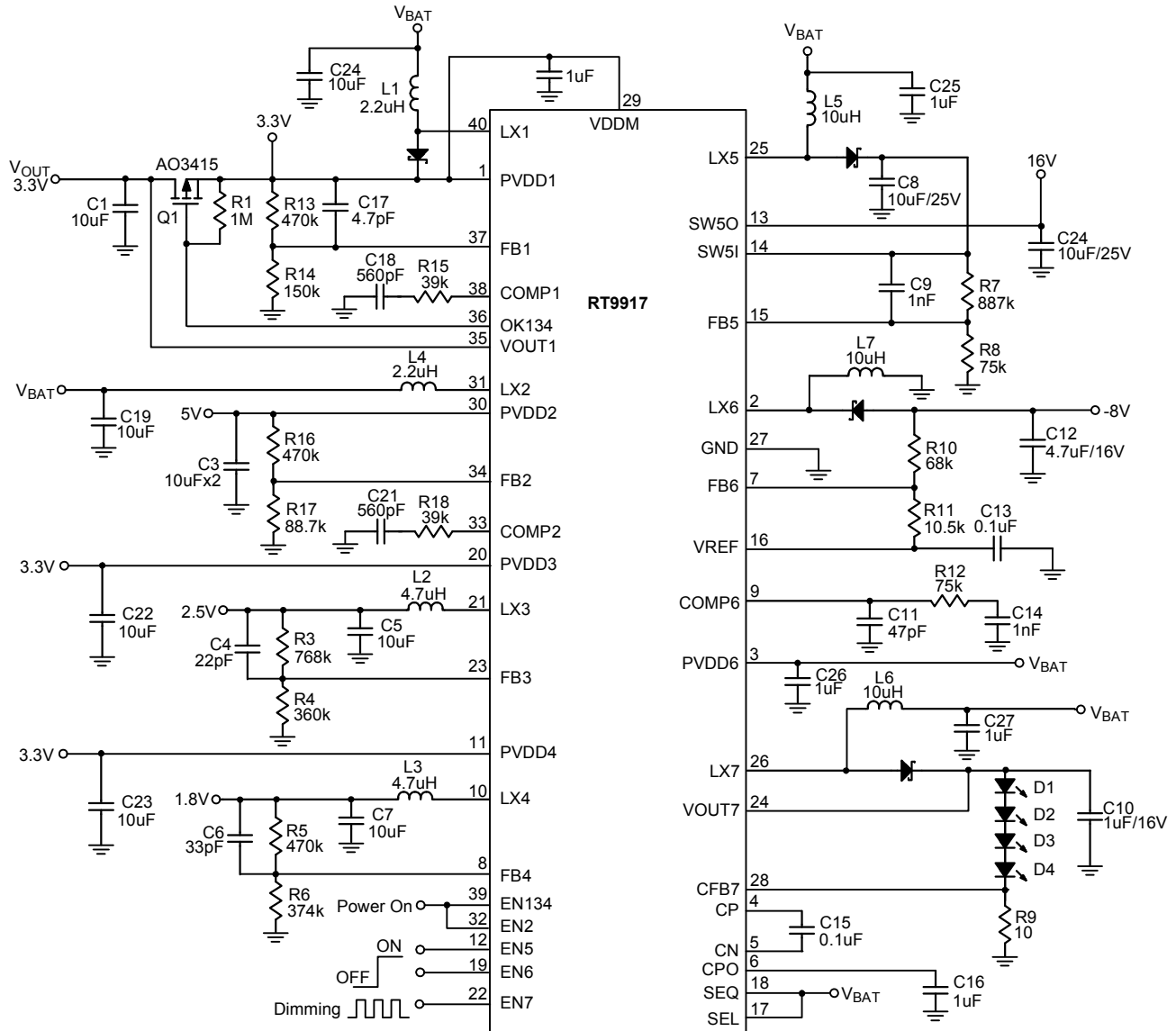
- VDDM (Pin 29):** Connected to VBAT via a 1uF capacitor.
- LX1 (Pin 40):** Connected to VBAT via a 2.2uH inductor (L1) and a 10uF capacitor (C24).
- PVDD1 (Pin 1):** Connected to a 5V source via a 10uF x 2 capacitor (C1) and a 150k resistor (R1).
- FB1 (Pin 37):** Connected to a feedback network consisting of resistors R13 (470k), R14 (88.7k), and R15 (39k), and capacitors C15 (4.7pF) and C16 (560pF).
- COMP1 (Pin 38):** Connected to a feedback network consisting of resistors R16 (470k), R17 (150k), and R18 (15k), and capacitors C17 (10uF) and C18 (10pF).
- OK134 (Pin 36):** Connected to a feedback network consisting of resistors R19 (15k) and R20 (15k), and capacitors C19 (2.2nF) and C20 (10uF).
- VOUT1 (Pin 35):** Connected to a feedback network consisting of resistors R21 (15k) and R22 (15k), and capacitors C21 (10uF) and C22 (10pF).
- PVDD2 (Pin 30):** Connected to a 3.3V source via a 10uF capacitor (C3).
- LX2 (Pin 31):** Connected to a 3.3V source via a 4.7uH inductor (L4) and a 10uF capacitor (C17).
- FB2 (Pin 34):** Connected to a feedback network consisting of resistors R23 (470k), R24 (150k), and R25 (15k), and capacitors C18 (10pF) and C19 (2.2nF).
- COMP2 (Pin 33):** Connected to a feedback network consisting of resistors R26 (470k), R27 (150k), and R28 (15k), and capacitors C20 (10uF) and C21 (10pF).
- PVDD3 (Pin 20):** Connected to a 2.5V source via a 10uF capacitor (C20).
- LX3 (Pin 21):** Connected to a 2.5V source via a 4.7uH inductor (L2) and a 10uF capacitor (C5).
- FB3 (Pin 23):** Connected to a feedback network consisting of resistors R29 (768k), R30 (360k), and R31 (15k), and capacitors C4 (22pF) and C5 (10uF).
- PVDD4 (Pin 11):** Connected to a 1.8V source via a 10uF capacitor (C21).
- LX4 (Pin 10):** Connected to a 1.8V source via a 4.7uH inductor (L3) and a 10uF capacitor (C7).
- FB4 (Pin 8):** Connected to a feedback network consisting of resistors R32 (470k), R33 (374k), and R34 (15k), and capacitors C6 (33pF) and C7 (10uF).
- EN1 (Pin 39):** Connected to a "Power On" signal.
- EN2 (Pin 32):** Connected to a "Power On" signal.
- EN5 (Pin 12):** Connected to a "Power On" signal.
- EN6 (Pin 19):** Connected to a "Power On" signal.
- EN7 (Pin 22):** Connected to a "Dimming" signal.
- CPO (Pin 6):** Connected to a "Power On" signal.
- SEQ (Pin 18):** Connected to a "Power On" signal.
- SEL (Pin 17):** Connected to a "Power On" signal.

RT9917

Power Off Sequence : CH2 Buck 3.3V → CH4 Buck 1.8V → CH3 Buck 2.5V → CH1 Boost 5V



For 2AA

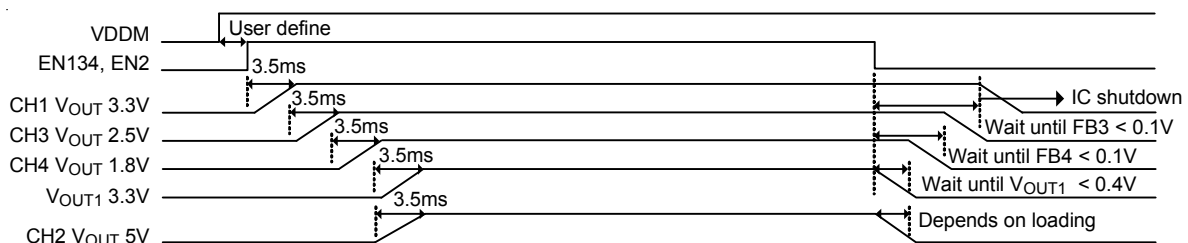


Note : A schottky diode connect from LX1 to PVDD1 is required for low-voltage start up.

Timing Diagram

Power On Sequence : CH1 Boost 3.3V → CH3 Buck 2.5V → CH4 Buck 1.8V → (CH2 Boost 5V and SW1 3.3V)

Power Off Sequence : (CH2 Boost 5V and SW1 3.3V) → CH4 Buck 1.8V → CH3 Buck 2.5V → CH1 Boost 3.3V



Channel	CH3				
Formula	$V_{OUT} = (1+R3/R4) \times 0.8$				
V_{OUT} (V)	2.5	1.8	1.3	1.2	1.0
L(uH)	4.7	4.7	4.7	4.7	4.7
R3(k Ω)	768	470	237	187	23.2
R4(k Ω)	360	374	374	374	93.1
C4(pF)	22	33	68	82	47
C _{OUT} (uF)	10	10	10	10	10

Channel	CH4				
Formula	$V_{OUT} = (1+R5/R6) \times 0.8$				
V_{OUT} (V)	2.5	1.8	1.3	1.2	1.0
L(uH)	4.7	4.7	4.7	4.7	4.7
R5(k Ω)	768	470	237	187	23.2
R6(k Ω)	360	374	374	374	93.1
C6(pF)	22	33	68	82	47
C _{OUT} (uF)	10	10	10	10	10

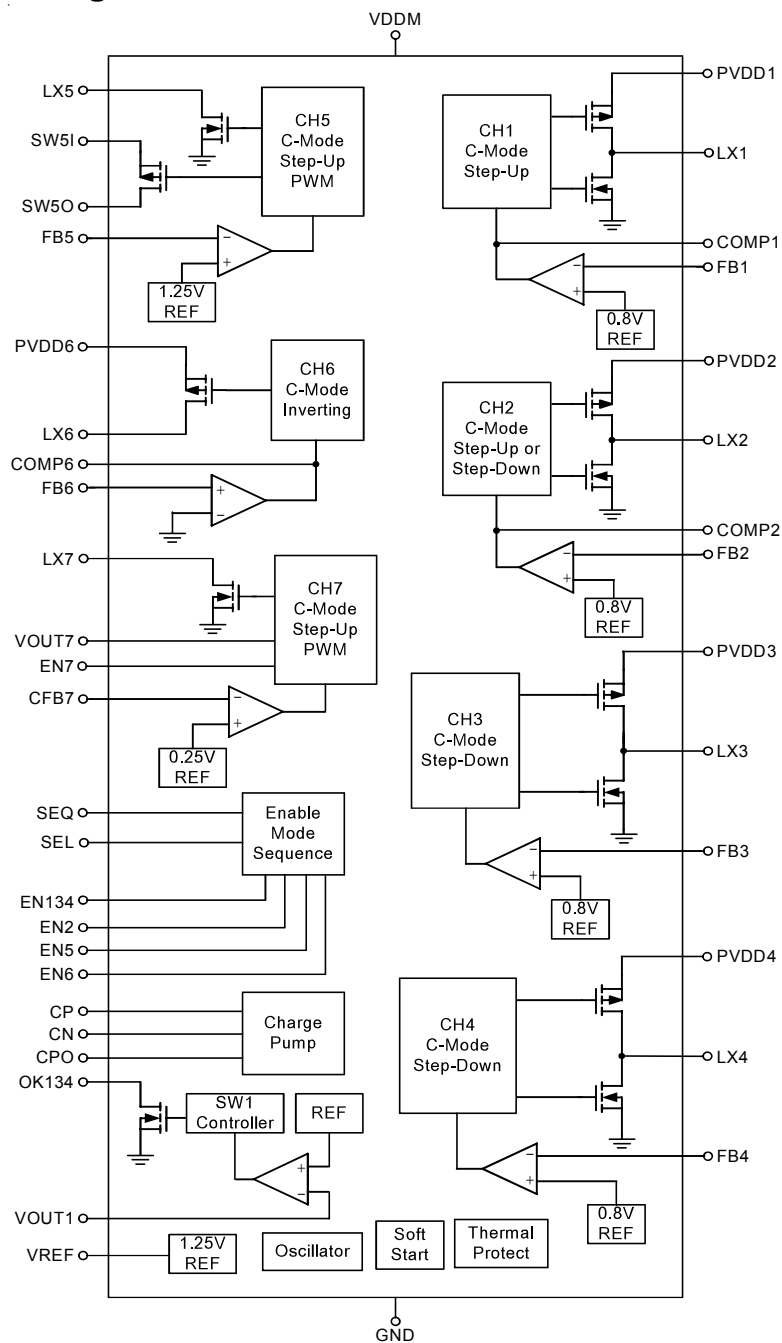
Channel	CH5				
Formula	$V_{OUT} = (1+R7/R8) \times 1.25$				
V_{OUT} (V)	12	13	15	15.5	16
L(uH)	10	10	10	10	10
R7(k Ω)	820	820	1000	820	886
R8(k Ω)	95.3	86.6	90.9	71.5	75
C9(pF)	1000	1000	1000	1000	1000
C _{OUT} (uF)	10/16V	10/16V	10/25V	10/25V	10/25V

Channel	CH6				
Formula	$V_{OUT} = (R10/R11) \times (-1.25)$ * R10+R11 <90k				
V_{OUT} (V)	-6	-6.3	-7	-7.5	-8
L(uH)	10	10	10	10	10
R10(k Ω)	57.6	69.8	63.4	68	68
R11(k Ω)	12	13.7	11.3	11.3	10.5
C _{OUT} (uF)	10/16V	10/16V	4.7/16V	4.7/16V	4.7/16V
R12(k Ω)	47	47	75	75	75
C11(pF)	47	47	47	47	47
C14(pF)	1000	1000	1000	1000	1000

Functional Pin Description

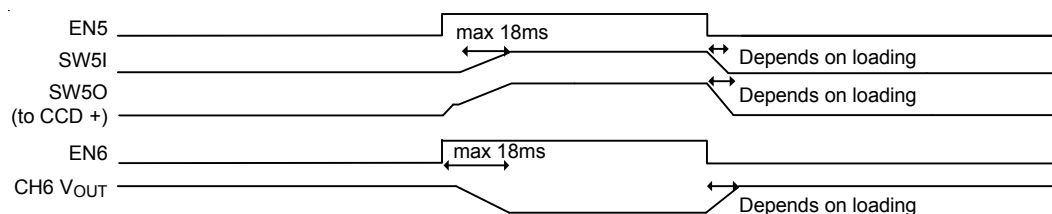
Pin No.	Pin Name	Pin Function
1	PVDD1	Power Input Pin for CH1.
2	LX6	Switch Node of CH6. High impedance in shutdown.
3	PVDD6	Power Input Pin for CH6.
4	CP	Charge Pump External Driver Pin.
5	CN	Charge Pump External Driver Pin.
6	CPO	Output Pin for Charge Pump.
7	FB6	Feedback Input Pin for CH6. High impedance in shutdown.
8	FB4	Feedback Input Pin for CH4. High impedance in shutdown.
9	COMP6	Compensation Pin for CH6. Pull to GND in shutdown.
10	LX4	Switch Node for CH4. High impedance in shutdown.
11	PVDD4	Power Input Pin for CH4.
12	EN5	Enable Pin for CH5.
13	SW5O	Output Pin for CH5 Load Disconnect.
14	SW5I	Input Pin for CH5 Load Disconnect.
15	FB5	Feedback Input Pin for CH5. High impedance in shutdown.
16	VREF	1.25V Reference Output Pin.
17	SEL	CH2 Boost/Buck Select Pin. Logic state can't be changed during operation.
18	SEQ	CH1, CH3, CH4 Power On/Off Sequence Setting Pin. Logic state can't be changed during operation.
19	EN6	Enable Pin for CH6.
20	PVDD3	Power Input Pin for CH3
21	LX3	Switch Node for CH3. High impedance in shutdown.
22	EN7	Enable Pin for CH7.
23	FB3	Feedback Input Pin for CH3. High impedance in shutdown.
24	VOU7	Sense Pin for CH7 Output Voltage.
25	LX5	Switch Node for CH5. High impedance in shutdown.
26	LX7	Switch Node for CH7. High impedance in shutdown.
27, 41 (Exposed Pad)	GND	Analog GND Pin. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
28	CFB7	Feedback Input Pin for CH7.
29	VDDM	IC analog Input Power Pin. This voltage is also used to drive power NMOS gate of CH5 and CH7.
30	PVDD2	Power Input Pin for CH2.
31	LX2	Switch Node for CH2. High impedance in shutdown.
32	EN2	Enable Pin for CH2
33	COMP2	Compensation Pin for CH2
34	FB2	Feedback Input Pin for CH2. High impedance in shutdown.
35	VOU1	Sense Pin for CH1 Output Voltage. High impedance in shutdown.
36	OK134	External Switch Control Pin. High impedance in shutdown.
37	FB1	Feedback Input Pin for CH1. High impedance in shutdown.
38	COMP1	Compensation Pin for CH1. Pull to GND in shutdown.
39	EN134	Enable Pin for CH1, CH3, CH4, SW 1.
40	LX1	Switch Node for CH1. High impedance in shutdown.

Function Block Diagram



Timing Diagram

CH5 and CH6 Timing Diagram



Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{DDM} ----- 0.3V to 7V
- Power Input PVDD1, PVDD2, PVDD3, PVDD4, PVDD6 ----- -0.3V to 7V
- Switch node :
 - LX1, LX2, LX3, LX4 ----- -0.3V to 7V
 - LX5, LX7, SW5I, SW5O, VOUT7 ----- -0.3V to 21V
 - LX6 ----- (PVDD6 – 14V) to (PVDD6 + 0.3V)
- The Other Pins ----- -0.3V to 7V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
 - WQFN 40L 5x5 ----- 2.778W
- Package Thermal Resistance (Note 2)
 - WQFN 40L 5x5, θ_{JA} ----- 36°C/W
 - WQFN 40L 5x5, θ_{JC} ----- 7°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
 - HBM (Human Body Mode) ----- 2kV
 - MM (Machine Mode) ----- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{DDM} ----- 2.7V to 5.5V
- EN7 Dimming Control Frequency Range for CH7 ----- 1kHz to 100kHz
(avoid 2k to 20kHz for audio noise)
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics(VDDM = 3.3V, $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage						
VDDM Minimum Startup Voltage	V_{ST}		--	--	1.6	V
VDDM Over Voltage Protection			5.6	6	6.5	V
VDDM Over Voltage Protection Hysteresis			--	--	0.6	V
Supply Current						
Shutdown Supply Current into VDDM	I_{OFF}	EN134 = EN2 = EN5 = EN6 = EN7 = 0V	--	1	10	μA
CH1 (Syn-Boost) + SW1 : Supply Current into VDDM	I_{Q1}	Non Switching, EN134 = 3.3V	--	--	800	μA
CH2 (Syn-Boost or Syn-Buck) : Supply Current into VDDM	I_{Q2}	Non Switching, EN2 = 3.3V	--	--	800	μA
CH3 (Syn-Buck) : Supply Current into VDDM	I_{Q3}	Non Switching, EN134 = 3.3V	--	--	800	μA

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CH4 (Syn-Buck) : Supply Current into VDDM	I_{Q4}	Non Switching, EN134 = 3.3V	--	--	800	μA
CH5 (Asyn-Boost) + SW5 : Supply Current into VDDM	I_{Q5}	Non Switching, EN5 = 3.3V	--	--	800	μA
CH6 (Inverting) + Charge pump Supply Current into VDDM	I_{Q6}	Non Switching, EN6 = 3.3V PVDD6 = 3.3V	--	--	800	μA
CH7 (WLED): Supply Current into VDDM	I_{Q7}	Non Switching, EN7 = 3.3V	--	--	800	μA
Oscillator						
CH1,2,3,4,5,6,7 Operating Frequency	f_{OSC}		900	1000	1100	kHz
CH1 Maximum Duty Cycle (Boost)		$V_{FB1} = 0.7V$	80	83	86	%
CH2 Maximum Duty Cycle (Boost)		$V_{FB2} = 0.7V$	80	83	86	%
CH2 Maximum Duty Cycle (Buck)		$V_{FB2} = 0.7V$	--	--	100	%
CH3 Maximum Duty Cycle (Buck)		$V_{FB3} = 0.7V$	--	--	100	%
CH4 Maximum Duty Cycle (Buck)		$V_{FB4} = 0.7V$	--	--	100	%
CH5 Maximum Duty Cycle (Boost)		$V_{FB5} = 1.15V$	91	94	97	%
CH6 Maximum Duty Cycle (Inverting)		$V_{FB6} = 0.1V$	91	94	97	%
CH7 Maximum Duty Cycle (WLED)		$C_{FB7} = 0.15V$	91	94	97	%
Feedback Regulation Voltage						
Feedback Regulation Voltage @ FB1, FB2, FB3, FB4			0.788	0.8	0.812	V
Feedback Regulation Voltage @ FB5			1.237	1.25	1.263	V
Feedback Regulation Voltage @ FB6			-15	0	15	mV
Feedback Regulation Voltage @ CFB7			0.237	0.25	0.263	V
OK134 Sink Current		OK134 = 1V	--	140	--	μA
Reference						
VREF Output Voltage	V_{REF}		1.237	1.25	1.263	V
VREF Load Regulation		$0\mu A < I_{REF} < 200\mu A$	--	--	10	mV
Power Switch						
CH1 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD1 = 3.3V	--	150	--	m Ω
		N-MOSFET, PVDD1 = 3.3V	--	150	--	m Ω
CH1 Current Limitation (Boost)		N-MOSFET, PVDD1 = 3.3V	--	3	--	A
CH2 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD2 = 3.3V	--	150	--	m Ω
		N-MOSFET, PVDD2 = 3.3V	--	150	--	m Ω
CH2 Current Limitation (Buck)		P-MOSFET, PVDD2 = 3.3V	--	1.5	--	A
CH2 Current Limitation (Boost)		N-MOSFET, PVDD2 = 3.3V	--	3	--	A
CH3 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD3 = 3.3V	--	200	--	m Ω
		N-MOSFET, PVDD3 = 3.3V	--	200	--	m Ω
CH3 Current Limitation (Buck)		P-MOSFET, PVDD3 = 3.3V	--	1.5	--	A

To be continued

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
CH4 On Resistance of MOSFET	$R_{DS(ON)}$	P-MOSFET, PVDD4 = 3.3V	–	200	–	m Ω
		N-MOSFET, PVDD4 = 3.3V	–	200	–	m Ω
CH4 Current Limitation (Buck)		P-MOSFET, PVDD4 = 3.3V	–	1.5	–	A
CH5 Load Disconnect MOSFET		P-MOSFET, SW5I = 3.3V	–	0.5	–	Ω
CH5 On Resistance of MOSFET		N-MOSFET, VDDM = 3.3V	–	0.5	–	Ω
CH5 Current Limitation		N-MOSFET, VDDM = 3.3V	–	1.5	–	A
CH6 On Resistance of MOSFET		P-MOSFET, PVDD6 = 3.3V	–	1	–	Ω
CH6 Current Limitation		P-MOSFET, PVDD6 = 3.3V	–	1.5	–	A
CH7 On Resistance of MOSFET		N-MOSFET, VDDM = 3.3V	–	0.5	–	Ω
CH7 Current Limitation		N-MOSFET, VDDM = 3.3V	–	0.8	–	A
Protection						
Over Voltage Protection of PVDD1			–	6	–	V
Over Voltage Protection of PVDD2			–	6	–	V
Under Voltage Protection of VOUT1			–	1.75	–	V
Over Voltage Protection of SW5I			–	19	–	V
Over Voltage Protection of VOUT7			–	19	–	V
CH5 Load Disconnect UVP of SW5O			–	0.4	–	V
Control						
EN134, EN2, EN5, EN6, EN7 Input High Level Threshold			–	0.8	1.3	V
EN134, EN2, EN5, EN6, EN7 Input Low Level Threshold			0.4	0.8	–	V
EN134, EN2, EN5, EN6, EN7 Sink Current			–	2	6	μ A
SEQ SEL Input High Level Threshold			1.3	–	–	V
SEQ SEL Input Low Level Threshold			–	–	0.4	V
SEQ SEL Sink Current		EN134 or EN2 or EN5 or EN6 or EN7 = 3.3V	–	6	18	μ A
SEQ SEL Sink Current		EN134 = EN2 = EN5 = EN6 = EN7 = 0V	–	0	0.1	μ A
Thermal Protection						
Thermal Shutdown	T_{SD}		125	160	–	$^{\circ}$ C
Thermal Shutdown Hysteresis	ΔT_{SD}		–	20	–	$^{\circ}$ C

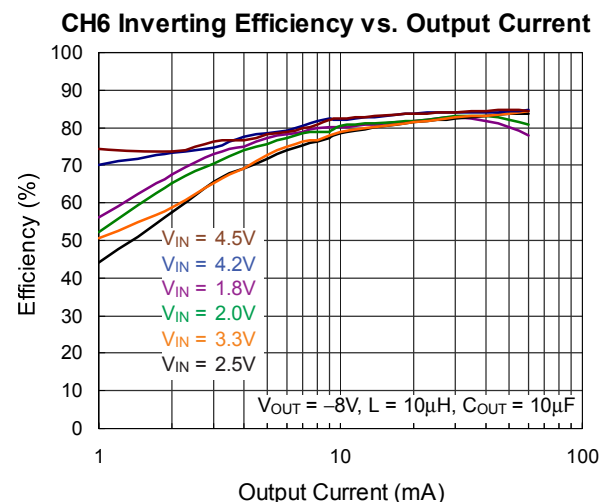
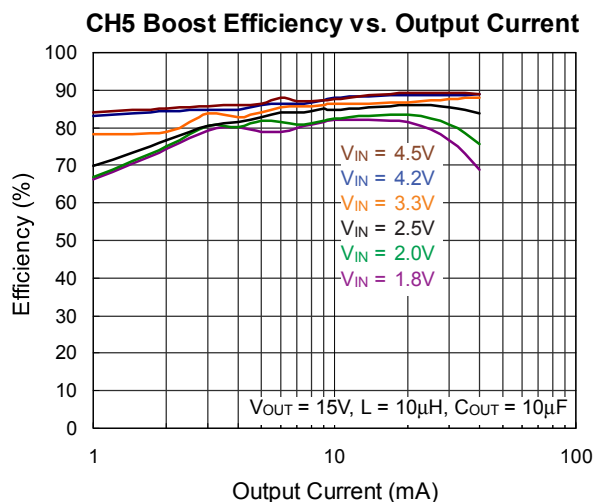
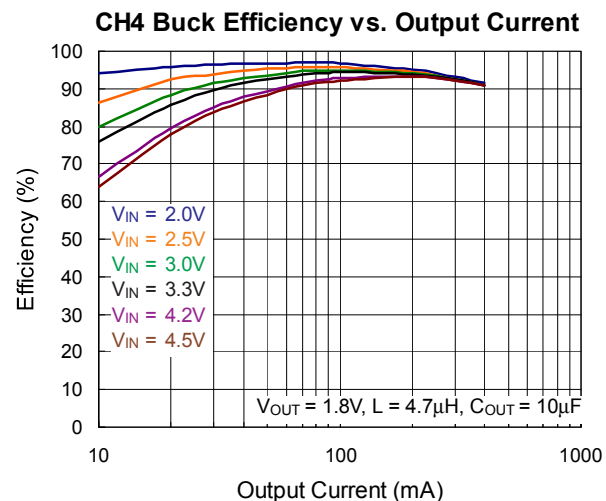
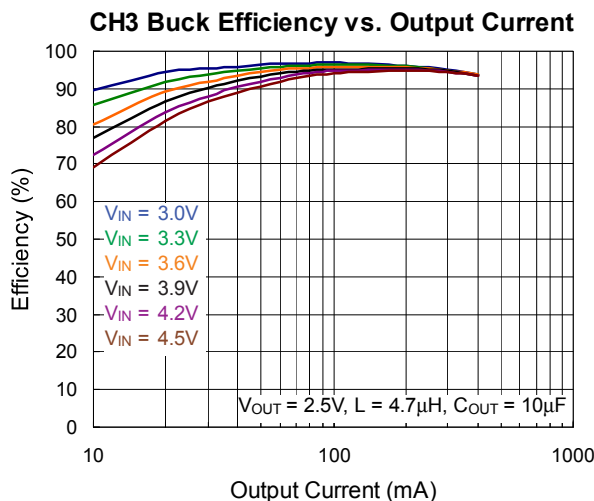
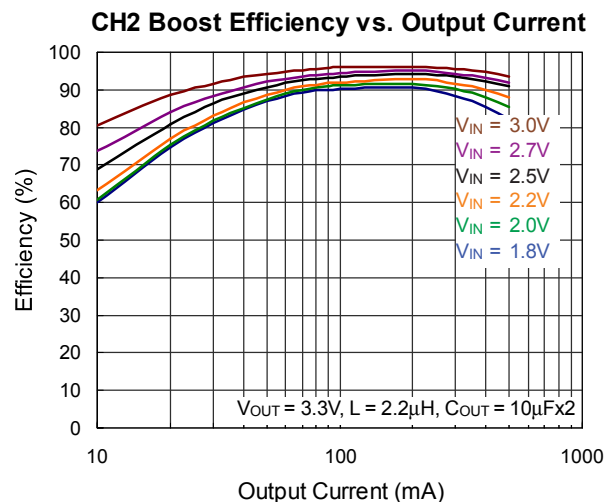
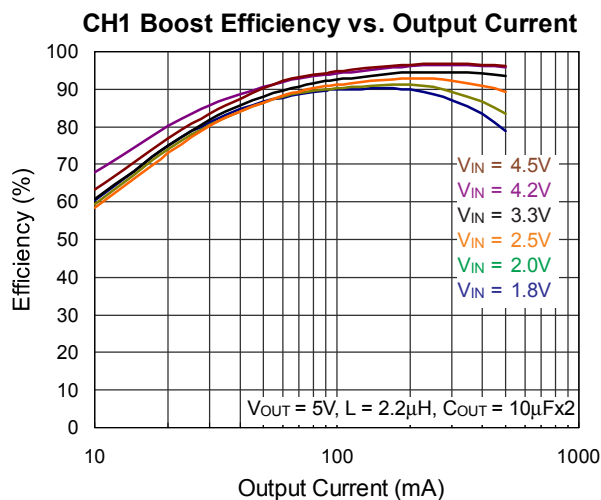
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

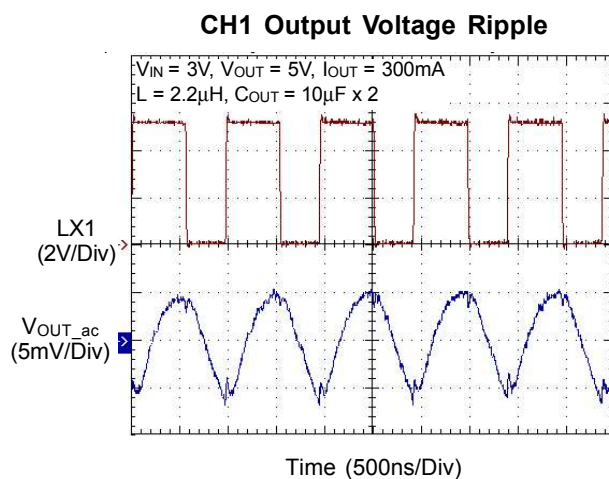
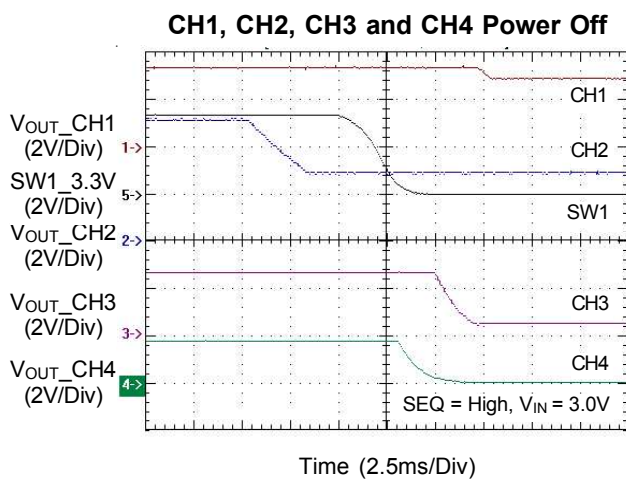
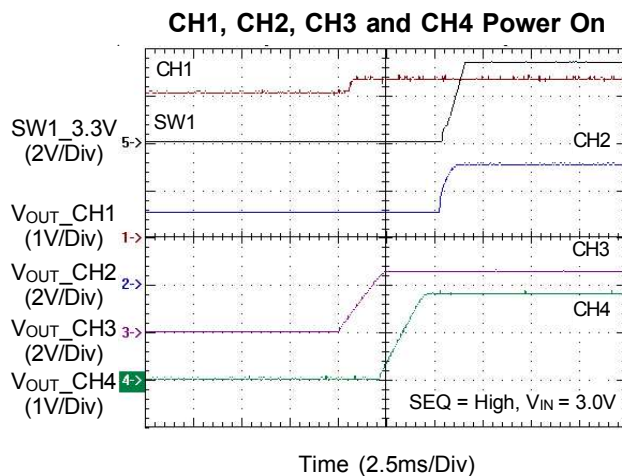
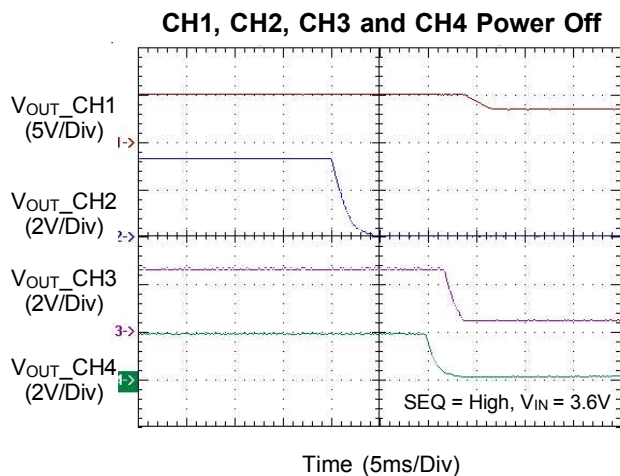
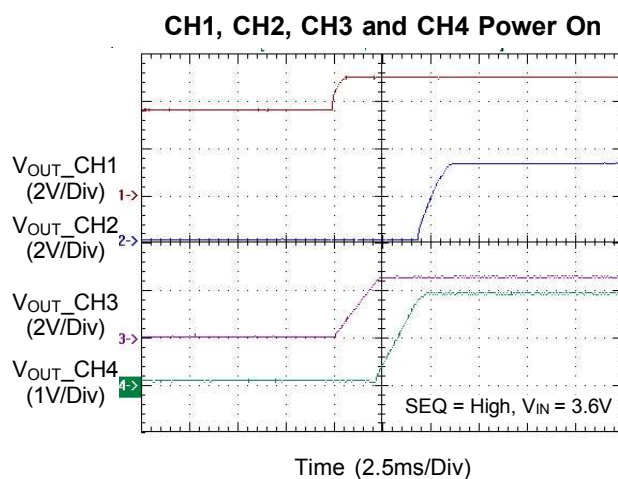
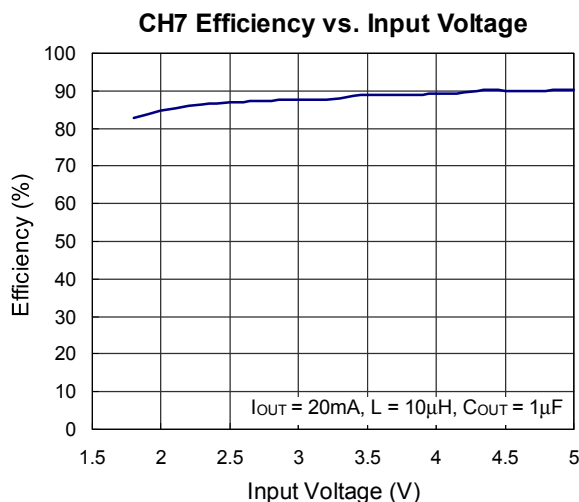
Note 2. θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}$ C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

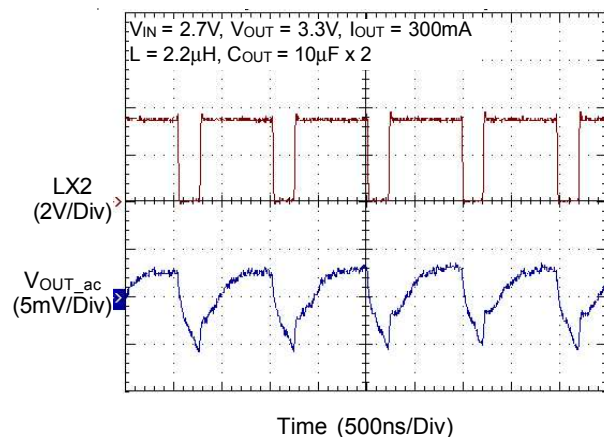
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

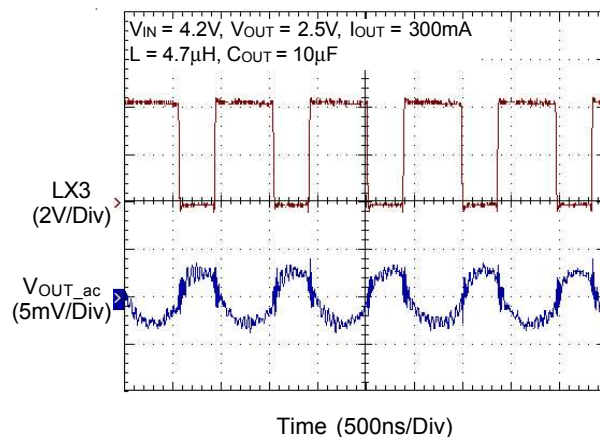




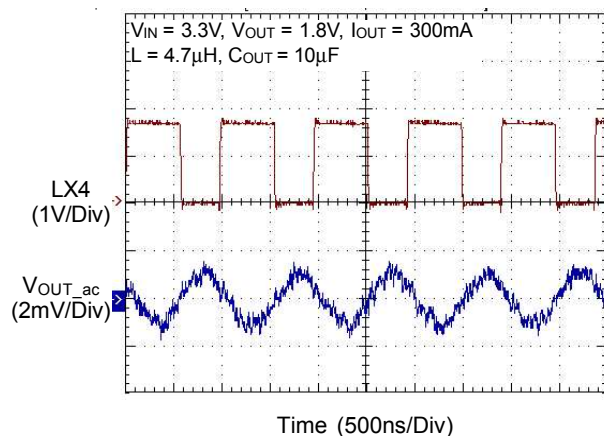
CH2 Output Voltage Ripple



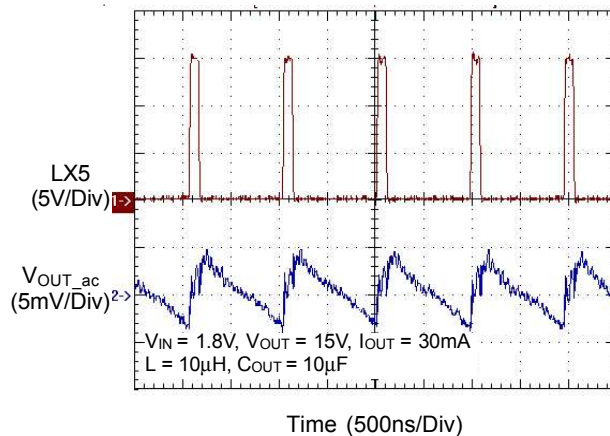
CH3 Output Voltage Ripple



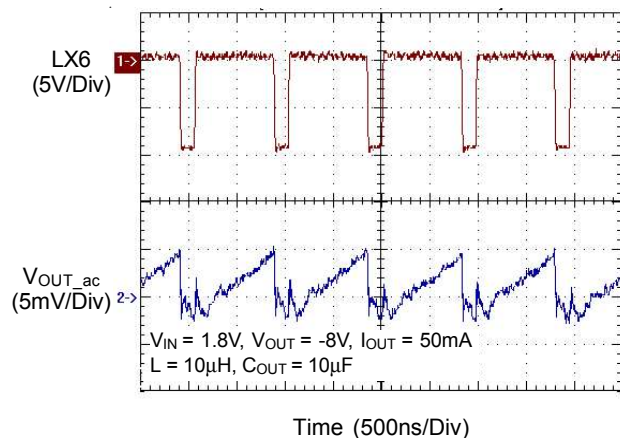
CH4 Output Voltage Ripple



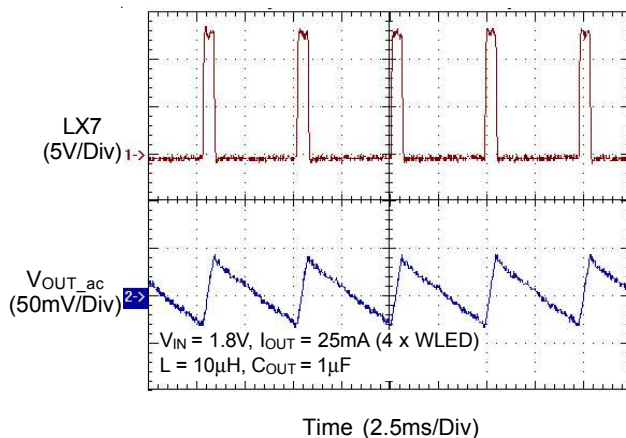
CH5 Output Voltage Ripple



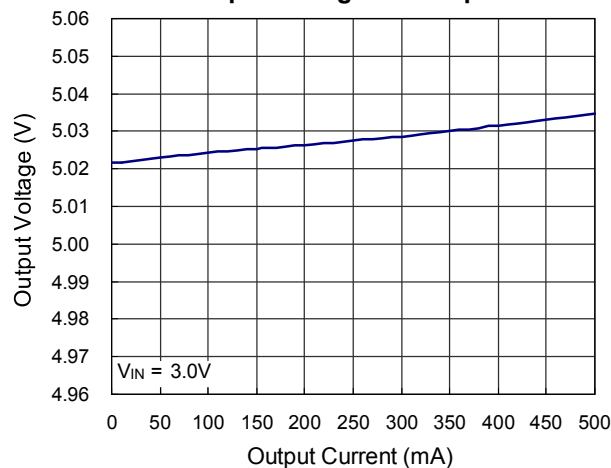
CH6 Output Voltage Ripple



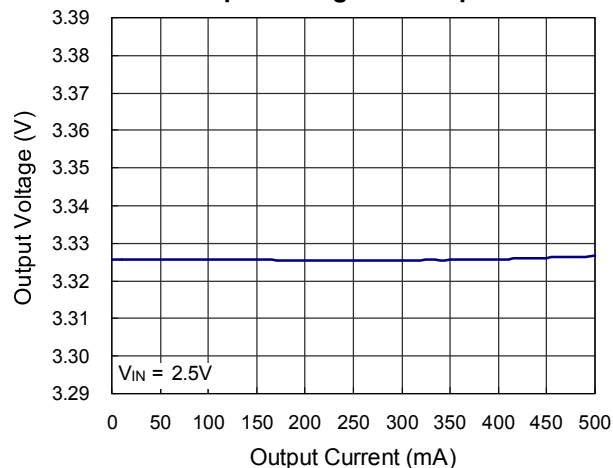
CH7 Output Voltage Ripple



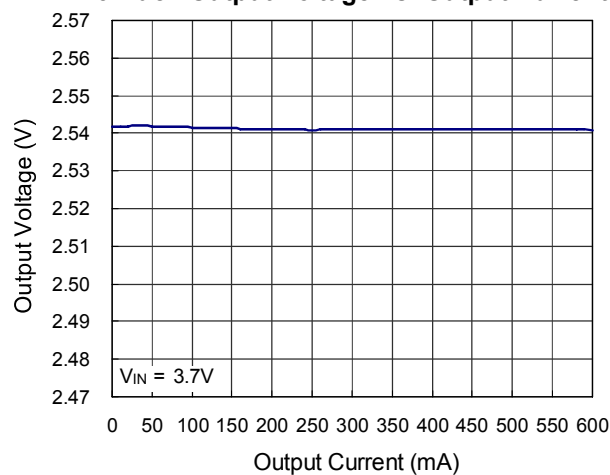
CH1 Boost Output Voltage vs. Output Current



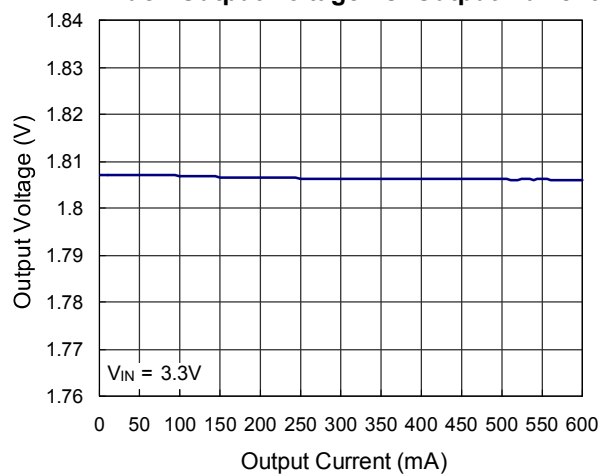
CH2 Boost Output Voltage vs. Output Current



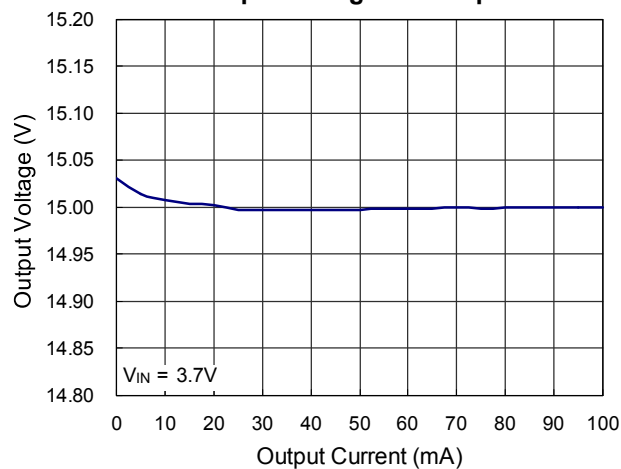
CH3 Buck Output Voltage vs. Output Current



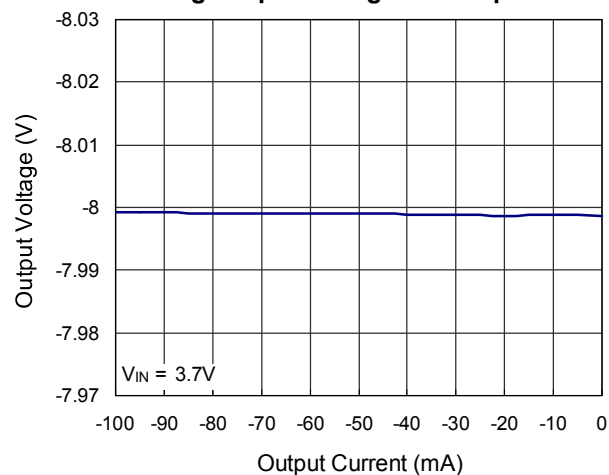
CH4 Buck Output Voltage vs. Output Current



CH5 Boost Output Voltage vs. Output Current



CH6 Inverting Output Voltage vs. Output Current



Application information

The RT9917 includes the following seven DC/DC converter channels to build a multiple-output power-supply system.

CH1 : Step-up synchronous current mode DC/DC converter with internal power MOSFETs. The output voltage could be load disconnected by a switch controller and an external PMOS.

CH2 : Selectable step-up or step-down synchronous current mode DC/DC converter with internal power MOSFETs.

CH3 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and internal compensation network.

CH4 : Step-down synchronous current mode DC/DC converter with internal power MOSFETs and internal compensation network.

CH5 : Step-up asynchronous current mode DC/DC converter with internal power MOSFET and internal compensation network. The output voltage could be load disconnected by an internal PMOS.

CH6 : Inverting current mode DC/DC converter with internal power MOSFET.

CH7 : Current mode WLED driver with internal power MOSFET and internal compensation network. Also provides open LED protection.

SW1 : Load disconnect controller for CH1.

SW5 : Load disconnect switch for CH5

All converters operate in PWM mode with 1MHz constant frequency under moderate to heavy loading. The RT9917 also provides two different on/off sequences by setting "SEQ" pin.

CH1 : Step-Up Converter

Step-up : The converter operates at fixed frequency PWM mode and continuous current mode (CCM) with internal MOSFET and synchronous rectifier for up to 95% efficiency.

Add a SBD between LX1 and PVDD1 for 2AA battery application.

CH2 : Selectable Step-Up or Step-Down Converter

Step-up : The converter operates at fixed frequency PWM mode and continuous current mode (CCM) with internal MOSFET and synchronous rectifier for up to 95% efficiency.

Step-down : The converter operates at fixed frequency PWM mode and continuous current mode (CCM) with internal MOSFET and synchronous rectifier for up to 95% efficiency. While the input voltage is close to the output voltage, the converter enters low dropout mode. The duty could be as long as 100% to extend battery life.

CH3 : Step-Down DC/DC Converter

The converter operates at fixed frequency PWM mode, CCM and integrated internal compensation. While the input voltage is close to the output voltage, the converter could enter low dropout mode with low output ripple. The duty could be as long as 100% to extend the battery life.

CH4 : Step-Down DC/DC Converter

The converter operates at fixed frequency PWM mode, CCM and integrated internal compensation. While the input voltage is close to the output voltage, the converter could enter low dropout mode with low output ripple. The duty could be as long as 100% to extend the battery life.

CH5 : Step-Up DC/DC Converter

It integrates asynchronous boost with an internal MOSFET, internal compensation and an external schottky diode to provide CCD positive power supply. The converter is inactive until the SW5 soft start procedure is finished. This feature provides load disconnect function and effectively limits the inrush current at start up.

CH6 : INV DC/DC Controller

This controller integrates an internal P-MOSFET and an external schottky diode to provide CCD negative power supply. The output voltage is set as

$V_{OUT} = (R10/R11) \times (-1.25)$ (R10, R11 refer to Typical Application Circuit).

CH7 : WLED Driver

It is an asynchronous DC/DC converter with an internal MOSFET, internal compensation and an external schottky diode to drive up to 4 WLED. This channel also features PWM dimming control from EN7 pin and open diode protection. The current through WLED is set as

$$I \text{ (mA)} = [250\text{mV}/R(\Omega)] \times \text{Duty (\%)}$$

R : Current sense resistor from CFB7 to GND.

Duty : PWM dimming by EN7 pin. Dimming frequency range is from 1kHz to 100kHz but it is recommended to avoid 2kHz to 20kHz for audio noise. Hold EN7 low for more than 15ms will turn off CH7.

SW1

SW1 is an open drain controller to drive an external PMOS and then functions as a load disconnect switch for CH1. This switch features soft start, Power On/Off Sequence and under voltage protection functions. OK134 is an open drain control pin. Once CH1, CH3 and CH4's soft start are completed, SW1 is on. The OK134 pin is slowly pulled low and controlled with soft start to suppress the inrush current. VOUT1 is used for SW1 soft start and under voltage protection. If SW1 is not used, connect a resistor to VOUT1 (Refer to Typical Application Circuit for Li-ion).

SW5

SW5 is an internal switch enabled by EN5 and functions as a load disconnection for CH5. This switch features soft start, Power On Sequence, over voltage (for SW5I) and under voltage (for SW5O) protection functions.

Charge Pumps

The charge pump function is enabled while battery type is alkaline battery. This channel provides pump voltage to enhance MOS gate driving capability. This function is not necessary while battery is Li-ion type.

Reference Voltage

The RT9917 provides a precise 1.25V reference voltage with sourcing capability 100μA. Connect a 0.1μF ceramic capacitor from VREF pin to GND. Reference voltage is enabled by connecting EN6 to logic high. Furthermore, this reference voltage is internally pulled to GND in shutdown.

Mode and sequence setting

Please refer to "Electrical Characteristics" for level of logic high or low.

Table 1. Mode setting

SEL	CH2
High	Boost
Low	Buck

For CH2, Mode setting is decided by "SEL" pin. The CH2 of RT9917 features flexible boost or buck topology setting for either 1x Li-ion or 2 x AA application by one pin.

Table 2. Sequence setting

SEQ	Power ON Sequence
High	CH1 -> CH3 -> CH4 -> (SW1 and CH2)
Low	CH3 -> CH4 -> CH1 -> (SW1 and CH2)

SEQ	Power OFF Sequence
High	(SW1 and CH2) -> CH4 -> CH3 -> CH1
Low	(SW1 and CH2) -> CH1 -> CH4 -> CH3

Sequence setting is decided by "SEQ" pin. Please note that the logic state can not be changed during operation.

SEQ = High

The Power On Sequence is :

- ▶ While EN134 goes high, CH1 will be turned on to wait for the completion of CH1's soft start.
- ▶ After that, CH3 will be turned on to wait for the completion of CH3's soft start.
- ▶ And then, CH4 will be turned on to wait for the completion of CH4's soft start.
- ▶ Then, SW1 will be turned on and CH2 is allowed to be turned on by EN2 at any time.
- ▶ Finally, SW1's soft start will be completed.

The Power-Off Sequence is :

- ▶ At first, while EN134 goes low, (SW1 is shutdown and internally pulled low, CH2 must be turned off by EN2) SW1 (note 1) and CH2 (note 2) will be shutdown.
- ▶ After that, CH4 will be turned off and internally pulled low to wait for the completion of CH4's shutdown.
- ▶ And then, CH3 will be turned off and internally pulled low to wait for CH3's shutdown completion.

- ▶ Then, CH1 will be turned off and internally pulled low (note 3) to wait for CH1's shutdown completion.
- ▶ Finally, the whole IC will be shutdown (if EN5, EN6 and EN7 already go low).

Note 1 : The SW1 is designed for CH1.

Note 2 : If CH2 is configured as a Boost, then the CH2 will not be internally pulled low and the completion of shutdown will not be checked.

Note3 : CH1 is configured as a Boost, so the CH1 will not be internally pulled low and the completion of shutdown will not be checked.

SEQ = Low

The Power On Sequence is :

- ▶ While EN134 goes high, CH3 will be turned on to wait for the completion of CH3's soft start.
- ▶ After that, CH4 will be turned on to wait for the completion of CH4's soft start.
- ▶ And then, CH1 will be turned on to wait for the completion

of CH1's soft start.

- ▶ Then, SW1 will be turned on and CH2 is allowed to be turned on by EN2 at any time.
- ▶ Finally, SW1's soft start will be completed.

The Power-Off Sequence is :

- ▶ At first, while EN134 goes low, (SW1 is shutdown and internally pulled low, CH2 must be turned off by EN2) SW1 (note 1) and CH2 (note 2) will be shutdown.
- ▶ Then, CH1 will be turned off and internally pulled low (note 3) to wait for CH1's shutdown completion.
- ▶ After that, CH4 will be turned off and internally pulled low to wait for the completion of CH4's shutdown.
- ▶ And then, CH3 will be turned off and internally pulled low to wait for CH3's shutdown completion.
- ▶ Finally, the whole IC will be shutdown (if EN5, EN6 and EN7 already go low).

Protection

	Protection type	Threshold (typical) Refer to Electrical spec	Protection methods	Reset method
V _{DDM}	Over Voltage Protection	V _{DDM} > 6V	Disable all channels (except CH7)	Restart if V _{DDM} < 5.6V (with hysteresis)
CH1:Boost	Current Limit	NMOS current > 3A	NMOS off, PMOS on	Automatic reset at next clock cycle
	PVDD1 OVP	PVDD1 > 6V	IC shutdown (except CH7)	V _{DDM} power reset
CH2:Boost	Current Limit	NMOS current > 3A	NMOS off, PMOS on	Automatic reset at next clock cycle
	PVDD2 OVP	PVDD2 > 6V	IC shutdown (except CH7)	V _{DDM} power reset
CH2:Buck	OCP	PMOS current > 1.5A	IC shutdown (except CH7)	V _{DDM} power reset
CH3:Buck	OCP	PMOS current > 1.5A	IC shutdown (except CH7)	V _{DDM} power reset
CH4:Buck	OCP	PMOS current > 1.5A	IC shutdown (except CH7)	V _{DDM} power reset
CH5:	OCP	NMOS current > 1.5A	NMOS off	Automatic reset at next clock cycle
CH6:	OCP	PMOS current > 1.5A	IC shutdown (except CH7)	V _{DDM} power reset
CH7:WLED	OCP	NMOS current > 0.8A	NMOS off	Automatic reset at next clock cycle
	OVP	VOUT7 > 19V	Shutdown CH7	Reset by toggling EN7
SW1	UVP	VOUT1 < 1.75V after SW1 soft start end	IC shutdown (except CH7)	V _{DDM} power reset
SW5	OVP	SW5I > 19V	IC shutdown (except CH7)	V _{DDM} power reset
	UVP	SW5O < 0.4V after SW5 soft start end	IC shutdown (except CH7)	V _{DDM} power reset
Thermal	Thermal shutdown	Temperature > 160°C	All channels stop switching	Temperature < 140°C

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-40L 5x5 packages, the thermal resistance θ_{JA} is 36°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (36^\circ\text{C/W}) = 2.778\text{W for WQFN-40L 5x5 packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA} . For RT9917 package, the Figure 1 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

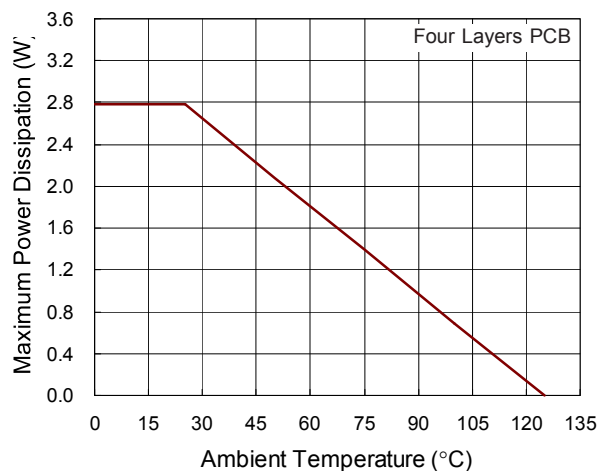


Figure 1. Derating Curves for RT9917 Packages

Layout Consideration

- ▶ All the traces of the compensation components should be short to reduce the parasitic connection resistance and isolated from other noisy device traces. The ground traces must be connected to ground plane independently.

Compensative parts: R15, C16, R18, C19, R12, C11, C14.

- ▶ All the traces of the feedback components should be short to reduce the parasitic connection resistance and isolated from other noisy device traces. The ground traces must be connected to ground plane independently. Output sense trace must be kept away from the noisy device (inductor).

Feedback parts:

R13, R14, C15 for CH1. R16, R17, C18 for CH2. R3, R4, C4 for CH3.

R5, R6, C6 for CH4. R7, R8, C9 for CH5.

R10, R11, C13 for CH6. R9 for CH7.

- ▶ All the traces of connecting inductor must be as wide as possible.

Inductor: L1, L2, L3, L4, L5, L6, L7.

- ▶ Output Capacitor should be placed close to V_{out} and connected to ground plane to reduce noise coupling.

Output capacitor: C1, C5, C7, C8, C10, C12, C17 and C24.

- ▶ Input capacitor should be placed close to V_{bat} and connected to ground plane.

Input capacitor: C2, C3, C20, C21, C26, C27 and C28.

- ▶ The GND (Pin 27) and Exposed Pad should be connected to a strong ground plane for heat sinking and noise protection.

- ▶ The EN7 pin is used for dimming control. Keep the FB3 trace away from the EN7.

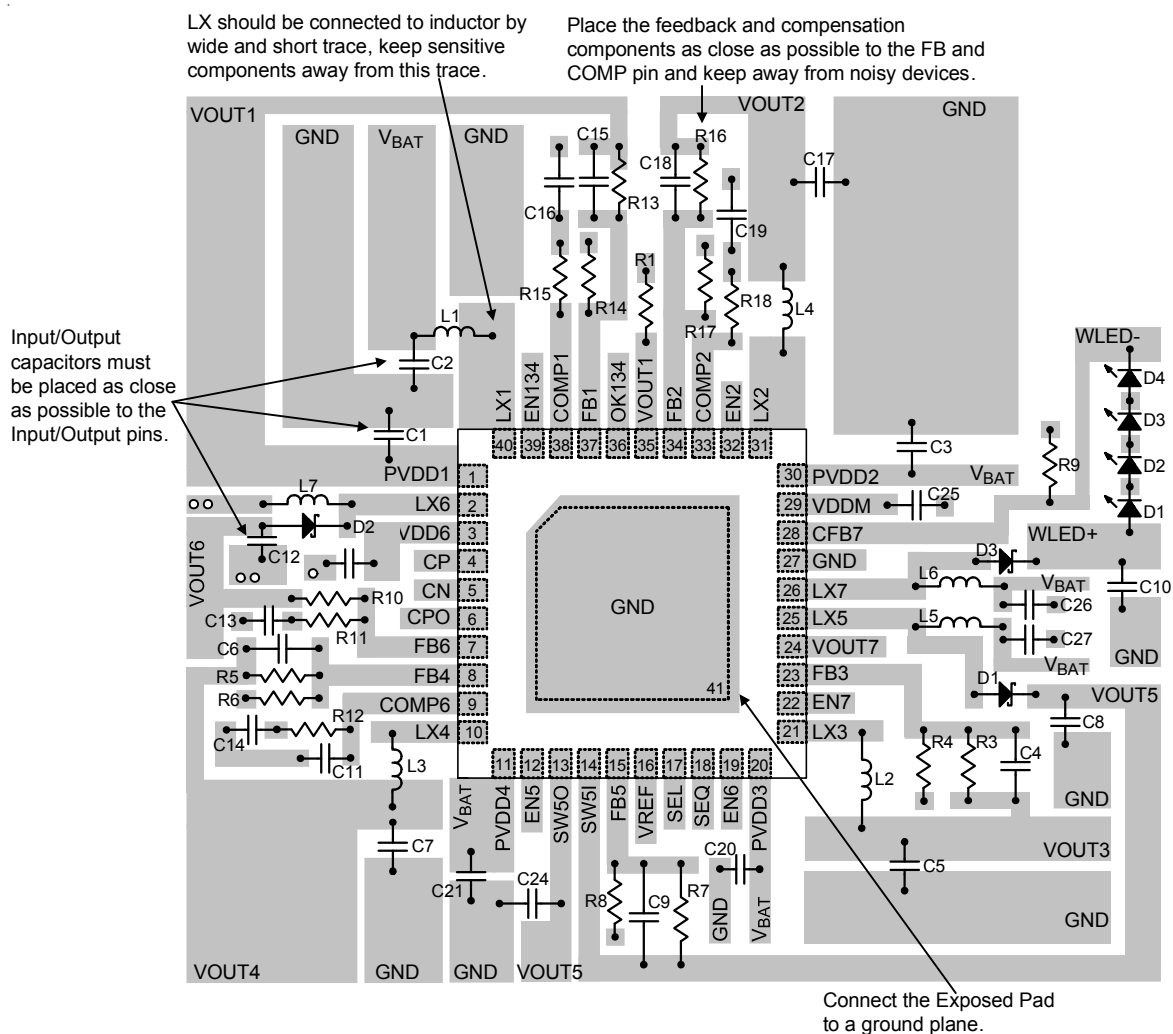
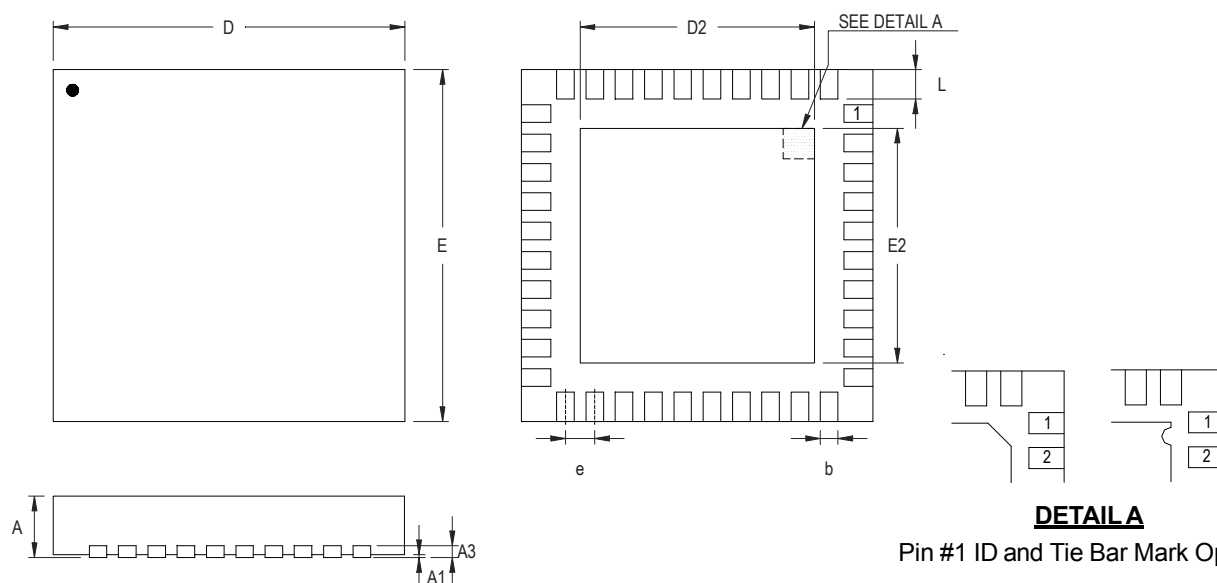


Figure 2

Outline Dimension



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	4.950	5.050	0.195	0.199
D2	3.250	3.500	0.128	0.138
E	4.950	5.050	0.195	0.199
E2	3.250	3.500	0.128	0.138
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 40L QFN 5x5 Package

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