

TPS37 Wide V_{IN} 65 V Dual Channel Overvoltage & Undervoltage (OV & UV) Detector with Programmable Sense and Reset Delay Function

1 Features

- Wide supply voltage range: 2.7 V to 65 V
- SENSE and RESET pins are 65 V graded
- Low quiescent current: 1 μ A (typical)
- Flexible and wide voltage threshold options
Table 13-1
 - 2.7 V to 36 V (1.5% maximum accuracy)
 - 800 mV option (1% maximum accuracy)
- Built-in hysteresis (V_{HYS})
 - Percentage options: 2% to 13% (1% steps)
 - Fixed options: $V_{TH} < 8\text{ V} = 0.5\text{ V}, 1\text{ V}, 1.5\text{ V}, 2\text{ V}, 2.5\text{ V}$
- Programmable reset time delay
 - 10 nF = 12.8 ms, 10 μ F = 12.8 s
- Programmable sense time delay
 - 10 nF = 1.28 ms, 10 μ F = 1.28 s
- Manual Reset ($\overline{MR}$) feature
- Output reset latching feature
- Output topology: Open-Drain or Push-Pull

2 Applications

- Analog input module
- CPU (PLC controller)
- Servo drive control module
- Servo drive power stage module
- Servo drive functional safety module
- HVAC valve and actuator control

3 Description

The TPS37 is a family of wide input range and low quiescent current window supervisors for fast detection of overvoltage (OV) and undervoltage (UV) conditions. Each device includes a precision internal reference, two independent and configurable voltage comparators and integrated resistor dividers. The TPS37 can be connected directly to and monitor 12 V / 24 V supply rails in a variety of industrial applications including factory automation, motor drives, building automation and others. Built-in hysteresis on the SENSE pins prevents false reset signals when monitoring a supply voltage rail.

The separate VDD and SENSE pins allow redundancy sought by high-reliability systems. SENSE is decoupled from VDD and can monitor higher and lower voltages than VDD. Optional use of external resistors are supported by the high impedance input of the SENSE pins. CTSx and CTRx pins allow delay adjustability on the rising and falling edges of the RESET signals. Also, CTSx functions as a debouncer by ignoring voltage glitches on the monitored voltage rails; CTRx operates as a manual reset ($\overline{MR}$) that can be used to force a system reset.

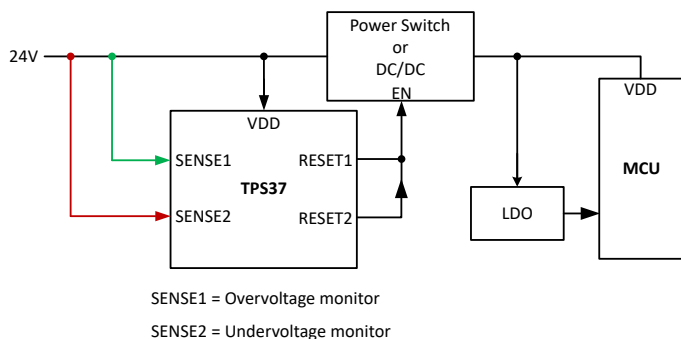
TPS37 is available in a WSON or SOT-23 package. The central pad is non-conductive to increase the creepage between VDD and GND per guidelines in IEC60664. TPS37 operates over -40°C to $+125^{\circ}\text{C}$ T_A .

Device Information

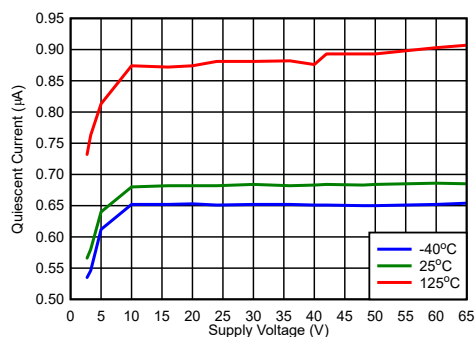
PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
TPS37	WSON (10) (DSK)	2.5 mm × 2.5 mm
TPS37	SOT-23 (14) (DYY) ⁽²⁾	4.1 mm × 1.9 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.

(2) Product Preview



Typical Application Circuit



Typical I_{DD} vs V_{DD}



Table of Contents

1 Features	1	9 Device Functional Modes	24
2 Applications	1	10 Application and Implementation	25
3 Description	1	10.1 Adjustable Voltage Thresholds.....	25
4 Revision History	2	10.2 Application Information.....	26
5 Device Comparison	3	11 Power Supply Recommendations	29
6 Pin Configuration and Functions	4	11.1 Power Dissipation and Device Operation.....	29
7 Specifications	6	12 Layout	30
7.1 Absolute Maximum Ratings.....	6	12.1 Layout Guidelines.....	30
7.2 ESD Ratings	6	12.2 Layout Example.....	30
7.3 Recommended Operating Conditions.....	6	12.3 Creepage Distance.....	31
7.4 Thermal Information	6	13 Device and Documentation Support	32
7.5 Electrical Characteristics.....	7	13.1 Device Nomenclature.....	32
7.6 Timing Requirements.....	9	13.2 Support Resources.....	33
7.7 Timing Diagrams	10	13.3 Trademarks.....	33
7.8 Typical Characteristics.....	12	13.4 Electrostatic Discharge Caution.....	33
8 Detailed Description	15	13.5 Glossary.....	33
8.1 Overview.....	15	14 Mechanical, Packaging, and Orderable Information	33
8.2 Functional Block Diagram.....	15		
8.3 Feature Description.....	16		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2021) to Revision D (December 2021)	Page
• Advanced Information to Production Data release.....	1

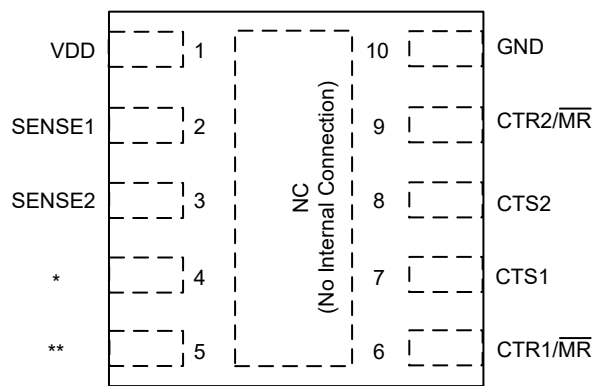
5 Device Comparison

Contact TI sales representatives or consult TI's E2E forum for details and availability; minimum order quantities may apply.

		Voltage Threshold		Hysteresis			
		CH 1	CH 2	CH 1	CH 2	XXX	R
TPS37 X		XX	XX	X	X	XXX	R
Topology		Threshold Voltage				Hysteresis	
Suffix	CH1	CH2					
A	OV OD L	UV OD L					
B	OV PP H	UV OD L					
C	OV OD L	UV OD H					
D	OV PP H	UV OD H					
E	OV OD H	UV OD H					
F	OV OD H	UV OD L					
G	OV PP L	UV OD H					
H	OV PP L	UV OD L					
		Threshold Voltage					
		100mV steps		400mV steps		500mV steps	
Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT
01	800mV	70	7.0V	A0	10.4V	D0	20.5V
27	2.7V	71	7.1V	A1	10.8V	D1	21.0V
28	2.8V	72	7.2V	A2	11.2V	D2	21.5V
29	2.9V	73	7.3V	A3	11.6V	D3	22.0V
30	3.0V	74	7.4V	A4	12.0V	D4	22.5V
31	3.1V	75	7.5V	A5	12.4V	D5	23.0V
32	3.2V	76	7.6V	A6	12.8V	D6	23.5V
33	3.3V	77	7.7V	A7	13.2V	D7	24.0V
34	3.4V	78	7.8V	A8	13.6V	D8	24.5V
35	3.5V	79	7.9V	A9	14.0V	D9	25.0V
36	3.6V	80	8.0V	B0	14.4V	E0	25.5V
37	3.7V	81	8.1V	B1	14.8V	E1	26.0V
38	3.8V	82	8.2V	B2	15.2V	E2	26.5V
39	3.9V	83	8.3V	B3	15.6V	E3	27.0V
40	4.0V	84	8.4V	B4	16.0V	E4	27.5V
41	4.1V	85	8.5V	B5	16.4V	E5	28.0V
42	4.2V	86	8.6V	B6	16.8V	E6	28.5V
43	4.3V	87	8.7V	B7	17.2V	E7	29.0V
44	4.4V	88	8.8V	B8	17.6V	E8	29.5V
45	4.5V	89	8.9V	B9	18.0V	E9	30.0V
46	4.6V	90	9.0V	C0	18.4V		
47	4.7V	91	9.1V	C1	18.8V		
48	4.8V	92	9.2V	C2	19.2V		
49	4.9V	93	9.3V	C3	19.6V		
50	5.0V	94	9.4V	C4	20.0V		
51	5.1V	95	9.5V				
52	5.2V	96	9.6V				
53	5.3V	97	9.7V				
54	5.4V	98	9.8V				
55	5.5V	99	9.9V				
56	5.6V	00	10.0V				
57	5.7V						
58	5.8V						
59	5.9V						
60	6.0V						
61	6.1V						
62	6.2V						
63	6.3V						
64	6.4V						
65	6.5V						
66	6.6V						
67	6.7V						
68	6.8V						
69	6.9V						
Suffix	CH1						
2	2%						
3	3%						
4	4%						
5	5%						
6	6%						
7	7%						
8	8%						
9	9%						
A	10%						
B	11%						
C	12%						
D	13%						
E	0.5V						
F	1V						
G	1.5V						
H	2V						
I	2.5V						
Suffix	Name						
DSK	WS0N						
DYY	SOT-23						
Suffix	Name						
R	Large						

1. Sense logic: OV = overvoltage; UV = undervoltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.7 V to 8 V threshold options
5. **Product Preview (DYY) package**

6 Pin Configuration and Functions



* Pin 4 Options

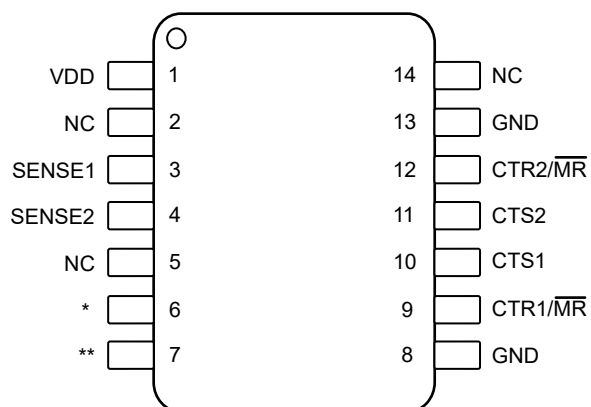
1. $\overline{\text{RESET1_OV}}\#\#$
2. $\text{RESET1_OV}\#\#$

** Pin 5 Options

1. $\overline{\text{RESET2_UVOD}}$
2. RESET2_UVOD

OD (Open-Drain) or PP (Push-Pull)

**Figure 6-1. DSK Package,
10-Pin WSON,
TPS37 (Top View)**



* Pin 6 Options

1. $\overline{\text{RESET1_OV}}\#\#$
2. $\text{RESET1_OV}\#\#$

** Pin 7 Options

1. $\overline{\text{RESET2_UVOD}}$
2. RESET2_UVOD

OD (Open-Drain) or PP (Push-Pull)

**Figure 6-2. DYY Package,
14-Pin SOT-23,
TPS37 (Top View)
PRODUCT PREVIEW**

Table 6-1. Pin Functions

PIN NAME	WSN (DSK)	SOT23 (DYY)	I/O	DESCRIPTION
	PIN NUM.	PIN NUM.		
VDD	1	1	I	Input Supply Voltage: Bypass with a 0.1 μ F capacitor to GND.
SENSE1	2	3	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on SENSE1 pin transitions above the upper threshold voltage of V_{IT+} , $\overline{\text{RESET1}}$ /RESET1 asserts after the sense time delay, set by CTS1. When the voltage on the SENSE1 pin transitions below the upper threshold voltage of $V_{IT+} - V_{HYS}$, $\overline{\text{RESET1}}$ /RESET1 deasserts after the reset time delay, set by CTR1. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
SENSE2	3	4	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on SENSE2 pin transitions below the lower threshold voltage of V_{IT-} , $\overline{\text{RESET2}}$ /RESET2 asserts after the sense time delay, set by CTS2. When the voltage on the SENSE2 pin transitions above the lower threshold voltage of $V_{IT-} + V_{HYS}$, $\overline{\text{RESET2}}$ /RESET2 deasserts after the reset time delay, set by CTR2. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance.
$\overline{\text{RESET1}}$ /RESET1	4	6	O	Output Reset Signal For Channel 1: See Section 5 for output topology options. $\overline{\text{RESET1}}$ /RESET1 asserts when SENSE1 rises outside of the upper voltage threshold. $\overline{\text{RESET1}}$ /RESET1 remains asserted for the reset time delay period after SENSE1 transitions out of an overvoltage (OV) fault condition. For active low open-drain reset output, an external pullup resistor is required. Do not place external pullup resistors on push-pull outputs. Reset output signal for: SENSE1 Sensing Topology: Overvoltage (OV) Output topology: Open Drain or Push Pull, Active Low or Active High
$\overline{\text{RESET2}}$ /RESET2	5	7	O	Output Reset Signal For Channel 2: See Section 5 for output topology options. $\overline{\text{RESET2}}$ /RESET2 asserts when SENSE2 falls outside of the lower voltage threshold. $\overline{\text{RESET2}}$ /RESET2 remains asserted for the reset time delay period after SENSE2 transitions out of an undervoltage (UV) fault condition. For active low open-drain reset output, an external pullup resistor is required. Reset output signal for: SENSE2 Sensing Topology: Undervoltage (UV) Output topology: Open Drain, Active Low or Active High
CTR1/ $\overline{\text{MR}}$	6	9	-	Channel 1 RESET Time Delay: User-programmable reset time delay for $\overline{\text{RESET1}}$ /RESET1. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. Manual Reset: If this pin is driven low, the $\overline{\text{RESET1}}$ /RESET1 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high.
CTR2/ $\overline{\text{MR}}$	9	12	-	Channel 2 RESET Time Delay: User-programmable reset time delay for $\overline{\text{RESET2}}$ /RESET2. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. Manual Reset: If this pin is driven low, the $\overline{\text{RESET2}}$ /RESET2 output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high.
GND	10	8, 13	-	Ground. All GND pins must be electrically connected to the board ground.
NC	PAD	2, 5, 14	-	The PAD for the DSK package is not internally connected, the PAD can be connected to GND or be left floating. For the DYY package, NC stands for "No Connect". The pins are to be left floating.
CTS1	7	10	O	Channel 1 SENSE Time Delay: Capacitor programmable sense delay: CTS1 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET1}}$ /RESET1 delay time to assert.
CTS2	8	11	O	Channel 2 SENSE Time Delay: Capacitor programmable sense delay: CTS2 pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET2}}$ /RESET2 delay time to assert.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted ⁽¹⁾

		MIN	MAX	UNIT
Voltage	VDD, V _{SENSE1} , V _{SENSE2} , V _{RESET1} , V _{RESET2} , V _{RESET1} , V _{RESET2}	−0.3	70	V
Voltage	V _{CTS1} , V _{CTS2} , V _{CTR1} , V _{CTR2}	−0.3	6	V
Current	I _{RESET1} , I _{RESET2} , I _{RESET1} , I _{RESET2}		10	mA
Temperature ⁽²⁾	Operating junction temperature, T _J	−40	150	°C
Temperature ⁽²⁾	Operating Ambient temperature, T _A	−40	150	°C
Temperature ⁽²⁾	Storage, T _{stg}	−65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that T_J = T_A.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	± 750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V _{DD}	2.7		65	V
Voltage	V _{SENSE1} , V _{SENSE2} , V _{RESET1} , V _{RESET2} , V _{RESET1} , V _{RESET2}	0		65	V
Voltage	V _{CTS1} , V _{CTS2} , V _{CTR1} , V _{CTR2}	0		5.5	V
Current	I _{RESET1} , I _{RESET2} , I _{RESET1} , I _{RESET2}	0		±5	mA
T _J	Junction temperature (free air temperature)	−40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS37	UNIT
		DSK	
		10-PIN	
R _{θJA}	Junction-to-ambient thermal resistance	87.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	76.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	54.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	4.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	54.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	34.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V _{DD}	Supply Voltage		2.7		65	V
UVLO ⁽¹⁾	Under Voltage Lockout	V _{DD} Falling below V _{DD} (MIN)			2.7	V
V _{POR}	Power on Reset Voltage ⁽²⁾ RESET, Active Low (Open-Drain, Push-Pull)	V _{OL} (MAX) = 300 mV I _{OUT} (Sink) = 15 μA			1.4	V
V _{POR}	Power on Reset Voltage ⁽²⁾ RESET, Active High (Push-Pull)	V _{OH} (MIN) = 0.8 x V _{DD} I _{OUT} (Source) = 15 μA			1.4	V
I _{DD}	Supply current into VDD pin	V _{IT} = 800 mV V _{DD} (MIN) ≤ V _{DD} ≤ V _{DD} (MAX)		1	2.6	μA
		V _{IT} = 2.7 V to 36 V V _{DD} (MIN) ≤ V _{DD} ≤ V _{DD} (MAX)		1	2	μA
SENSE (Input)						
I _{SENSE}	Input current (SENSE1, SENSE2)	V _{IT} = 800 mV			100	nA
I _{SENSE}	Input current (SENSE1, SENSE2)	V _{IT} < 10 V			0.8	μA
I _{SENSE}	Input current (SENSE1, SENSE2)	10 V < V _{IT} < 26 V			1.2	μA
I _{SENSE}	Input current (SENSE1, SENSE2)	V _{IT} > 26 V			2	μA
V _{ITN}	Input Threshold Negative (Undervoltage)	V _{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V _{IT} = 800 mV ⁽³⁾	0.792	0.800	0.808	V
V _{ITP}	Input Threshold Positive (Overvoltage)	V _{IT} = 2.7 V to 36 V	-1.5		1.5	%
		V _{IT} = 800 mV ⁽³⁾	0.792	0.800	0.808	V
V _{HYS}	Hysteresis Accuracy ⁽⁴⁾	V _{IT} = 0.8 V and 2.7 V to 36 V V _{HYS} Range = 2% to 13% (1% step)	-1.5		1.5	%
		V _{IT} = 2.7 V to 8 V V _{HYS} = 0.5 V, 1 V, 1.5 V, 2 V, 2.5 V V _{IT} -V _{HYS} ≥ 2.4 V	-1.5		1.5	%
RESET (Output)						
I _{lkg} (OD)	Open-Drain leakage (RESET1, RESET2)	V _{RESET} = 5.5 V V _{ITN} < V _{SENSE} < V _{ITP}			300	nA
		V _{RESET} = 65 V V _{ITN} < V _{SENSE} < V _{ITP}			300	nA
V _{OL} ⁽⁵⁾	Low level output voltage	2.7 V ≤ VDD ≤ 65 V I _{RESET} = 5 mA			300	mV
V _{OH_DO}	High level output voltage dropout (V _{DD} - V _{OH} = V _{OH_DO}) (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I _{RESET} = 500 uA			100	mV
V _{OH} ⁽⁵⁾	High level output voltage (Push-Pull only)	2.7 V ≤ VDD ≤ 65 V I _{RESET} = 5 mA	0.8V _{DD}			V

7.5 Electrical Characteristics (continued)

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5 \text{ V}$, and load $C_{LOAD} = 10 \text{ pF}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16 \text{ V}$ and $V_{IT} = 6.5 \text{ V}$ (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance ($CTR1 / \overline{MR}$, $CTR2 / \overline{MR}$)		877	1000	1147	Kohms
R_{CTS}	Internal resistance ($CTS1$, $CTS2$)		88	100	122	Kohms
Manual Reset ($\overline{MR}$)						
$V_{\overline{MR_IH}}$	$CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic high input	$V_{DD} = 2.7 \text{ V}$	2200			mV
$V_{\overline{MR_IH}}$	$CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic high input	$V_{DD} = 65 \text{ V}$	2500			mV
$V_{\overline{MR_IL}}$	$CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic low input	$V_{DD} = 2.7 \text{ V}$			1300	mV
$V_{\overline{MR_IL}}$	$CTR1 / \overline{MR}$ and $CTR2 / \overline{MR}$ pin logic low input	$V_{DD} = 65 \text{ V}$			1300	mV

- (1) When V_{DD} voltage falls below UVLO, reset is asserted for Output 1 and Output 2. V_{DD} slew rate $\leq 100 \text{ mV} / \mu\text{s}$
- (2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR} , the output cannot be determined. $V_{DD} \text{ dv/dt} \leq 100 \text{ mV}/\mu\text{s}$
- (3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
- (4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
- (5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

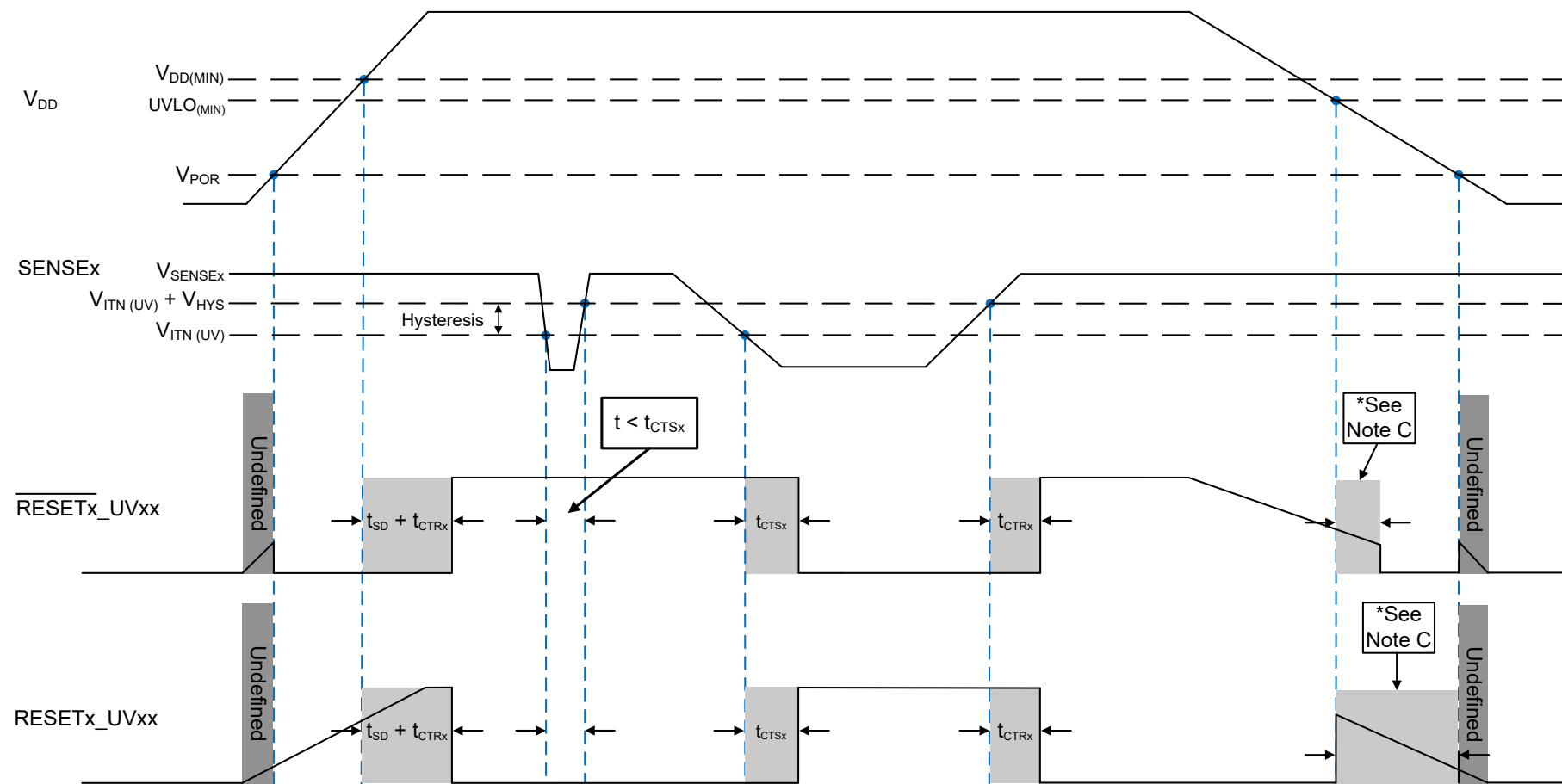
7.6 Timing Requirements

At $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$, $CTR1/\overline{MR} = CTR2/\overline{MR} = CTS1 = CTS2 = \text{open}$ ⁽¹⁾, output reset pull-up resistor $R_{PU} = 10 \text{ k}\Omega$, voltage $V_{PU} = 5.5\text{V}$, and $C_{LOAD} = 10 \text{ pF}$. VDD and SENSE slew rate = $1\text{V} / \mu\text{s}$. The operating free-air temperature range $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = 25^\circ\text{C}$ and $V_{DD} = 16\text{V}$ and $V_{IT} = 6.5\text{V}$ (V_{IT} refers to either V_{ITN} or V_{ITP}).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters					
t_{CTR}	Reset release time delay ($CTR1/\overline{MR}$, $CTR2/\overline{MR}$) ⁽²⁾	$V_{IT} = 2.7\text{V}$ to 36V $C_{CTR1} = C_{CTR2} = \text{Open}$ 20% Overdrive from Hysteresis		100	μs
		$V_{IT} = 800\text{mV}$ $C_{CTR1} = C_{CTR2} = \text{Open}$ 20% Overdrive from Hysteresis		40	μs
t_{CTS}	Sense detect time delay ($CTS1$, $CTS2$) ⁽³⁾	$V_{IT} = 2.7\text{V}$ to 36V $C_{CTS1} = C_{CTS2} = \text{Open}$ 20% Overdrive from V_{IT}		34	90 μs
		$V_{IT} = 800\text{mV}$ $C_{CTS1} = C_{CTS2} = \text{Open}$ 20% Overdrive from V_{IT}		8	17 μs
t_{SD}	Startup Delay ⁽⁴⁾	$C_{CTR1}/\overline{MR} = C_{CTR2}/\overline{MR} = \text{Open}$		2	ms

- (1) C_{CTR1} = Reset delay channel 1, C_{CTR2} = Reset delay channel 2,
 C_{CTS1} = Sense delay channel 1, C_{CTS2} = Sense delay channel 2
- (2) **CTR Reset detect time delay:**
 Overvoltage active-LOW output is measure from $V_{ITP} - HYS$ to V_{OH}
 Undervoltage active-LOW output is measure from $V_{ITN} + HYS$ to V_{OH}
 Overvoltage active-HIGH output is measure from $V_{ITP} - HYS$ to V_{OL}
 Undervoltage active-HIGH output is measure from $V_{ITN} + HYS$ to V_{OL}
- (3) **CTS Sense detect time delay:**
 Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
 Active-high output is measured from V_{IT} to V_{OH}
 V_{IT} refers to either V_{ITN} or V_{ITP}
- (4) During the power-on sequence, VDD must be at or above $V_{DD(MIN)}$ for at least t_{SD} before the output is in the correct state based on V_{SENSE} .
 t_{SD} time includes the propagation delay ($C_{CTR1} = C_{CTR2} = \text{Open}$). Capacitor in C_{CTR1} or C_{CTR2} will add time to t_{SD} .

7.7 Timing Diagrams



- A. For open-drain output option, the timing diagram assumes the $\overline{\text{RESETx_UVOD}}$ / RESETx_UVOD pin is connected via an external pull-up resistor to VDD.
- B. Be advised that this diagram shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t_{CTRx}) time.
- C. $\overline{\text{RESETx_UVxx}}$ / RESETx_UVxx is asserted when VDD goes below the UVLO_(MIN) threshold after the time delay, t_{CTRx} , is reached.

Figure 7-1. SENSEx Undervoltage (UV) Timing Diagram

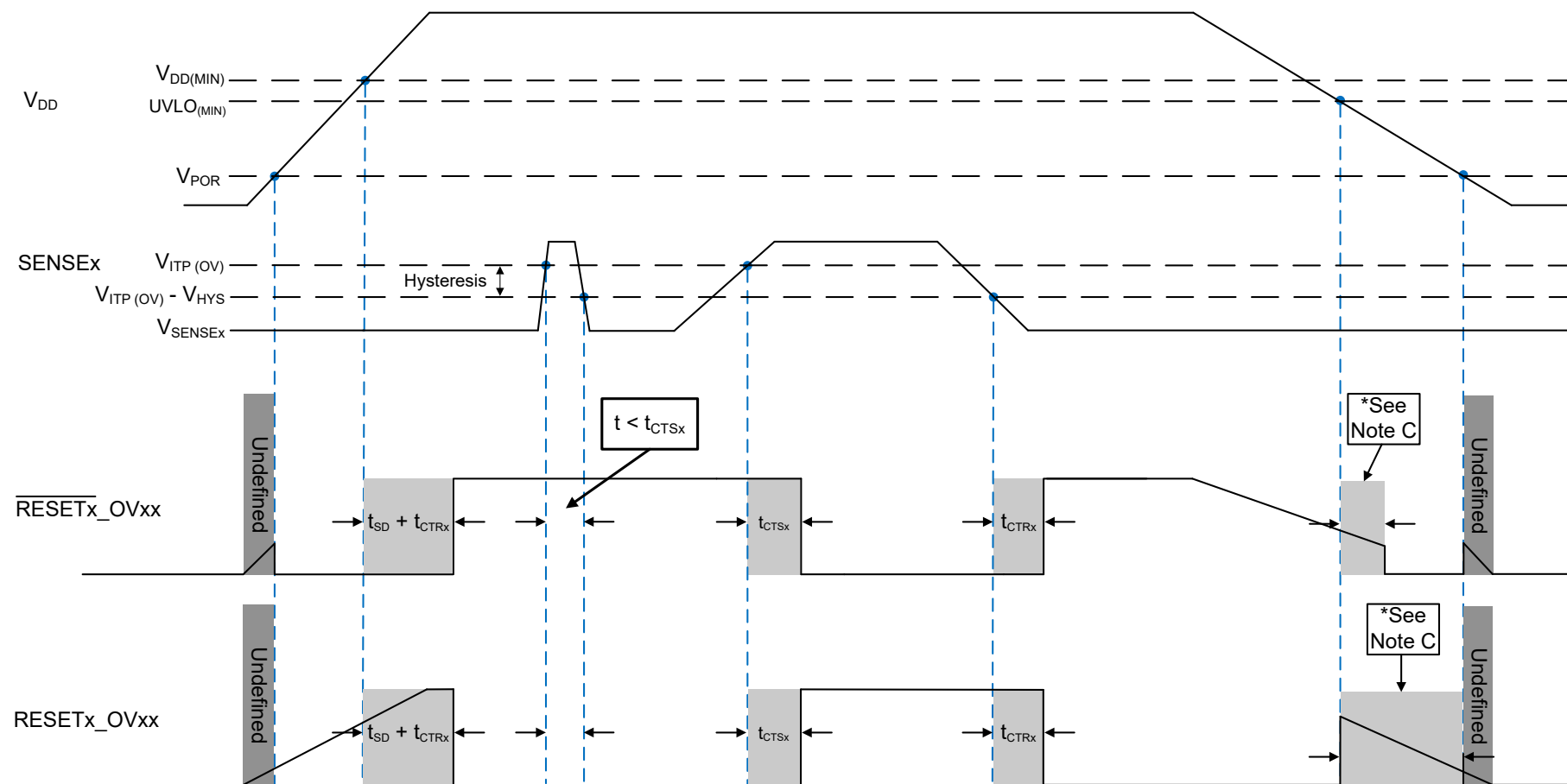
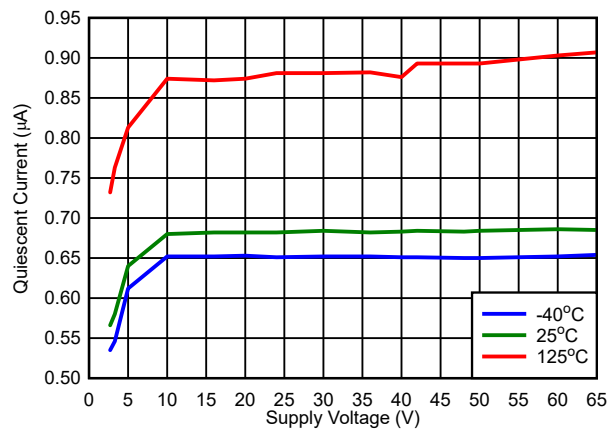


Figure 7-2. SENSEx Overvoltage (OV) Timing Diagram

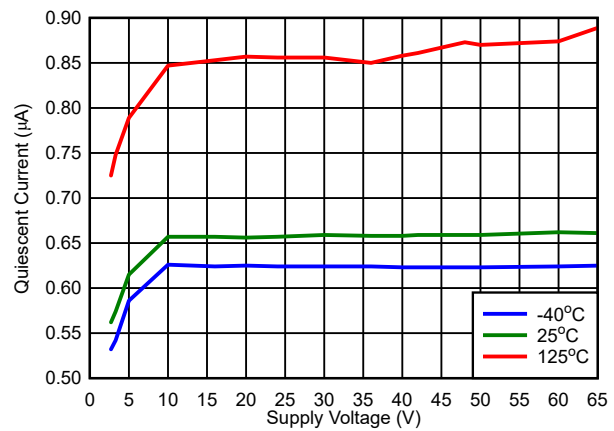
7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS37 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.



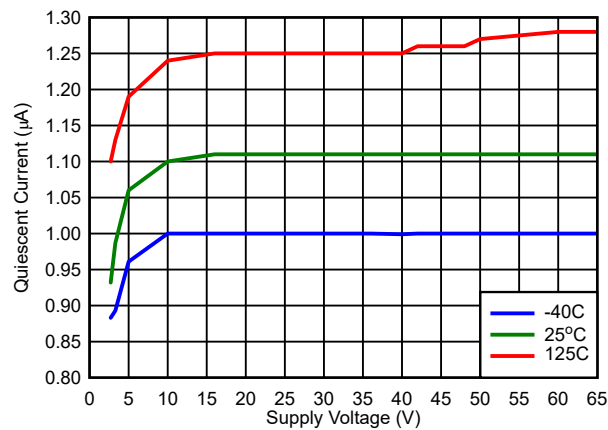
$\overline{\text{RESET}} = \text{High}, V_{IT} = 2.7\text{ V}$

Figure 7-3. V_{DD} vs I_{DD} ($\overline{\text{RESET}} = \text{High}, V_{IT} = 2.7\text{ V}$)



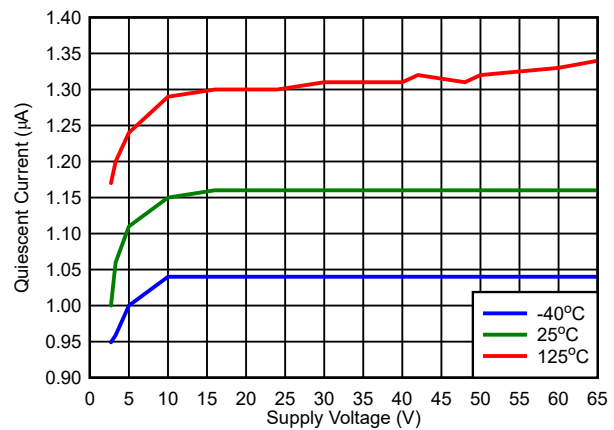
$\overline{\text{RESET}} = \text{Low}, V_{IT} = 2.7\text{ V}$

Figure 7-4. V_{DD} vs I_{DD} ($\overline{\text{RESET}} = \text{Low}, V_{IT} = 2.7\text{ V}$)



$\overline{\text{RESET}} = \text{High}, V_{IT} = 0.8\text{ V}$

Figure 7-5. V_{DD} vs I_{DD} ($\overline{\text{RESET}} = \text{High}, V_{IT} = 0.8\text{ V}$)



$\overline{\text{RESET}} = \text{Low}, V_{IT} = 0.8\text{ V}$

Figure 7-6. V_{DD} vs I_{DD} ($\overline{\text{RESET}} = \text{Low}, V_{IT} = 0.8\text{ V}$)

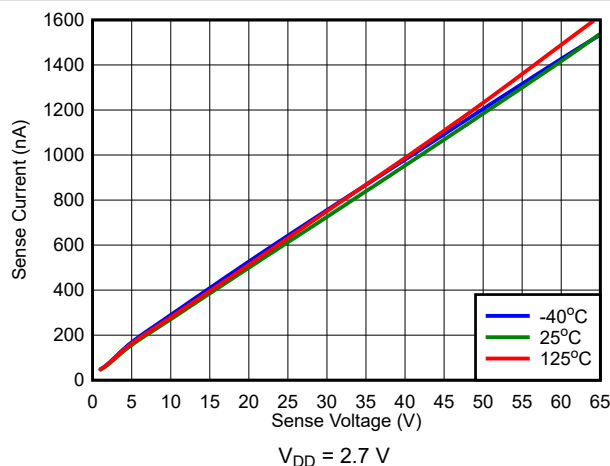


Figure 7-7. V_{SENSE} vs I_{SENSE}

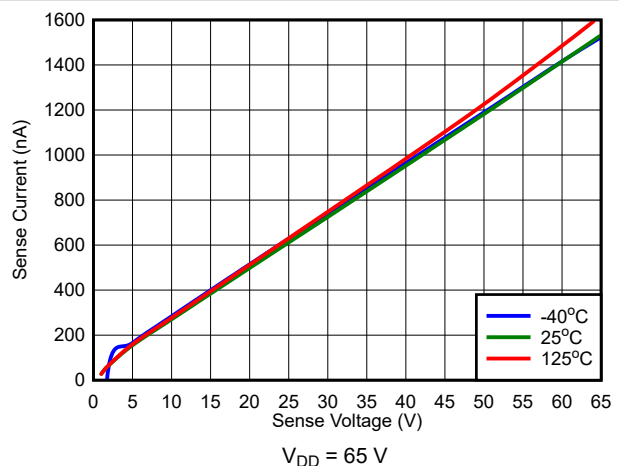


Figure 7-8. V_{SENSE} vs I_{SENSE}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS37 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

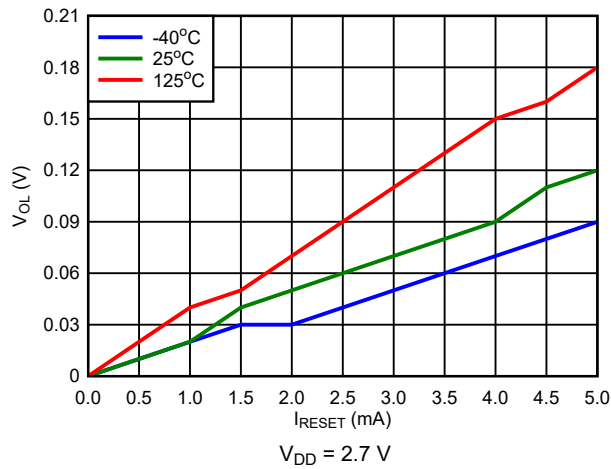


Figure 7-9. Open-Drain Active Low V_{OL} vs I_{RESET}

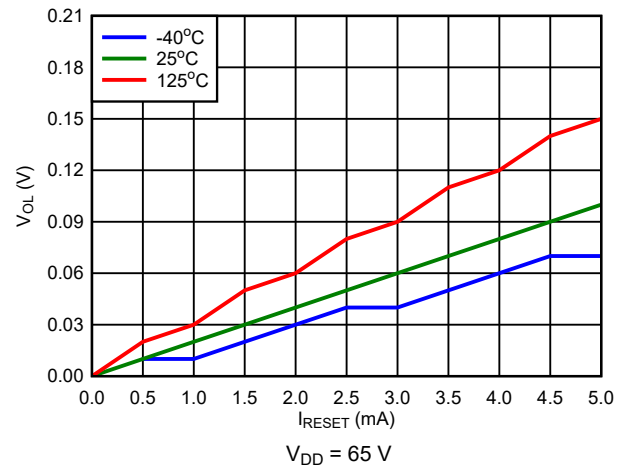


Figure 7-10. Open-Drain Active Low V_{OL} vs I_{RESET}

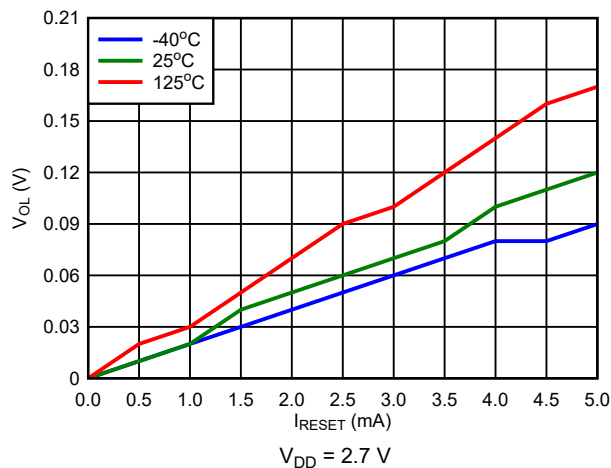


Figure 7-11. Open-Drain Active High V_{OL} vs I_{RESET}

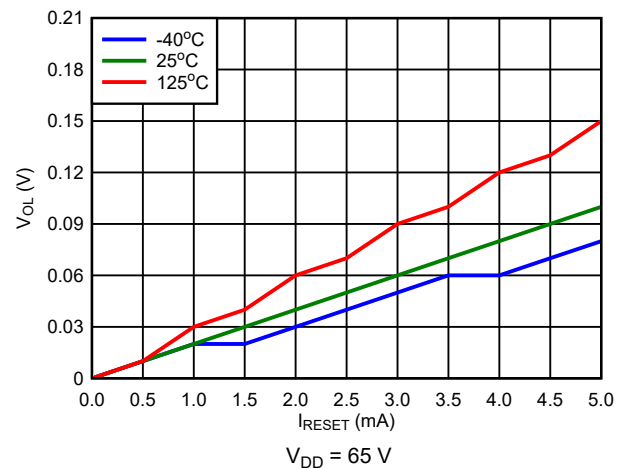


Figure 7-12. Open-Drain Active High V_{OL} vs I_{RESET}

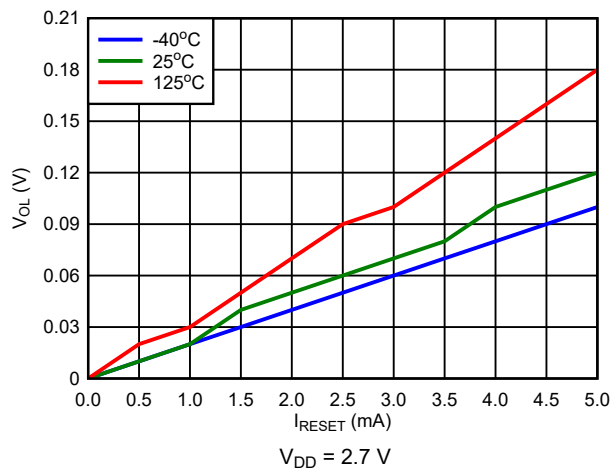


Figure 7-13. Push-Pull Active High V_{OL} vs I_{RESET}

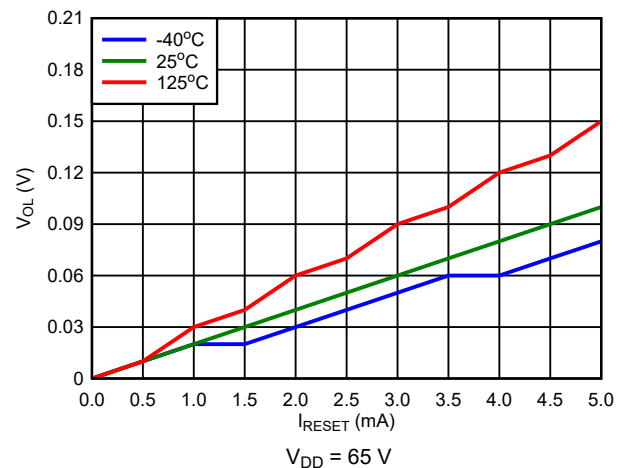


Figure 7-14. Push-Pull Active High V_{OL} vs I_{RESET}

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS37 device. Test conditions are $T_A = 25^\circ\text{C}$, $R_{PU} = 100\text{ k}\Omega$, $C_{Load} = 50\text{ pF}$, unless otherwise noted.

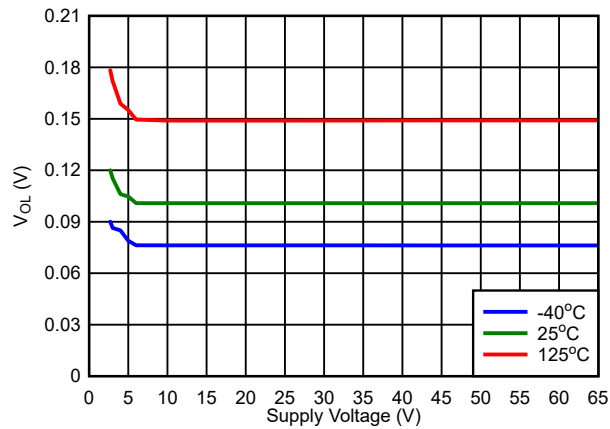


Figure 7-15. Open-Drain Active Low V_{OL} vs V_{DD}

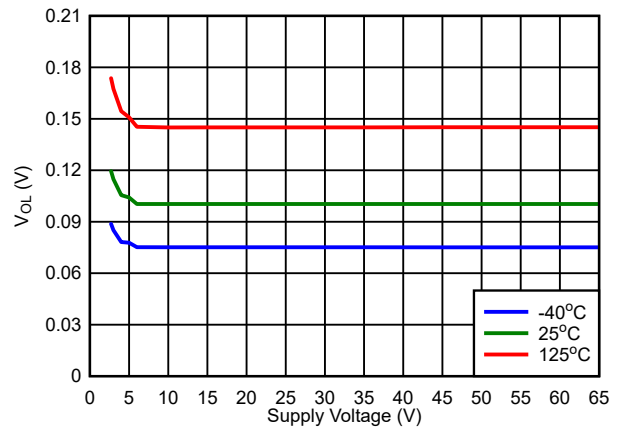


Figure 7-16. Open-Drain Active High V_{OL} vs V_{DD}

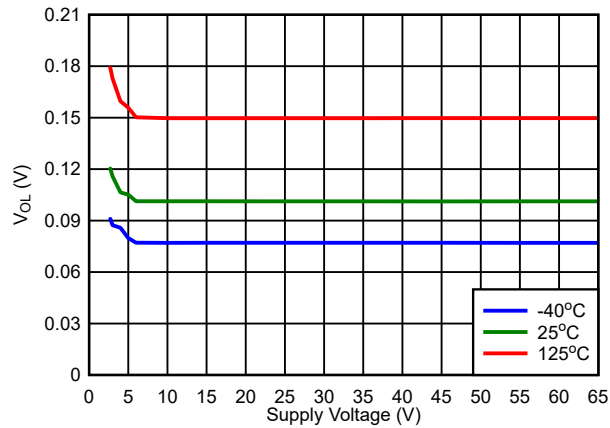


Figure 7-17. Push-Pull Active Low V_{OL} vs V_{DD}

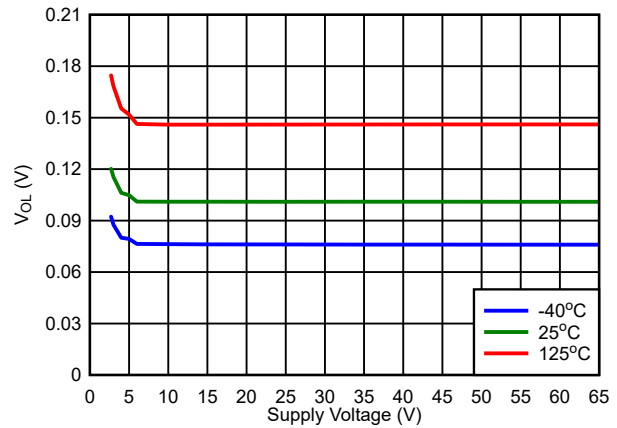


Figure 7-18. Push-Pull Active High V_{OL} vs V_{DD}

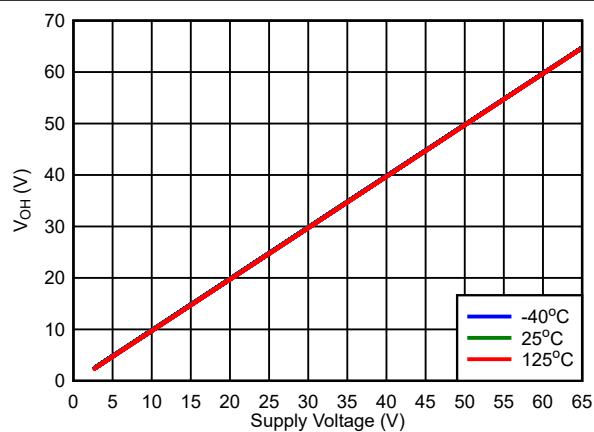


Figure 7-19. Push-Pull Active Low V_{OH} vs V_{DD}

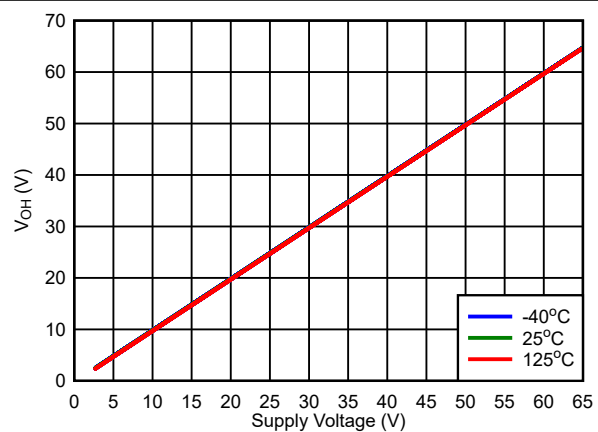


Figure 7-20. Push-Pull Active High V_{OH} vs V_{DD}

8 Detailed Description

8.1 Overview

The TPS37 is a family of high voltage and low quiescent current reset IC with fixed threshold voltage. Voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support external resistor if required by application, the lowest threshold 800 mV (bypass internal resistor ladder) is recommended for external resistors use case to take advantage of faster detection time and lower I_{SENSE} current.

VDD, SENSE and RESET pins can support 65 V continuous operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage. One thing of note, the TPS37 does not have clamps within the device so external circuits or devices must be added to limit the voltages to the absolute max limit.

Additional features include programmable sense time delay (CTS1, CTS2) and reset delay time and manual reset (CTR1 / $\overline{MR}$, CTR2 / $\overline{MR}$).

8.2 Functional Block Diagram

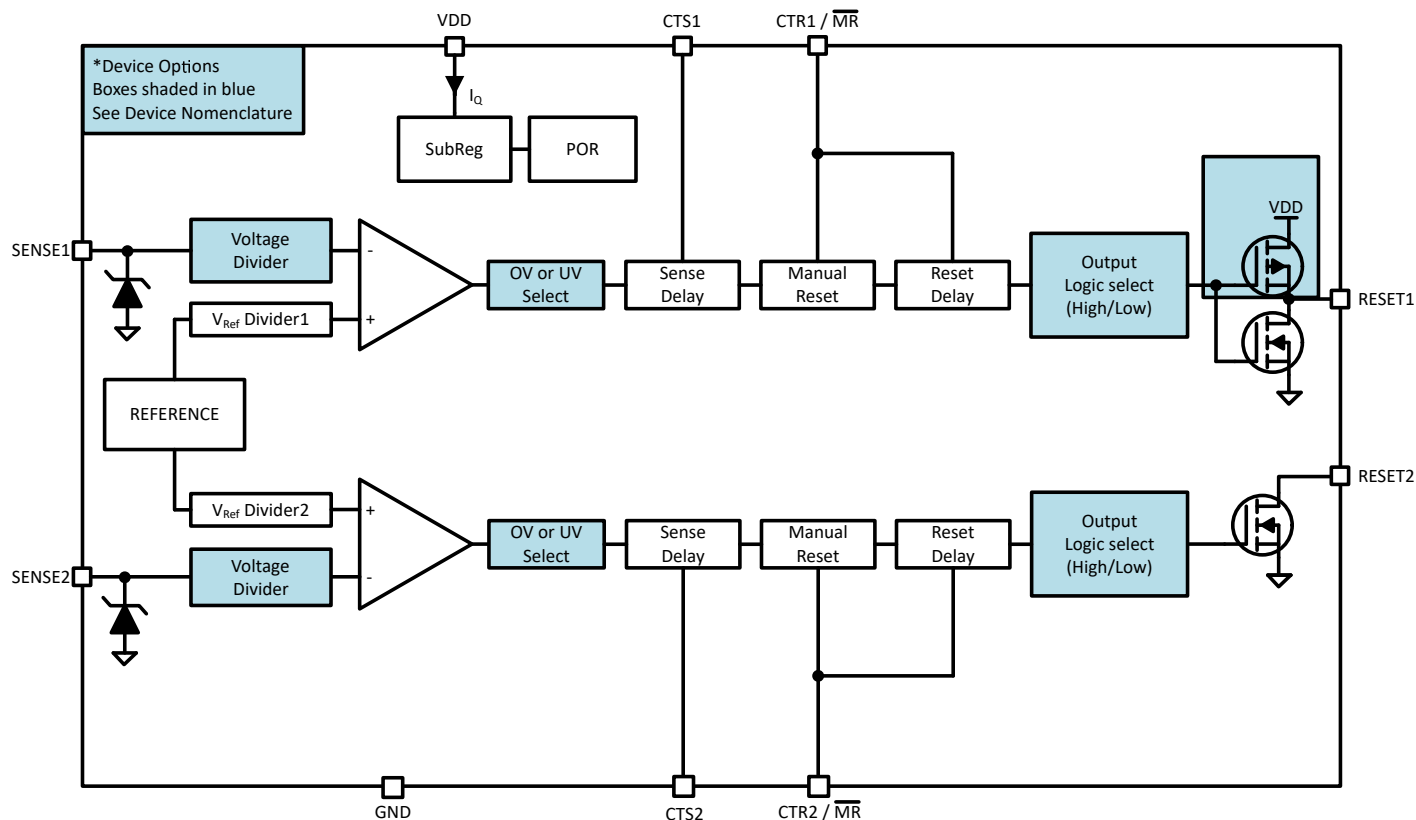


Figure 8-1. Functional Block Diagram ¹

¹ Refer to [Section 5](#) for complete list of topologies and output logic combination

8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 μ F capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET} , meaning that VDD can be higher or lower than the other pins.

8.3.1.1 Undervoltage Lockout ($V_{POR} < V_{DD} < UVLO$)

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the output pins will be in reset, regardless of the voltage at SENSE pins.

8.3.1.2 Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

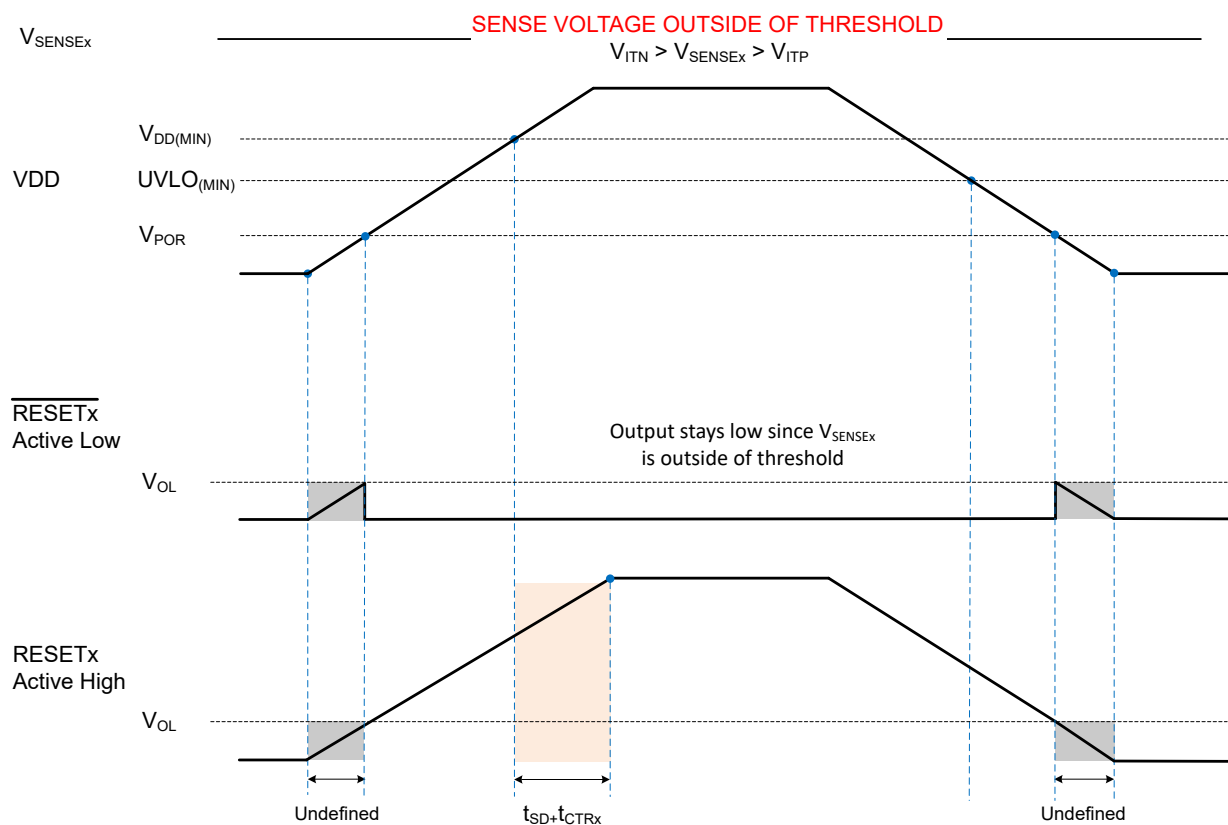


Figure 8-2. Power Cycle (SENSE Outside of Nominal voltage) ²

² Figure assumes an external pull-up resistor is connected to the reset pin via VDD

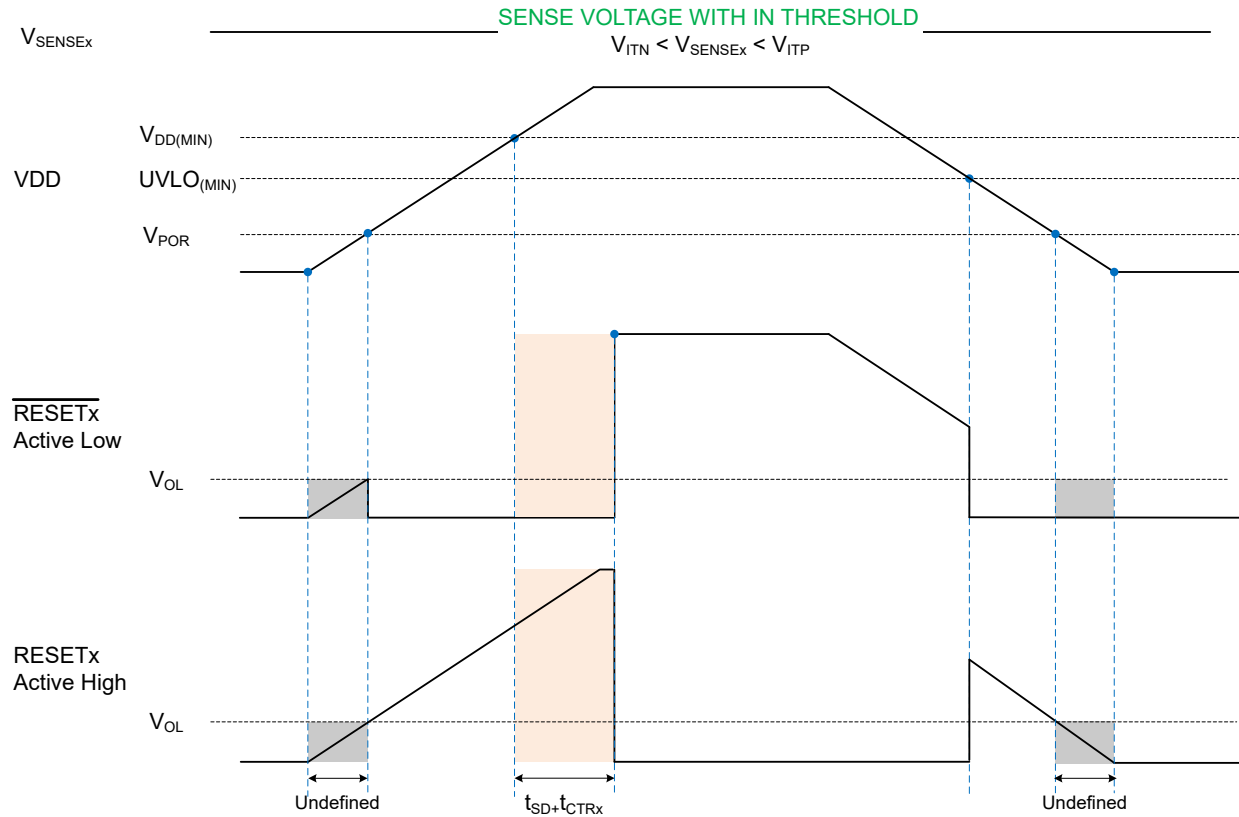


Figure 8-3. Power Cycle (SENSE Within Nominal voltage) ³

³ Figure assumes an external pull-up resistor is connected to the reset pin via VDD

8.3.2 SENSE

The TPS37 high voltage family integrates two voltage comparators, a precision reference voltage and trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Channels are independent of each other, meaning that SENSE1 and SENSE2 and respective outputs can be connected to different voltage rails.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE_x inputs in order to reduce sensitivity to transient voltages on the monitored signal. SENSE1 and SENSE2 pins can be connected directly to VDD pin.

8.3.2.1 SENSE Hysteresis

Built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

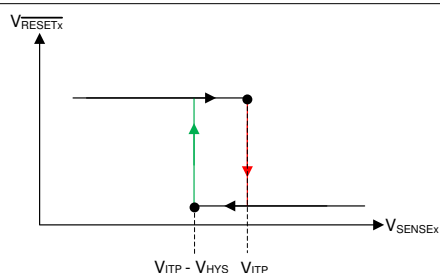


Figure 8-4. Hysteresis (Overvoltage Active-Low)

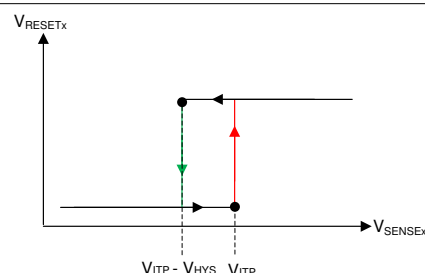


Figure 8-5. Hysteresis (Overvoltage Active-High)

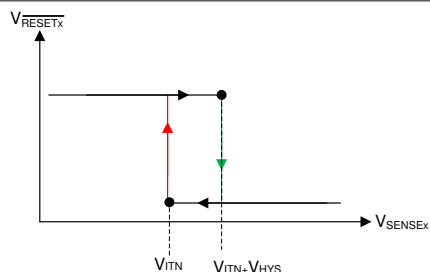


Figure 8-6. Hysteresis (Undervoltage Active-High)

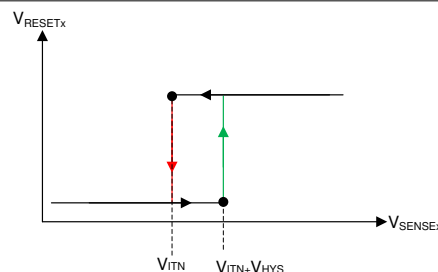


Figure 8-7. Hysteresis (Undervoltage Active-Low)

Table 8-1. Common Hysteresis Lookup Table

TARGET			DEVICE ACTUAL HYSTERESIS OPTION
DETECT THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
18.0 V	Overvoltage	17.5 V	-3%
18.0 V	Overvoltage	16.0 V	-11%
17.0 V	Overvoltage	16.5 V	-3%
16.0 V	Overvoltage	15.0 V	-6%
15.0 V	Overvoltage	14.0 V	-7%
6.0 V	Undervoltage	6.5 V	0.5 V
5.5 V	Undervoltage	6 V	0.5 V
8 V	Undervoltage	9 V	1 V
5 V	Undervoltage	7.5 V	2.5 V

Table 8-1 shows a sample of hysteresis and voltage options for the TPS37. For threshold voltages ranging from 2.7 V to 8 V, one option is to select a fixed hysteresis value ranging from 0.5 V to 2.5 V in increments of 0.5 V. Additionally, a second option can be selected where the hysteresis value is a percentage of the threshold voltage. The percentage of voltage hysteresis ranges from 2% to 13%.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is $(V_{ITN(UV)} + V_{HYS})$ and for the overvoltage (OV) channel is $(V_{ITP(OV)} - V_{HYS})$. For a visual understanding of the UV and OV release voltage, see SENSEx Undervoltage (UV) Timing Diagram and SENSEx Overvoltage (OV) Timing Diagram. The accuracy of the release voltage, or stated in the Section 7.5 as *Hysteresis Accuracy* is $\pm 1.5\%$. Expanding what is shown in Table 8-1, below are a few voltage hysteresis examples that include the hysteresis accuracy:

Undervoltage (UV) Channel

$$V_{ITN} = 0.8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 5\% = 40 \text{ mV}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 39.4 \text{ mV or } 40.6 \text{ mV}$$

$$\text{Release Voltage} = V_{ITN} + V_{HYS} = 839.4 \text{ mV to } 840.6 \text{ mV}$$

Overvoltage (OV) Channel

$$V_{ITP} = 8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 2 \text{ V}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 1.97 \text{ V or } 2.03 \text{ V}$$

$$\text{Release Voltage} = V_{ITP} - V_{HYS} = 5.97 \text{ V to } 6.03 \text{ V}$$

8.3.3 Output Logic Configurations

TPS37 has two channels with separate sense pins and reset pins that can be configured independently of each other. Channel 1 is available as Open-Drain and Push-Pull while channel 2 is only available as Open-Drain topology.

The available output logic configuration combinations are shown in [Table 8-2](#).

Table 8-2. TPS37 Output Logic

DESCRIPTION	NOMENCLATURE	VALUE	
GPN	TPS37 (+ topology)	CHANNEL 1	CHANNEL 2
Topology (OV and UV only) both channels are either OV or UV - UV = Undervoltage - OV = Overvoltage - PP = Push-Pull - OD = Open-Drain - L = Active low - H = Active high	TPS37A	OV OD L	UV OD L
	TPS37B	OV PP H	UV OD L
	TPS37C	OV OD L	UV OD H
	TPS37D	OV PP H	UV OD H
	TPS37E	OV OD H	UV OD H
	TPS37F	OV PP H	UV OD L
	TPS37G	OV OD L	UV OD H
	TPS37H	OV OD H	UV OD L

8.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the (I_{lk}) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS37 open-drain output pin.

8.3.3.2 Push-Pull

Push-Pull output does not require an external resistor since is the output is internally pulled-up to VDD during V_{OH} condition and output will be connected to GND during V_{OH} condition.

8.3.3.3 Active-High (RESET)

RESET (active-high), denoted with no bar above the pin label. RESET remains low (V_{OL} , deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.3.4 Active-Low ($\overline{\text{RESET}}$)

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH} , deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.4 User-Programmable Reset Time Delay

TPS37 has adjustable reset release time delay with external capacitors. Channel timing are independent of each other.

- A capacitor in CTR1 / $\overline{MR}$ program the reset time delay of Output 1.
- A capacitor in CTR2 / $\overline{MR}$ program the reset time delay of Output 2.
- No capacitor on these pins gives the fastest reset delay time indicated in the [Section 7.6](#).

8.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR1 pin and GND, CTR2 for channel 2. In this section CTRx represent either channel 1 or channel 2.

The relationship between external capacitor C_{CTR_EXT} (typ) and the time delay t_{CTR} (typ) is given by [Equation 1](#).

$$t_{CTR} (typ) = -\ln (0.28) \times R_{CTR} (typ) \times C_{CTR_EXT} (typ) + t_{CTR} (no\ cap) \quad (1)$$

$R_{CTR} (typ)$ = is in kilo ohms (kOhms)

$C_{CTR_EXT} (typ)$ = is given in microfarads (μF)

$t_{CTR} (typ)$ = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in [Section 7.5](#), and a constant. The minimum and maximum variance due to the constant is show in [Equation 2](#) and [Equation 3](#):

$$t_{CTR} (min) = -\ln (0.31) \times R_{CTR} (min) \times C_{CTR_EXT} (min) + t_{CTR} (no\ cap) (min) \quad (2)$$

$$t_{CTR} (max) = -\ln (0.25) \times R_{CTR} (max) \times C_{CTR_EXT} (max) + t_{CTR} (no\ cap) (max) \quad (3)$$

The recommended maximum reset delay capacitor for the TPS37 is limited to 10 μF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

8.3.5 User-Programmable Sense Delay

TPS37 has adjustable sense release time delay with external capacitors. Channel timing are independent of each other. Sense delay is used as a de-glitcher or ignoring known transients.

- A capacitor in CTS1 program the excursion detection on SENSE1.
- A capacitor in CTS2 program the excursion detection on SENSE2.
- No capacitor on these pins gives the fastest detection time indicated in the [Section 7.6](#).

8.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS1 pin and GND, CTS2 for channel 2. In this section CTSx represent either channel 1 or channel 2.R

The relationship between external capacitor C_{CTS_EXT} (typ) and the time delay t_{CTSx} (typ) is given by [Equation 4](#).

$$t_{CTSx} \text{ (typ)} = -\ln(0.28) \times R_{CTSx} \text{ (typ)} \times C_{CTS_EXT} \text{ (typ)} + t_{CTSx} \text{ (no cap)} \quad (4)$$

R_{CTSx} = is in kilo ohms (kOhms)

C_{CTS_EXT} = is given in microfarads (μF)

t_{CTSx} = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTSx}) provided in [Section 7.5](#), and a constant. The minimum and maximum variance due to the constant is show in [Equation 5](#) and [Equation 6](#):

$$t_{CTSx} \text{ (min)} = -\ln(0.31) \times R_{CTSx} \text{ (min)} \times C_{CTS_EXT} \text{ (min)} + t_{CTSx} \text{ (no cap (min))} \quad (5)$$

$$t_{CTRx} \text{ (max)} = -\ln(0.25) \times R_{CTSx} \text{ (max)} \times C_{CTS_EXT} \text{ (max)} + t_{CTSx} \text{ (no cap (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the TPS37 is limited to 10 μF as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time between fault events to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or time duration between fault events needs to be greater than 10% of the programmed sense time delay.

8.3.6 Manual RESET (CTR1 / $\overline{\text{MR}}$) and (CTR2 / $\overline{\text{MR}}$) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section $\overline{\text{MR}}$ is a generic reference to (CTR1 / $\overline{\text{MR}}$) and (CTR2 / $\overline{\text{MR}}$). A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET1}}$ to assert on reset output. After $\overline{\text{MR}}$ is left floating, $\overline{\text{RESET1}}$ will release the reset if the voltage at SENSE1 pin is at nominal voltage. $\overline{\text{MR}}$ should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the $\overline{\text{MR}}$ cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in Figure 8-8.

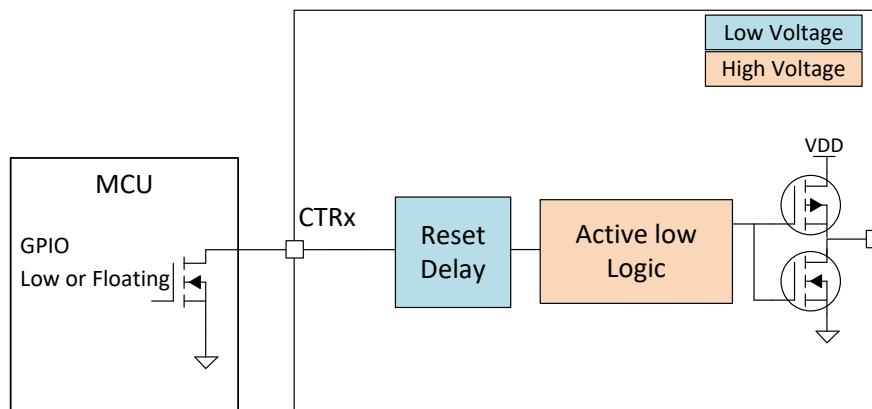


Figure 8-8. Manual Reset Implementation

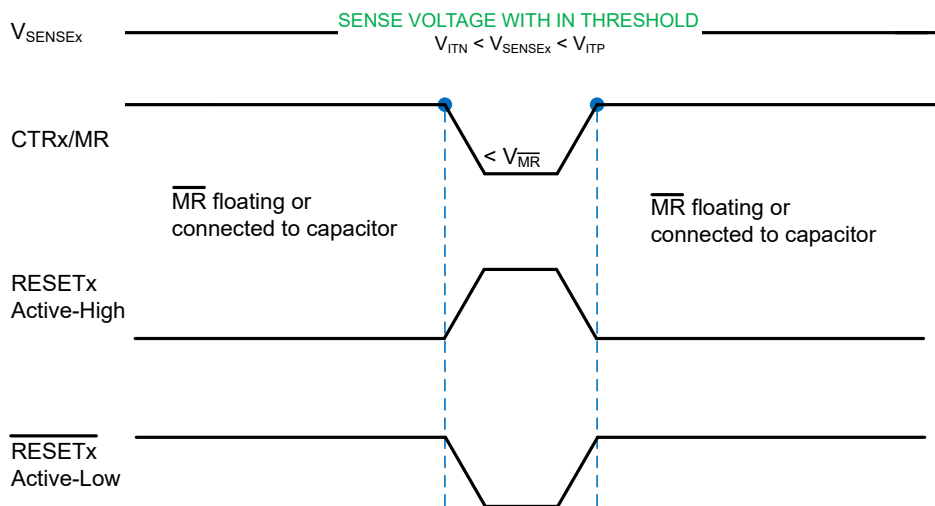


Figure 8-9. Manual Reset Timing Diagram

Table 8-3. $\overline{\text{MR}}$ Functional Table

$\overline{\text{MR}}$	SENSE ON NOMINAL VOLTAGE	RESET STATUS
Low	Yes	Reset asserted
Floating	Yes	Fast reset release when SENSE voltage goes back to nominal voltage
Capacitor	Yes	Programmable reset time delay
High	Yes	NOT Recommended

9 Device Functional Modes

Table 9-1. Undervoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR ⁽¹⁾ / MR PIN	VDD PIN	OUTPUT ⁽²⁾ (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Undervoltage Detection	$SENSE > V_{ITN(UV)}$	$SENSE < V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Undervoltage Detection	$SENSE < V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE < V_{ITN(UV)}$	$SENSE > V_{ITN(UV)} + HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Manual Reset	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Low	$V_{DD} > V_{DD(MIN)}$	Low
UVLO Engaged	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{POR} < V_{DD} < V_{DD(MIN)}$	Low
Below V_{POR} , Undefined Output	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

Table 9-2. Overvoltage Detect Functional Mode Truth Table

DESCRIPTION	SENSE		CTR ⁽¹⁾ / MR PIN	VDD PIN	OUTPUT ⁽²⁾ (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Overvoltage Detection	$SENSE < V_{ITN(OV)}$	$SENSE > V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Overvoltage Detection	$SENSE > V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE > V_{ITN(OV)}$	$SENSE < V_{ITN(OV)} - HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Manual Reset	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Low	$V_{DD} > V_{DD(MIN)}$	Low
UVLO Engaged	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{POR} < V_{DD} < UVLO$	Low
Below V_{POR} , Undefined Output	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Adjustable Voltage Thresholds

Equation 7 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored V_{MON} for undervoltage (UV) using channel 2 of the TPS37A010122DSKR variant. Using Equation 7 and shown in Figure 10-1, R_1 is the top resistor of the resistor divider that is between V_{MON} and V_{SENSE2} , R_2 is the bottom resistor that is between V_{SENSE2} and GND, V_{MON} is the voltage rail that is being monitored and V_{SENSE2} is the input threshold voltage. The monitored UV threshold, denoted as V_{MON-} , where the device will assert a reset signal occurs when $V_{SENSE2} = V_{IT-(UV)}$ or, for this example, $V_{MON-} = 10.8V$ which is 90% from 12 V. Using Equation 7 and assuming $R_2 = 10k\Omega$, R_1 can be calculated shown in Equation 8 where I_{R1} is represented in Equation 9:

$$V_{SENSE2} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

$$R_1 = (V_{MON-} - V_{SENSE2}) \div I_{R1} \quad (8)$$

$$I_{R1} = I_{R2} = V_{SENSE2} \div R_2 \quad (9)$$

Substituting Equation 9 into Equation 8 and solving for R_1 in Equation 7, $R_1 = 125k\Omega$. The TPS37A010122DSKR is typically meant to monitor a 0.8 V rail with $\pm 2\%$ voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} would need to go above $V_{IT-} + V_{HYS}$. For this example, $V_{MON} = 11.016 V$ when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance R_{SENSE} can be calculated by the SENSE voltage V_{SENSE} divided by the SENSE current I_{SENSE} as shown in Equation 11. V_{SENSE} can be calculated using Equation 7 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using Equation 10.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (10)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (11)$$

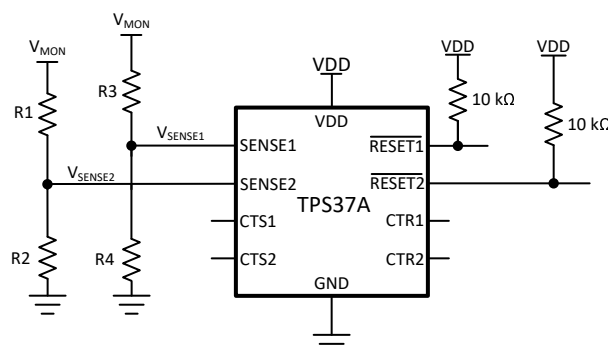


Figure 10-1. Adjustable Voltage Threshold with External Resistor Dividers

10.1.1 Application Curves

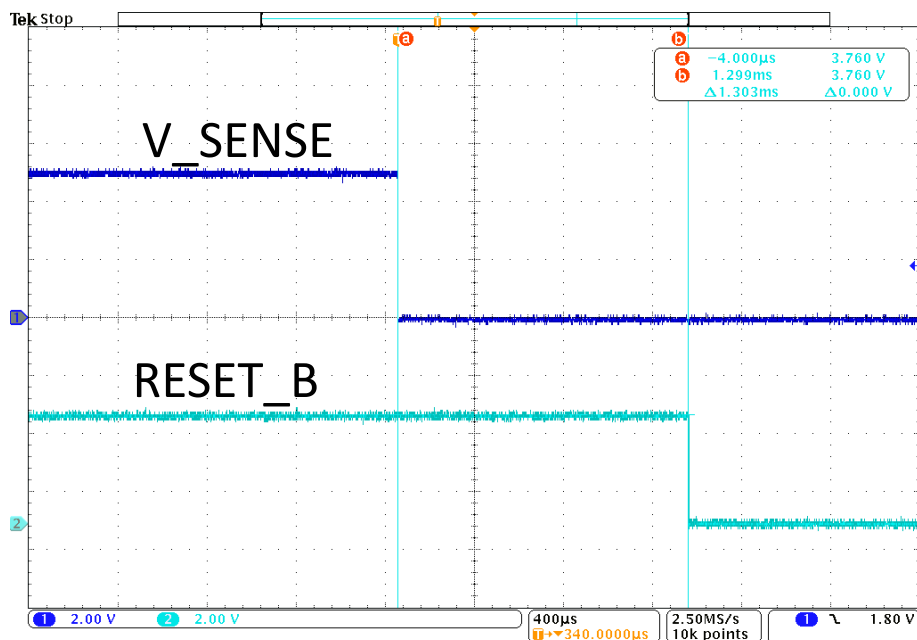


Figure 10-2. Undervoltage Reset Waveform

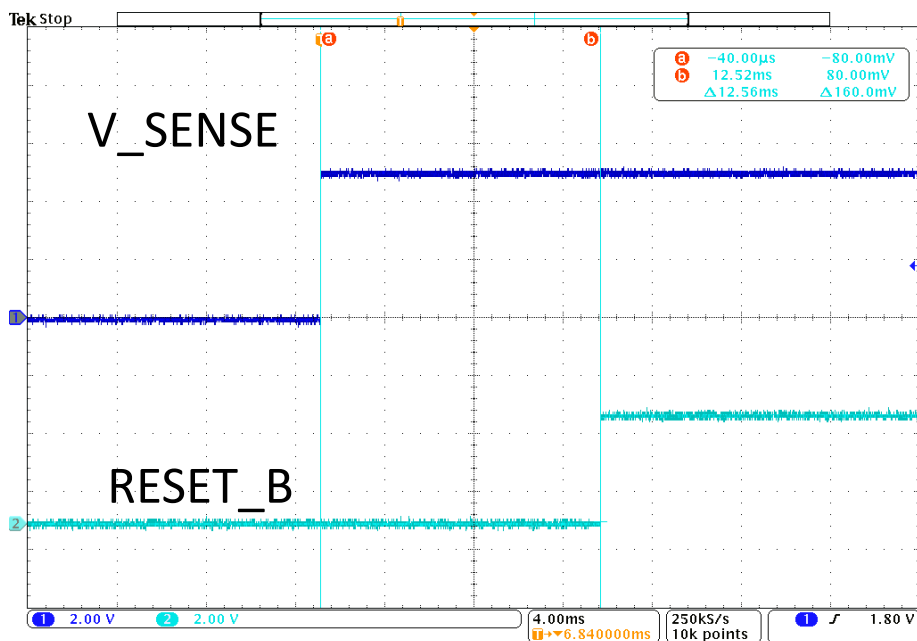


Figure 10-3. Undervoltage Recovery Waveform

10.2 Application Information

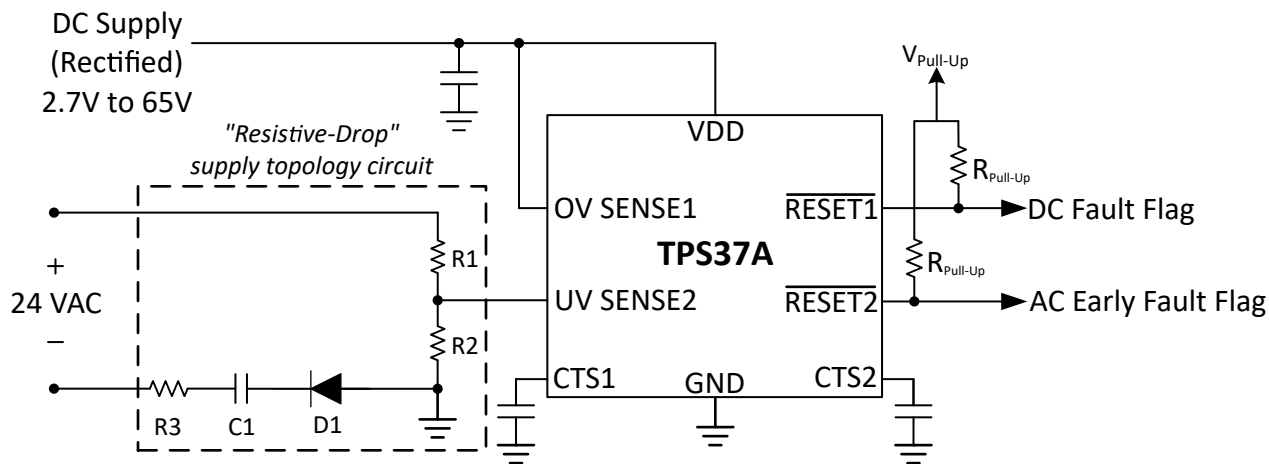
The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

10.2.1 Typical Application

10.2.1.1 Design 1: High Voltage – Fast AC Signal Monitoring For Power Fault Detection

In many industrial and factory automation applications, there are multiple power rails that power various subsystems within the application. Some of these power rails include 24 / 48 VAC AC sources with a known

operating frequency that requires a full-bridge rectifier and capacitors to convert its signal to a DC voltage where it can be monitored by a voltage supervisor. One drawback with the described conversion is the response time of the DC voltage when the AC power rail experiences a change of operating frequency or voltage amplitude. Due to the output filter of the full-bridge rectifier, the detection in the change of voltage or operating frequency may require several AC cycles before the voltage supervisor outputs a fault condition. The direct monitoring of the AC source by using a “Resistive-Drop” supply topology circuit provides the user a fast transient fault detection. In this design example, the TPS37A is being highlighted with the ability to offer a unique “window operating” solution by monitoring the output of the AC source for over or undervoltage operation.



* The circuit solution is not isolated and one must take into account when planning to use in high power systems.

Figure 10-4. Sensing an AC Signal for Power Fault Detection

10.2.1.1.1 Design Requirements

This design requires voltage supervision on an AC, with a known operating frequency, power supply rail. The overvoltage fault sensing is achieved by monitoring the DC output of a full bridge rectifier while the undervoltage fault is detected by inputting a half wave signal and its voltage frequency and magnitude are being monitored. The target output of this TPS37A application is for 5 V reset logic.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 24 VAC 800 Hz power supply for undervoltage and overvoltage conditions. Trigger undervoltage fault at 5 V and overvoltage fault at 24 V.	TPS37A provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations.
Maximum Input Voltage	Operate with power supply input up to 34 V.	The TPS37A can support a VDD of up to 65 V.
Output logic voltage	Open-Drain Output Topology	An open-drain output is recommended to provide the a 5 V reset signal.
SENSE Delay when a fault is detected	RESET delay of at least 0.625 ms which is the time between half wave cycles	$C_{CTS2} = 5.6 \text{ nF}$ sets 717 μs delay
Voltage Monitor Accuracy	Maximum voltage monitor accuracy of 1.5%.	The TPS37A has 1.5% maximum voltage monitor accuracy.

10.2.1.1.2 Detailed Design Procedure

The main advantage of this unique application is being able to monitor a single AC source with a known operating frequency AC source rail. Because the TPS37A is an over and undervoltage detector with delay function, detecting faults either from a change of operating frequency range or voltage amplitude of the AC source is achievable.

Figure 10-4 illustrates an example of how the TPS37A is monitoring an AC source. Input to SENSE1 of TPS37A is monitoring a full wave rectifier DC signal. The DC signal is the result from the rectification of the 24 VAC source and monitors the AC source for overvoltage events due to a change of voltage amplitude or an increase

to operating frequency. Input to SENSE2 of TPS37A will monitor the AC source by using a "resistive-drop" supply topology circuit. The unique circuit resistively divides the AC voltage signal and provides only the positive half wave [Figure 10-5](#) into SENSE2 input. The half wave signal does not go through any output filter and hence any change to the AC voltage or operating frequency can be rapidly detected. Knowing the operating frequency of the AC source and converting to the time domain, the TPS37A SENSE2 delay can be programmed, by the capacitor on CTS2 pin, to equal or be greater than one-half of the operating period (the frequency of the half wave rectification signal) or the half cycle shown in [Figure 10-5](#). When the half wave voltage amplitude falls below the SENSE2 threshold voltage, the SENSE2 time delay counter begins to increment. If the next half wave voltage amplitude exceeds the SENSE2 threshold voltage, the SENSE2 time delay counter will reset and the TPS37A RESET2 pin will indicate no fault was detected. Conversely, if the voltage amplitude of the half wave does not reach the SENSE2 threshold voltage within the programmed time delay of t_{CTS} , a fault will occur. Also, a fault can occur if the operating frequency from the AC source decreases, resulting in lower AC voltage amplitude at the programmed time delay t_{CTS} .

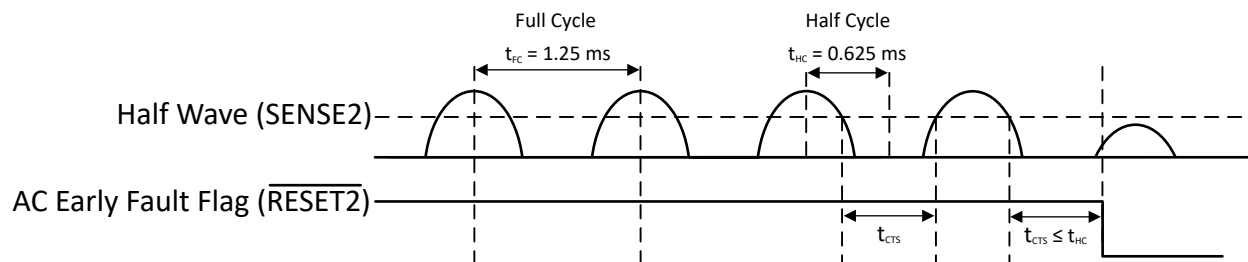


Figure 10-5. Design 2 Timing Diagram

The TPS37A, with its ability of having a wide VDD range from 2.7 V to 65 V and under and overvoltage detection, offers a unique "window operating" AC power rail monitoring solution. Combining SENSE delay feature with the "resistive-drop" supply circuitry, detecting an undervoltage event on the half cycle of the AC power rail provides a fast power fault response. Likewise, the TPS37A provides an overvoltage monitoring and SENSE delay fault detection for the same AC power rail. With under and overvoltage supervision of the AC power rail, applications needing a specific operating DC range to protect its subsystems is achieved through TPS37A. Good design practice recommends using a 0.1-μF capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.

Note that this design solution is not isolated and one must take into account when planning to use in high power systems.

11 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V (V_{POR}) to 65 V (max operation). Good analog design practice recommends placing a minimum 0.1 μ F ceramic capacitor as near as possible to the VDD pin.

11.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using [Equation 12](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (12)$$

The actual power being dissipated in the device can be represented by [Equation 13](#):

$$P_D = V_{DD} \times I_{DD} + P_{RESET} \quad (13)$$

P_{RESET} is calculated by [Equation 14](#) or [Equation 15](#)

$$P_{RESET} (PUSH/PULL) = V_{DD} - V_{RESET} \times I_{RESET} \quad (14)$$

$$P_{RESET} (OPEN-DRAIN) = V_{RESET} \times I_{RESET} \quad (15)$$

[Equation 12](#) and [Equation 13](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature (T_{A-MAX}) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature (T_{A-MAX}) may have to be de-rated. T_{A-MAX} is dependent on the maximum operating junction temperature ($T_{J-MAX-OP} = 125^\circ\text{C}$), the maximum allowable power dissipation in the device package in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by [Equation 16](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (16)$$

12 Layout

12.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 μ F ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSEx pins, placing a 10 nF to 100 nF capacitor between the SENSEx pins and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS1, CTS2, CTR1, or CTR2, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- For open-drain variants, place the pull-up resistors on $\overline{\text{RESET1}}$ and $\overline{\text{RESET2}}$ pins as close to the pins as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).
- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

12.2 Layout Example

The DSK layout example in [Figure 12-1](#) shows how the TPS37 is laid out on a printed circuit board (PCB) with user-defined delays.

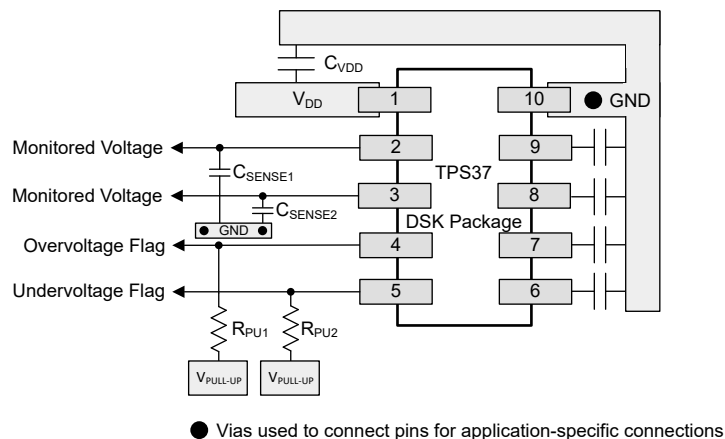


Figure 12-1. TPS37 DSK Package Recommended Layout

The DYY layout example in Figure 12-2 shows how the TPS37 is laid out on a printed circuit board (PCB) with user-defined delays.

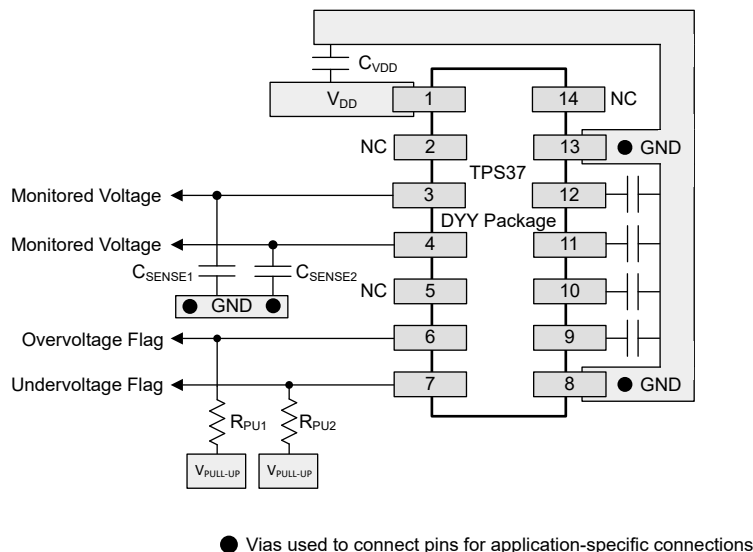


Figure 12-2. TPS37 DYY Package Recommended Layout

12.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in Figure 12-3 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

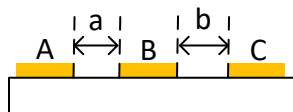


Figure 12-3. Creepage Distance

Figure 12-3 details:

- A = Left pins (high voltage)
- B = Central pad (not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltage)
- Creepage distance = $a + b$

13 Device and Documentation Support

13.1 Device Nomenclature

Section 5 shows how to decode the function of the device based on its part number

Table 13-1 shows TPS37 possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

Table 13-1. Voltage Options

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS
08	800 mV (divider bypass)	70	7.0 V	A0	10.4 V	D0	20.5 V	F0	31.0 V
27	2.7 V	71	7.1 V	A1	10.8 V	D1	21.0 V	F1	32.0 V
28	2.8 V	72	7.2 V	A2	11.2 V	D2	21.5 V	F2	33.0 V
29	2.9 V	73	7.3 V	A3	11.6 V	D3	22.0 V	F3	34.0 V
30	3.0 V	74	7.4 V	A4	12.0 V	D4	22.5 V	F4	35.0 V
31	3.1 V	75	7.5 V	A5	12.4 V	D5	23.0 V	F5	36.0 V
32	3.2 V	76	7.6 V	A6	12.8 V	D6	23.5 V		
33	3.3 V	77	7.7 V	A7	13.2 V	D7	24.0 V		
34	3.4 V	78	7.8 V	A8	13.6 V	D8	24.5 V		
35	3.5 V	79	7.9 V	A9	14.0 V	D9	25.0 V		
36	3.6 V	80	8.0 V	B0	14.4 V	E0	25.5 V		
37	3.7 V	81	8.1 V	B1	14.8 V	E1	26.0 V		
38	3.8 V	82	8.2 V	B2	15.2 V	E2	26.5 V		
39	3.9 V	83	8.3 V	B3	15.6 V	E3	27.0 V		
40	4.0 V	84	8.4 V	B4	16.0 V	E4	27.5 V		
41	4.1 V	85	8.5 V	B5	16.4 V	E5	28.0 V		
42	4.2 V	86	8.6 V	B6	16.8 V	E6	28.5 V		
43	4.3 V	87	8.7 V	B7	17.2 V	E7	29.0 V		
44	4.4 V	88	8.8 V	B8	17.6 V	E8	29.5 V		
45	4.5 V	89	8.9 V	B9	18.0 V	E9	30.0 V		
46	4.6 V	90	9.0 V	C0	18.4 V				
47	4.7 V	91	9.1 V	C1	18.8 V				
48	4.8 V	92	9.2 V	C2	19.2 V				
49	4.9 V	93	9.3 V	C3	19.6 V				
50	5.0 V	94	9.4 V	C4	20.0 V				
51	5.1 V	95	9.5 V						
52	5.2 V	96	9.6 V						
53	5.3 V	97	9.7 V						
54	5.4 V	98	9.8 V						
55	5.5 V	99	9.9 V						
56	5.6 V	00	10.0 V						
57	5.7 V								
58	5.8 V								
59	5.9 V								
60	6.0 V								
61	6.1 V								

Table 13-1. Voltage Options (continued)

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS
62	6.2 V								
63	6.3 V								
64	6.4 V								
65	6.5 V								
66	6.6 V								
67	6.7 V								
68	6.8 V								
69	6.9 V								

13.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

13.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

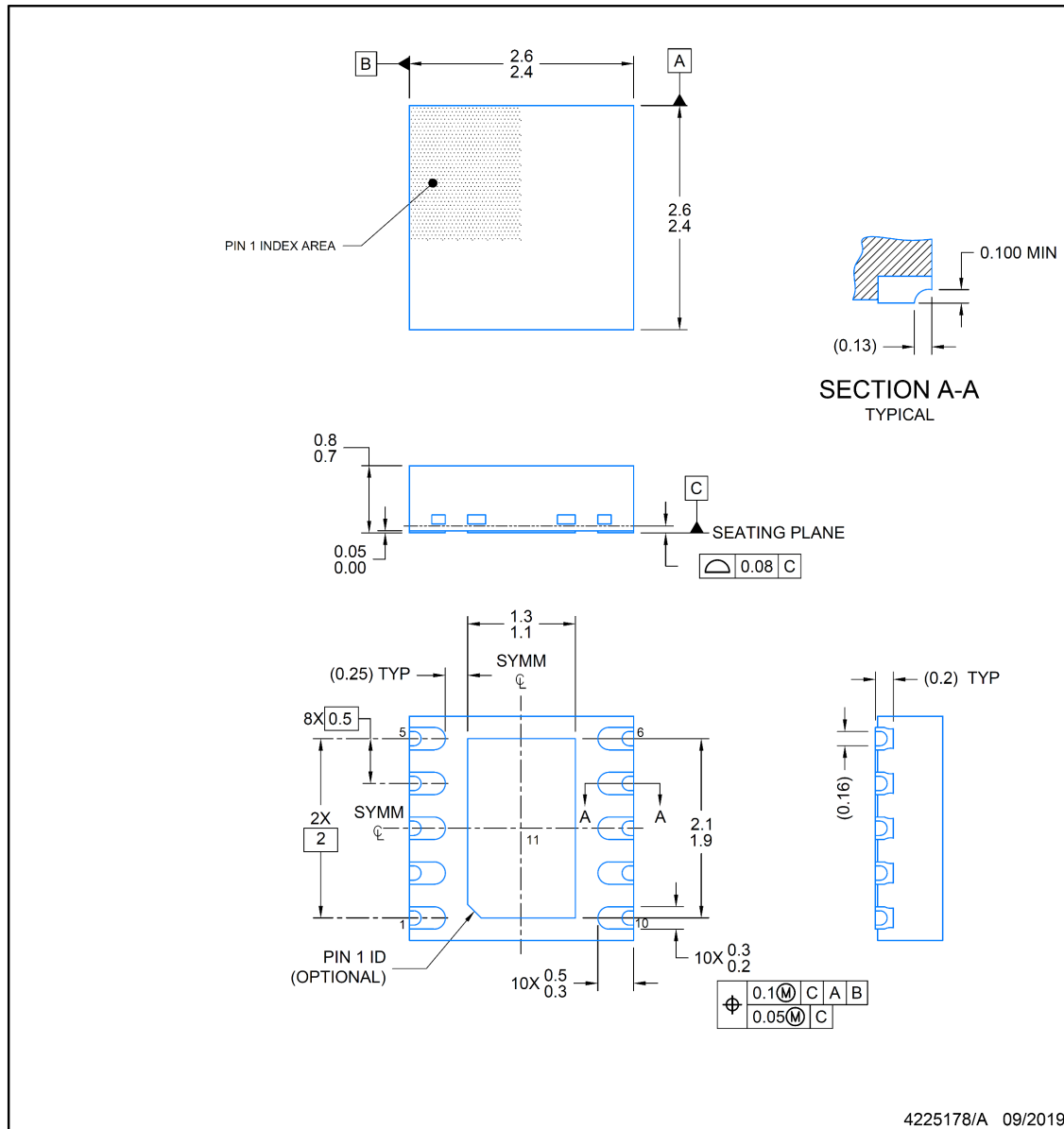
[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

DSK0010C**PACKAGE OUTLINE****WSN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD

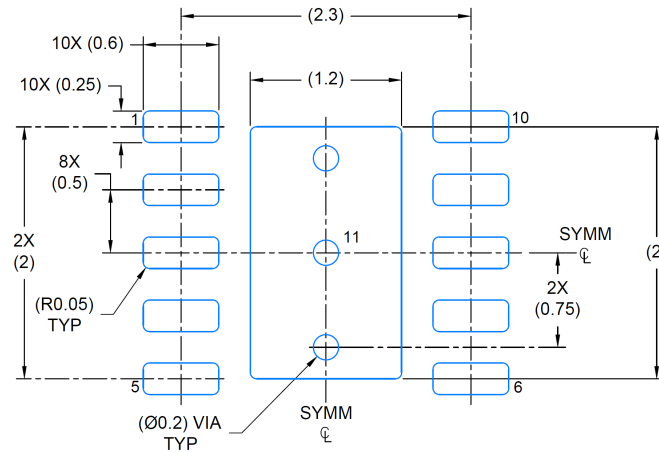


EXAMPLE BOARD LAYOUT

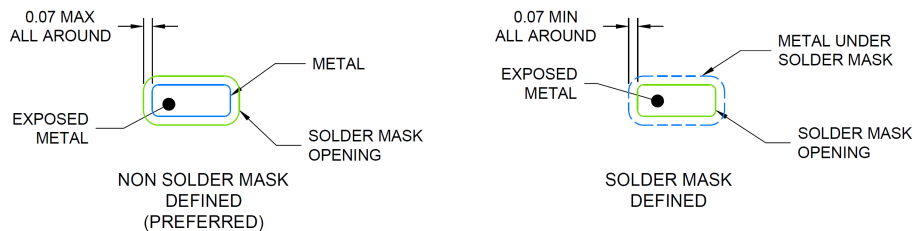
DSK0010C

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

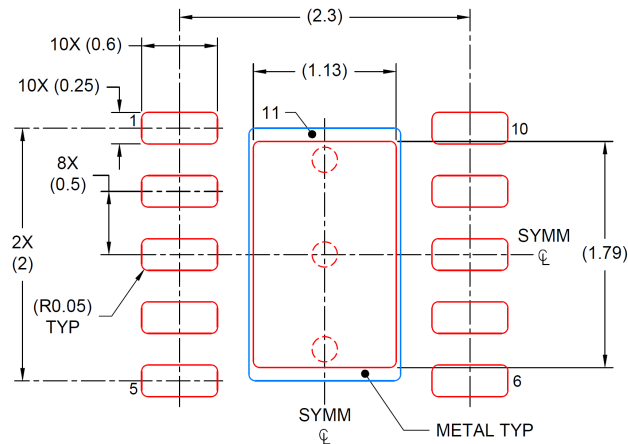
4225178/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN**DSK0010C****WSN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

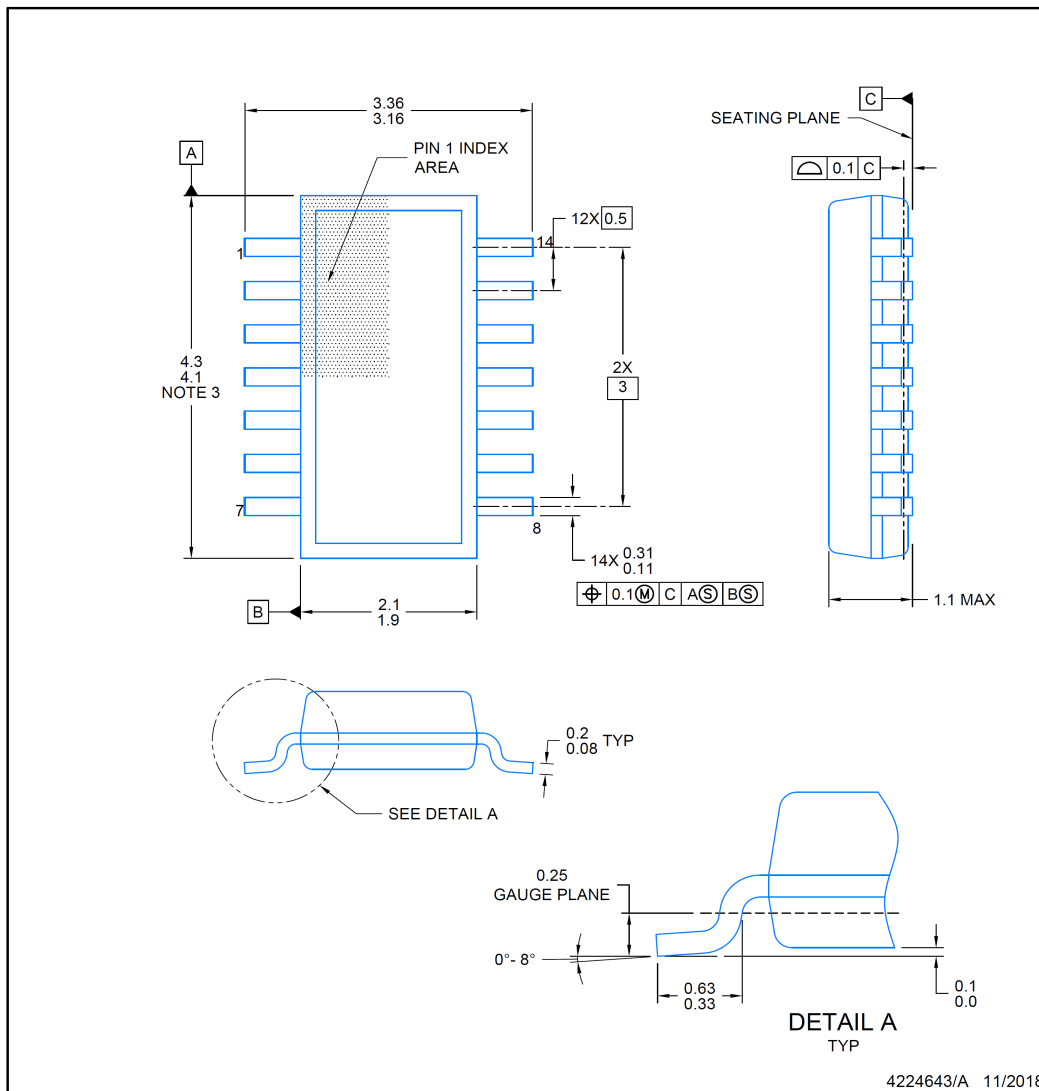
EXPOSED PAD
 84% PRINTED COVERAGE BY AREA
 SCALE: 20X

4225178/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DYY0014A **PACKAGE OUTLINE**
SOT-23-THIN - 1.1 mm max height
PLASTIC SMALL OUTLINE

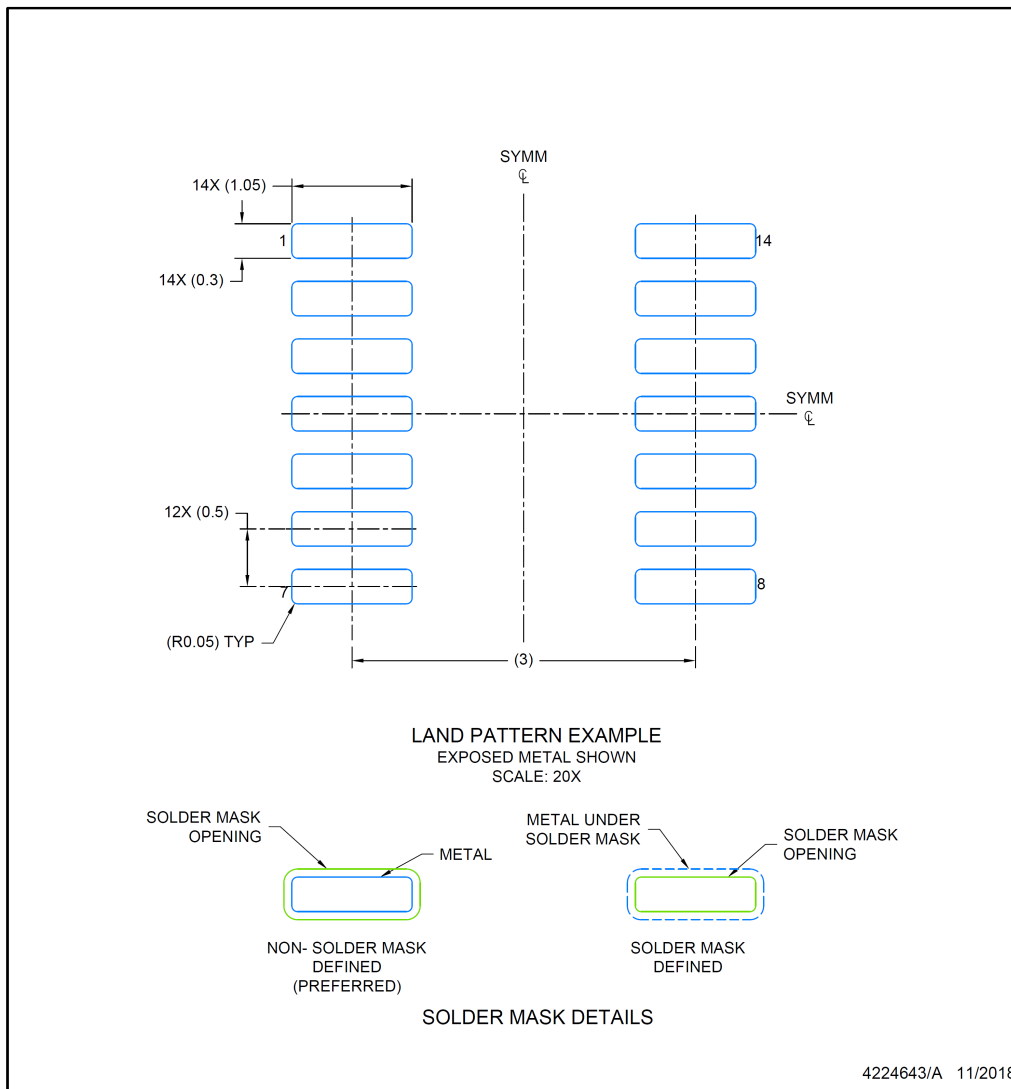


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.

DYY0014A
EXAMPLE BOARD LAYOUT
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



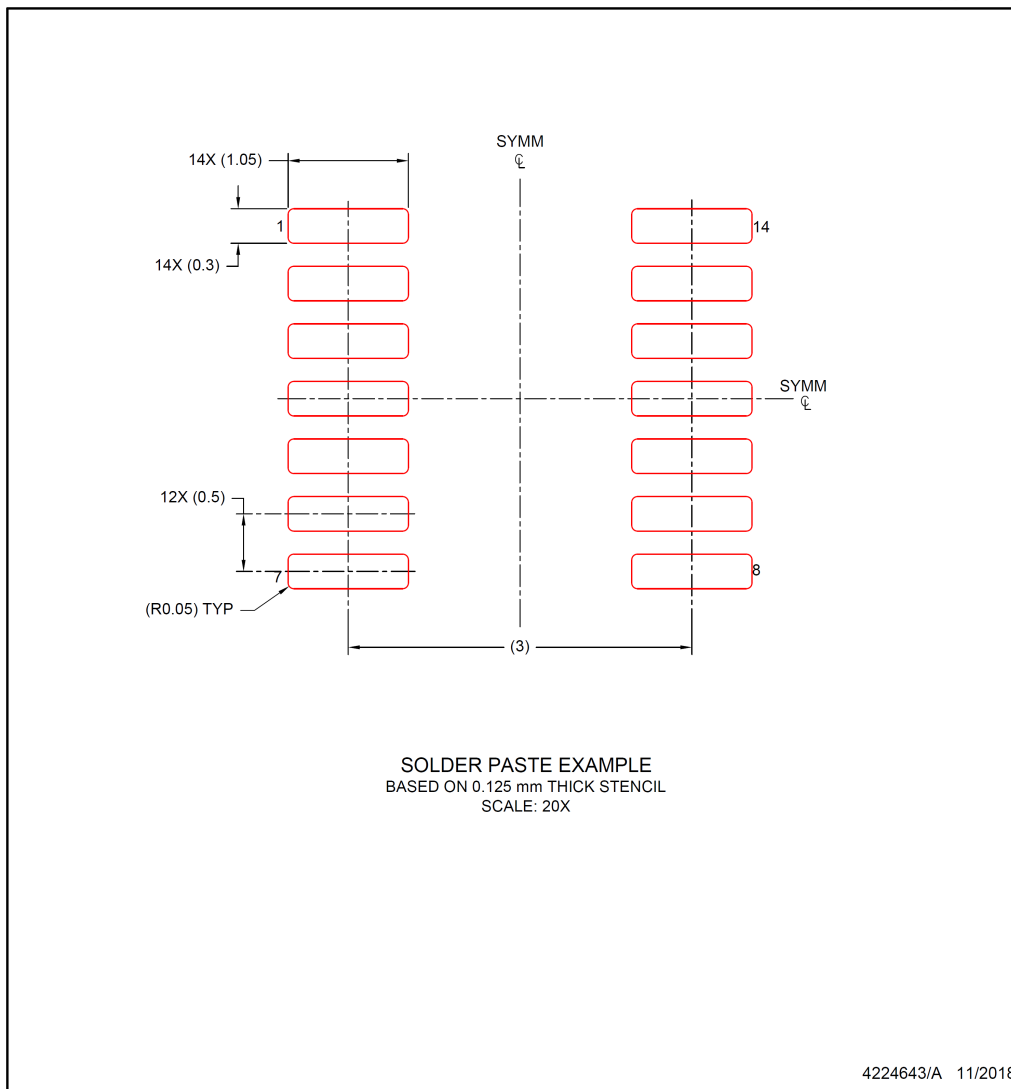
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYY0014A SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS37A010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2KAL	Samples
TPS37B010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2K8L	Samples
TPS37F010122DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2K9L	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

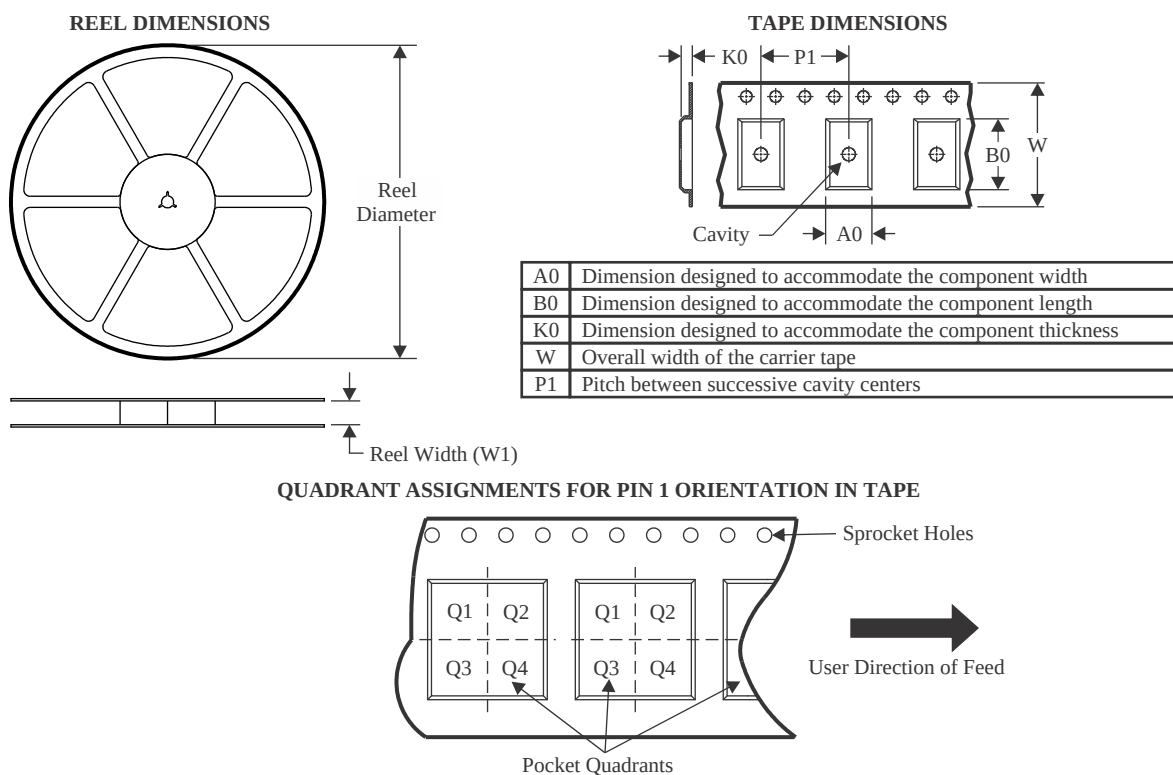
OTHER QUALIFIED VERSIONS OF TPS37 :

- Automotive : [TPS37-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

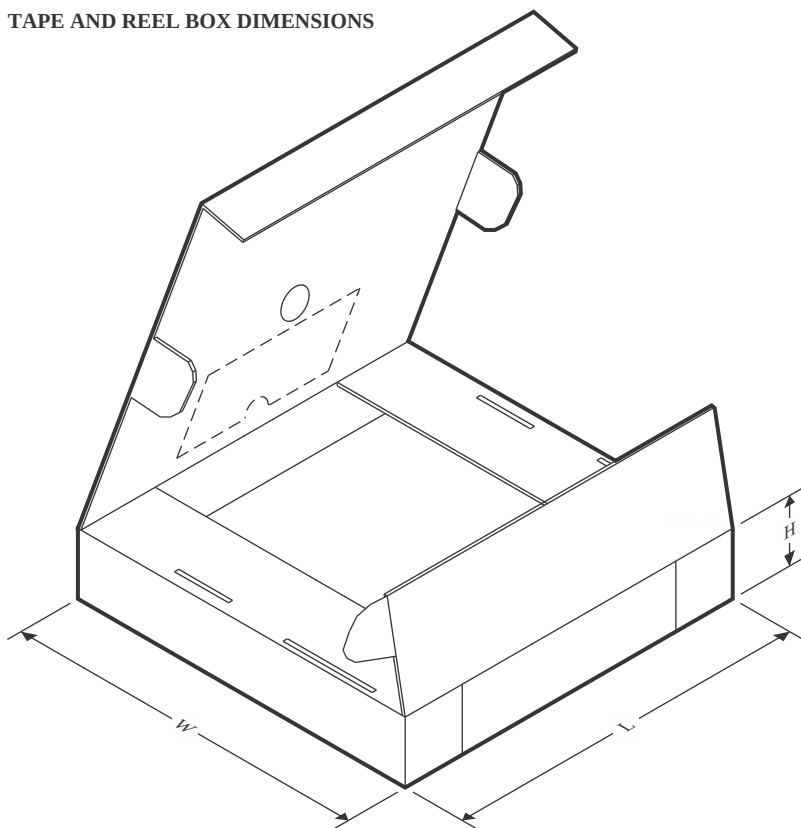
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS37A010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS37B010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS37F010122DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

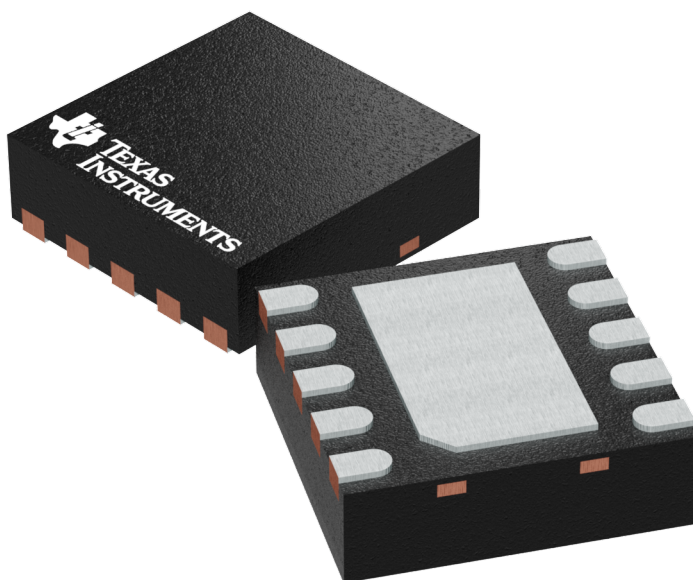
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS37A010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0
TPS37B010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0
TPS37F010122DSKR	SON	DSK	10	3000	210.0	185.0	35.0

DSK 10

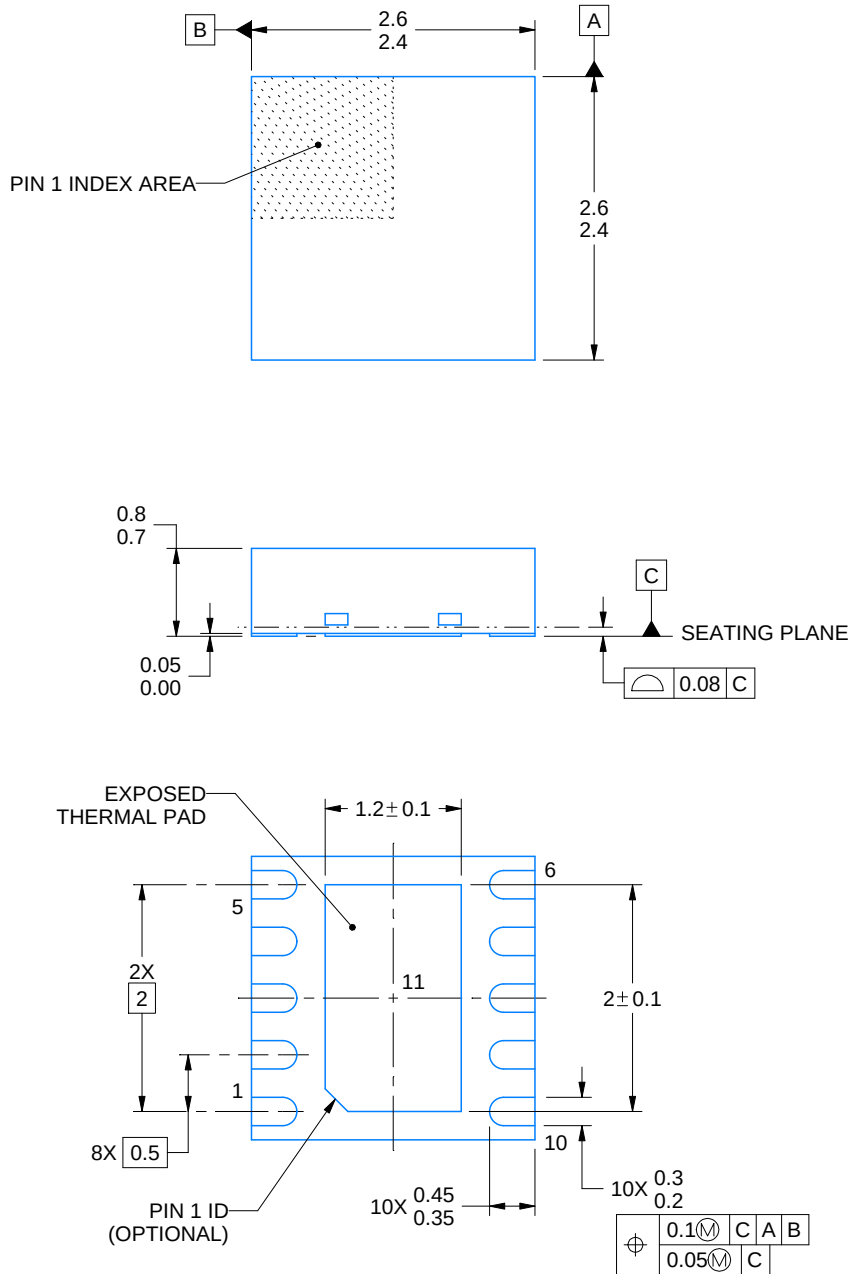
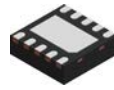
WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4218903/B 10/2020

NOTES:

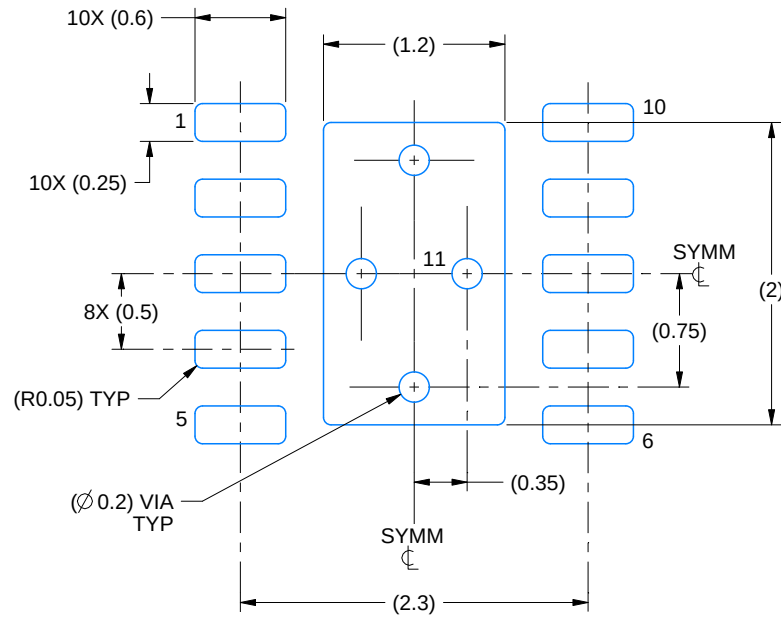
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

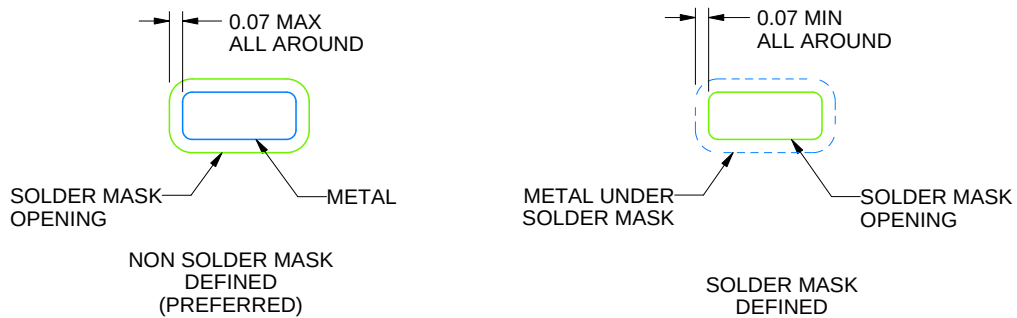
DSK0010A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

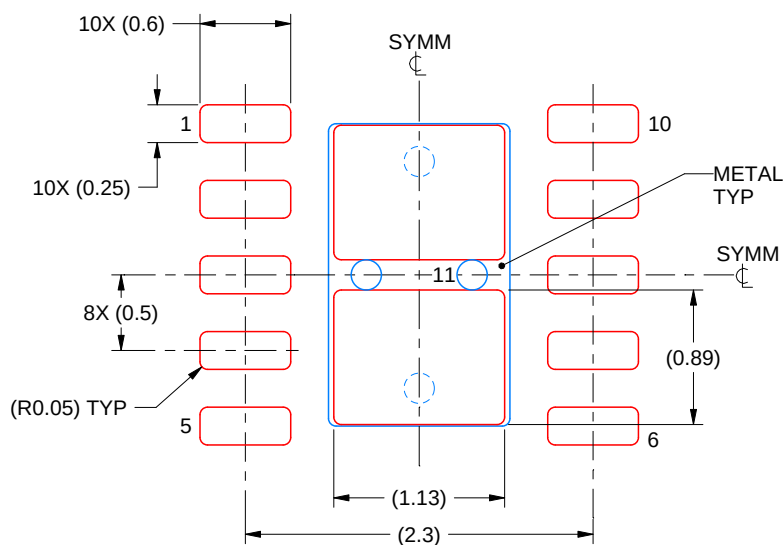
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DSK0010A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated