

✓ 54/74122 010 656 03251

RETRIGGERABLE RESETTABLE MULTIVIBRATOR

DESCRIPTION — The '122 features positive and negative dc level triggering inputs, complementary outputs, an optional 10 kΩ internal timing resistor and an overriding Direct Clear ($\bar{C}_D$) input. When the circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per Truth Table) will cause the delay period to start again, without disturbing the outputs. This process can be repeated indefinitely and thus the output pulse period (Q HIGH, $\bar{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated by a LOW signal applied to $\bar{C}_D$, which also prevents triggering. An internal connection from $\bar{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\bar{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows:

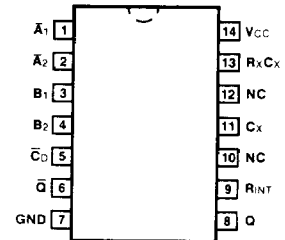
$$t_w = 0.32 R_x C_x (1.0 + 0.7/R_x)$$

Where t_w is in ns, R_x is in kΩ and C_x is in pF.

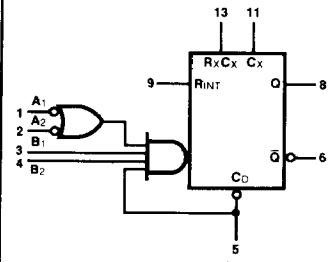
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0 \text{ V}, \pm 5\%$ $T_A = 0^\circ \text{ C to } +70^\circ \text{ C}$	$V_{CC} = +5.0 \text{ V} \pm 10\%$ $T_A = -55^\circ \text{ C to } +125^\circ \text{ C}$	
Plastic DIP (P)	A	74122PC		9A
Ceramic DIP (D)	A	74122DC	54122DM	6A
Flatpak (F)	A	74122FC	54122FM	3I

CONNECTION DIAGRAM PINOUT A



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7
NC = Pins 10, and 12

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1, \bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\bar{C}_D$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q, $\bar{Q}$	Outputs	20/10

TRIGGERING TRUTH TABLE

INPUTS*					RESPONSE
$\bar{C}_D$	$\bar{A}_1$	$\bar{A}_2$	B ₁	B ₂	
L	X	X	X	X	No Trigger
X		L	X	X	No Trigger
X		X	L	X	No Trigger
H		H	H	H	Trigger
X	X	X		L	No Trigger
X	H	H		X	No Trigger
H	L	X		H	Trigger
	L	X	H	H	Trigger

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

*Input pins 1 and 2 are logically interchangeable, as are input pins 3 and 4.

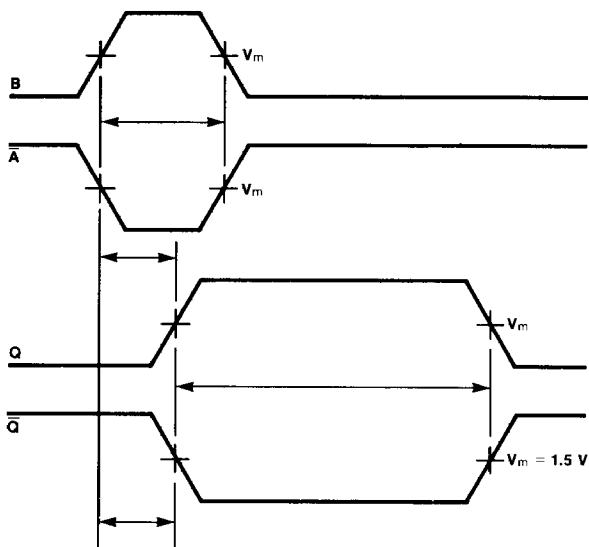
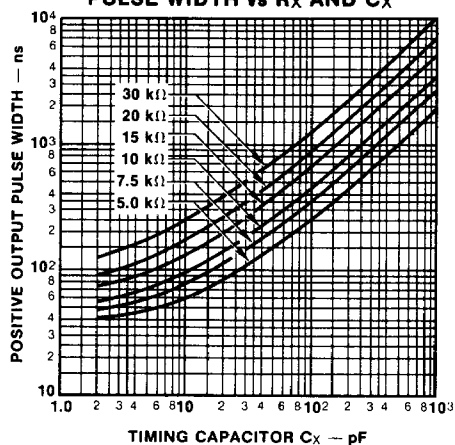
PULSE WIDTH vs R_X AND C_X

Fig. a

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I _{OS}	Output Short Circuit Current	-10	-40	mA	V _{CC} = Max
I _{CC}	Power Supply Current		28	mA	V _{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω			
		Min	Max		
t _{PLH}	Propagation Delay B to Q		28	ns	C _x = 0 pF, R _x = 5 kΩ Fig. 3-1, Fig. a
t _{PLH}	Propagation Delay $\bar{A}_n$ to Q		33	ns	
t _{PHL}	Propagation Delay B to $\bar{Q}$		36	ns	
t _{PHL}	Propagation Delay $\bar{A}_n$ to $\bar{Q}$		40	ns	
t _{PLH}	Propagation Delay $\bar{C}_D$ to $\bar{Q}$		40	ns	C _x = 0 pF, R _x = 5 kΩ Figs. 3-1, 3-10
t _{PHL}	Propagation Delay $\bar{C}_D$ to Q		27	ns	
t _{w(out)}	Pulse Width at Q with Zero Timing Capacitor		65	ns	C _x = 0 pF, R _x = 5 kΩ Fig. 3-1, Fig. a
t _{w(out)}	Pulse Width with External Timing Components	3.08	3.76	μs	C _x = 1000 pF, R _x = 10 kΩ Figs. 3-1, Fig. a

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER		54/74		UNITS	CONDITIONS
			Min	Max		
t _w	Trigger Pulse Width		40		ns	Over Operating V _{CC} and Temperature Range
R _x	External Timing Resistor	XC	5.0	50	kΩ	
		XM	5.0	25		
C _x	External Timing Capacitor		No Restrictions		pF	