

**NOT RECOMMENDED
FOR NEW DESIGNS**
 Use CMOS Technology

January 1997

CD74FCT823A, CD74FCT824A

**BiCMOS FCT Interface Logic,
9-Bit D-Type Flip-Flops, Three-State**

Features

- Buffered Inputs
- Typical Propagation Delay: 7.5ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- Positive Edge Triggered
- CD74FCT824A
 - Inverting
- CD74FCT823A
 - NonInverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at $V_{CC} = 5V$
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT823AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT824AEN	0 to 70	24 Ld PDIP	E24.3

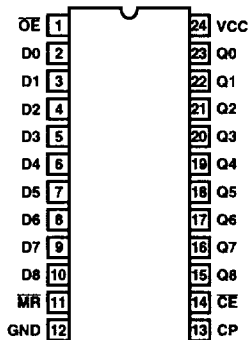
Description

The CD74FCT823A and CD74FCT824A nine bit, D-Type, three-state, positive edge triggered flip-flops use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC} . This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

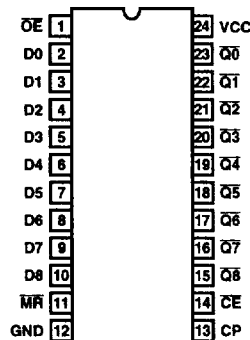
The nine flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable (OE) controls the three-state outputs and is independent of the register operation. These nine bit wide buffered registers with clock Enable (CE) and Master Reset (MR) inputs are ideal for parity bus interfacing in high performance microprogrammed systems.

Pinout

CD74FCT823A
(PDIP)
TOP VIEW



CD74FCT824A
(PDIP)
TOP VIEW

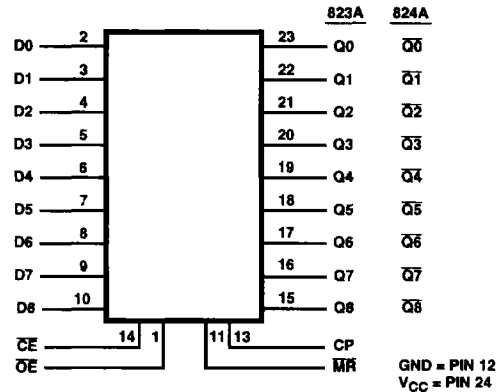


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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CD74FCT823A, CD74FCT824A

Functional Diagram



TRUTH TABLE (Note 1)

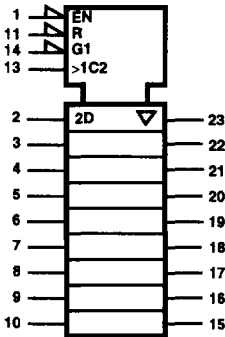
INPUTS					Q OUTPUTS		FUNCTION
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	D	CP	CD74FCT823A	CD74FCT824A	
H	X	L	L	$\uparrow$	Z	Z	High Z
H	X	L	H	$\uparrow$	Z	Z	
H	L	X	X	X	Z	Z	Reset
L	L	X	X	X	L	L	
H	H	H	X	X	Z	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	$\uparrow$	Z	Z	Load
H	H	L	H	$\uparrow$	Z	Z	
L	H	L	L	$\uparrow$	L	H	
L	H	L	H	$\uparrow$	H	L	

NOTE:

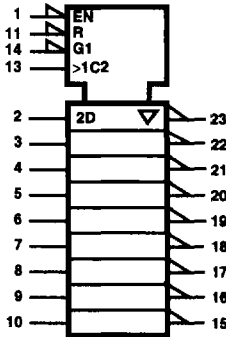
- 1. H= HIGH Voltage Level
- L = LOW Voltage Level
- NC = No Change
- $\uparrow$ = LOW to HIGH Transition
- X = Don't Care
- Z = HIGH Impedance

IEC Logic Symbol

CD74FCT823A



CD74FCT824A



CD74FCT823A, CD74FCT824A

Absolute Maximum Ratings

DC Supply Voltage (V_{CC})	-0.5V to 6V
DC Diode Current, I_{IK} (For $V_I < -0.5V$)	-20mA
DC Output Diode Current, I_{OK} (for $V_O < -0.5V$)	-50mA
DC Output Sink Current per Output Pin, I_O	70mA
DC Output Source Current per Output Pin, I_O	-30mA
DC V_{CC} Current (I_{CC})	234mA
DC Ground Current (I_{GND})	453mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	75
Maximum Junction Temperature	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$

Operating Conditions

Operating Temperature Range, T_A	0 $^{\circ}C$ to 70 $^{\circ}C$
Supply Voltage Range, V_{CC}	4.75V to 5.25V
DC Input Voltage, V_I	0 to V_{CC}
DC Output Voltage, V_O	0 to $\leq V_{CC}$
Input Rise and Fall Slew Rate, dt/dv	0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0 $^{\circ}C$ to 70 $^{\circ}C$, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T _A)				UNITS
					25°C		0°C TO 70°C		
		V _I (V)	I _O (mA)		V _{CC} (V)	MIN	MAX	MIN	
High Level Input Voltage	V _{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V _{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I _{IH}	V _{CC}		Max	-	0.1	-	1	μA
Low Level Input Current	I _{IL}	GND		Max	-	-0.1	-	-1	μA
Three-State Leakage Current	I _{OZH}	V _{CC}		Max	-	0.5	-	10	μA
	I _{OZL}	GND		Max	-	-0.5	-	-10	μA
Input Clamp Voltage	V _{IK}	V _{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I _{OS}	V _O = 0 V _{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	Max	-	8	-	80	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI _{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

- Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
- Inputs that are not measured are at V_{CC} or GND.
- FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70 $^{\circ}C$.

CD74FCT823A, CD74FCT824A

Switching Specifications Over Operating Range FCT Series $t_r, t_f = 2.5\text{ns}$, $C_L = 50\text{pF}$, R_L (Figure 1)

PARAMETER	SYMBOL	V _{CC} (V)	25°C	0°C TO 70°C		UNITS	
			TYP	MIN	MAX		
Propagation Delays		(Note 6)					
Clock to Q	CD74FCT823A	t _{PLH} , t _{PHL}	5	7.5	1.5	10	ns
Clock to $\overline{Q}$	CD74FCT824A	t _{PLH} , t _{PHL}	5	7.5	1.5	10	ns
$\overline{MR}$ to Q		t _{PHL}	5	10.5	1.5	14	ns
Output Enable to Q	CD74FCT823A	t _{PZL} , t _{PZH}	5	9	1.5	12	ns
Output Disable to Q	CD74FCT823A	t _{PLZ} , t _{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$	CD74FCT824A	t _{PZL} , t _{PZH}	5	9	1.5	12	ns
Output Disable to $\overline{Q}$	CD74FCT824A	t _{PLZ} , t _{PHZ}	5	6	1.5	8	ns
Power Dissipation Capacitance	C _{PD} (Note 7)	-	-	-	-	-	pF
Minimum (Valley) V _{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV}	5	0.5	-	-	-	V
Maximum (Peak) V _{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP}	5	1	-	-	-	V
Input Capacitance	C _I	-	-	-	-	10	pF
Three-State Output Capacitance	C _O	-	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.

7. C_{PD} , measured per flip-flop, is used to determine the dynamic power consumption.

P_D (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:

V_{CC} = supply voltage

ΔI_{CC} = flow through current x unit load

C_L = output load capacitance

D = duty cycle of input high

f_O = output frequency

f_I = input frequency

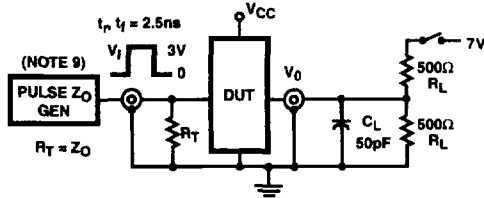
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Maximum Clock Frequency	f_{MAX}	5 (Note 8)	-	70	-	MHz
Master Reset Recovery Time	t_{REC}	5	-	7	-	ns
Setup Time, Data to Clock, $\overline{CE}$ to Clock	t_{SU}	5	-	4	-	ns
Hold Time - Data, $\overline{CE}$	t_H	5	-	2	-	ns
Pulse Width - Clock, $\overline{MR}$	t_W	5	-	7	-	ns

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$; $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

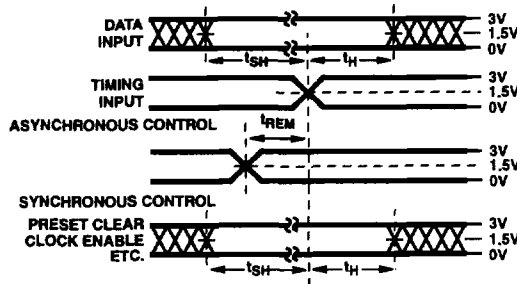


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL} , Open Drain	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

$V_{IN} = 0\text{V}$ to 3V .

Input: $t_r = t_f = 2.5\text{ns}$ (10% to 90%), unless otherwise specified

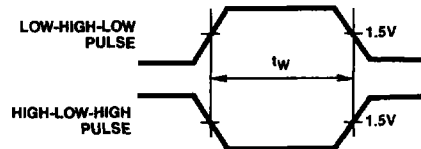


FIGURE 3. PULSE WIDTH

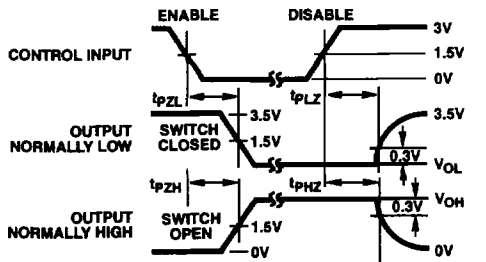


FIGURE 4. ENABLE AND DISABLE TIMING

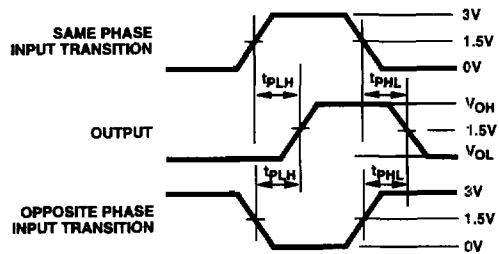
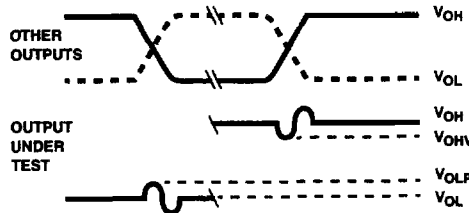


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH} .
11. Input pulses have the following characteristics:
 $P_{RR} \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS