Am29861A

High-Performance Bus Transceiver

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

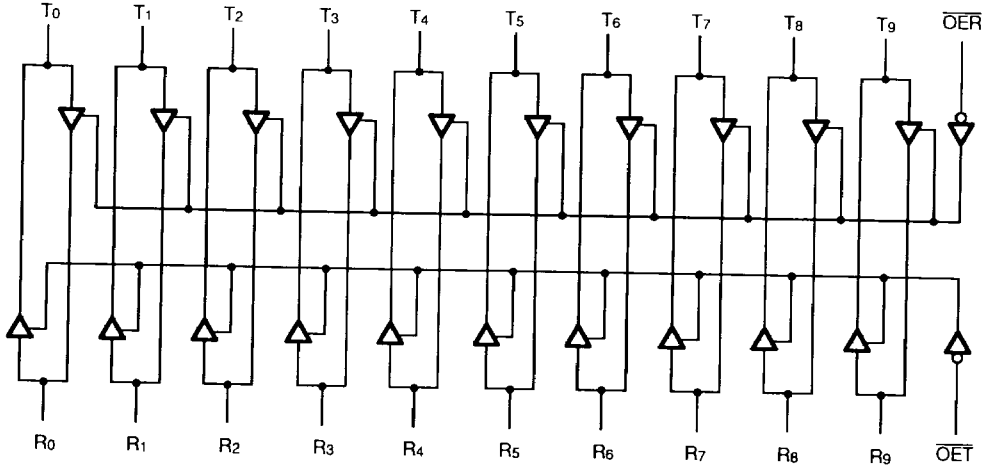
- **High-speed symmetrical bidirectional transceiver**
  - t_{PD} = 5 ns typical
- **200–mV minimum input hysteresis on input data ports**
- **Three-state outputs glitch-free during power-up and down**
- **I_{OL}: 48 mA commercial**
- **Higher speed, lower power version of the Am29861**

GENERAL DESCRIPTION

The Am29861A Bus Transceiver provides high-performance bus interface buffering for wide address/data paths or buses carrying parity. The device is a 10-bit bidirectional transceiver. The device features data inputs with 200–mV minimum input hysteresis to provide improved noise immunity. The Am29861A is produced with AMD's proprietary IMOX bipolar process, and features typical propagation delays of 5 ns.

Each member of the Am29800A Bus Interface Family is designed to drive high-capacitive loads while providing low-capacitive bus loading at both the inputs and outputs.

BLOCK DIAGRAM



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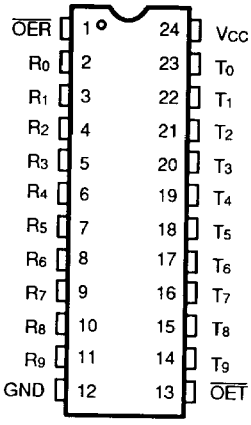
Publication# 07142 Rev. D Amendment/0
Issue Date: December 1990

CONNECTION DIAGRAM
Top View

DIP



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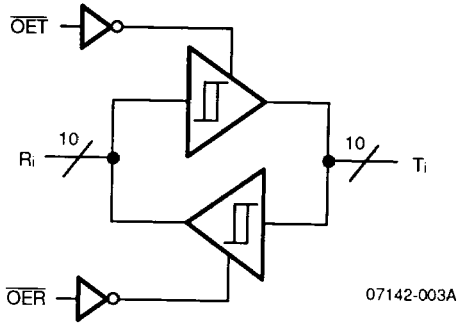
LOGIC SYMBOLS



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FUNCTION TABLE

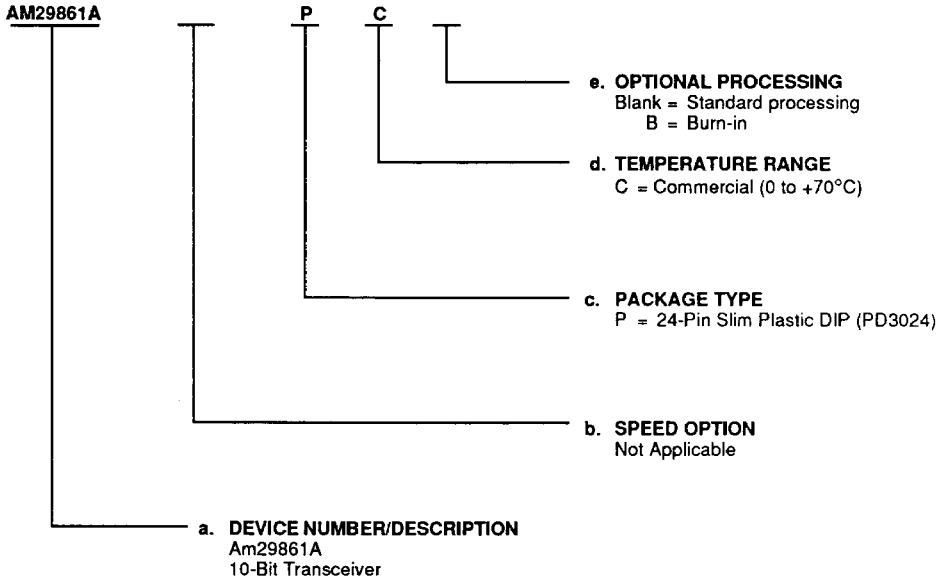
Inputs				Outputs		
$\overline{OET}$	$\overline{OER}$	R_i	T_i	R_i	T_i	Function
L	H	L	N/A	N/A	L	Transmit
L	H	H	N/A	N/A	H	Transmit
H	L	N/A	L	L	N/A	Receive
H	L	N/A	H	H	N/A	Receive
H	H	X	X	Z	Z	Hi–Z

H = HIGH
L = LOW
Z = High Impedance
X = Don't Care
N/A = Not Applicable

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29861A	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION
Am29861A

$\overline{OER}$
Output Enable-Receive (Input, Active LOW)

When LOW in conjunction with $\overline{OET}$ HIGH, the devices are in the Receive mode (R_i are outputs, T_i are inputs).

$\overline{OET}$
Output Enable–Transmit (Input, Active LOW)

When LOW in conjunction with $\overline{OER}$ HIGH, the devices are in the Transmit mode (R_i are inputs, T_i are outputs).

R_i
Receive Port (Input/Output)

R_i are the 10-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

T_i
Transmit Port (Input/Output)

T_i are the 10-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Ambient Temperature with Power Applied	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Output For High Output State	−0.5 V to +5.5 V
DC Input Voltage	−1.5 V to +6.0 V
DC Output Current, Into Outputs	100 mA
DC Input Current	−30 mA to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Suppy Voltage (V_{CC})	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −15 mA	2.4		V
			I_{OH} = −24 mA	2.0		
V_{OL}	Output LOW Voltage	V_{CC} = 4.5 V, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed input logical HIGH voltage for all inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed input logical LOW voltage for all inputs (Note 1)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.5 V, I_{IN} = −18 mA			−1.2	V
V_{HYST}	Input Hysteresis			200		mV
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−0.5	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			50	µA
I_I	Input HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			100	µA
I_{ZL}	I/O Port LOW Current	V_{CC} = 5.5 V, V_{IN} = 0.4 V			−550	µA
I_{ZH}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 2.7 V			100	µA
I_{ZI}	I/O Port HIGH Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V			150	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = 5.5 V, V_{OUT} = 0 V (Note 2)		−75	−250	mA
I_{OFF}	Bus Leakage Current	V_{CC} = 0 V, V_{OUT} = 2.9 V			100	µA
I_{CC}	Supply Current	V_{CC} = 5.5 V, Outputs Unloaded	Outputs LOW		140	mA
			Outputs HIGH		115	
			Outputs Hi–Z		130	

Notes:

1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.
2. Not more than one output shorted at a time. Duration of short-circuit test should not exceed one second

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

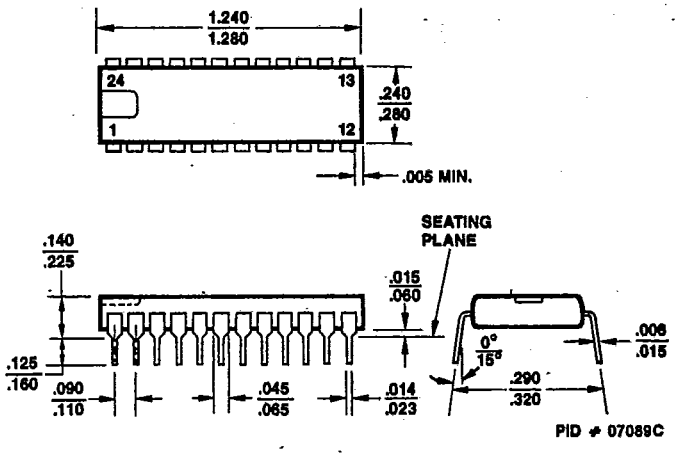
Symbol	Parameter Description	Parameter Test Conditions*	Min	Max	Unit
t_{PLH}	Propagation Delay from	C_L = 50 pF R_1 = 500 Ω R_2 = 500 Ω		8	ns
t_{PHL}	R_i to T_i or T_i to R_i			8	ns
t_{ZH}	Output Enable Time $\overline{OET}$ to			11	ns
t_{ZL}	T_i or $\overline{OER}$ to R_i			12	ns
t_{HZ}	Output Disable Time OET to			10	ns
t_{LZ}	T_i or $\overline{OER}$ to R_i			10	ns

* See Test Circuit and Waveforms. (Chapter 2)

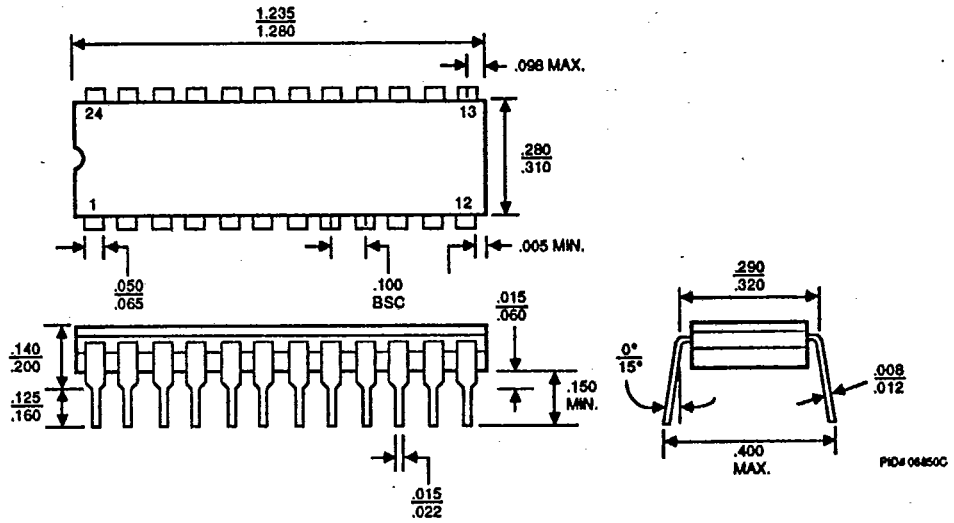
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

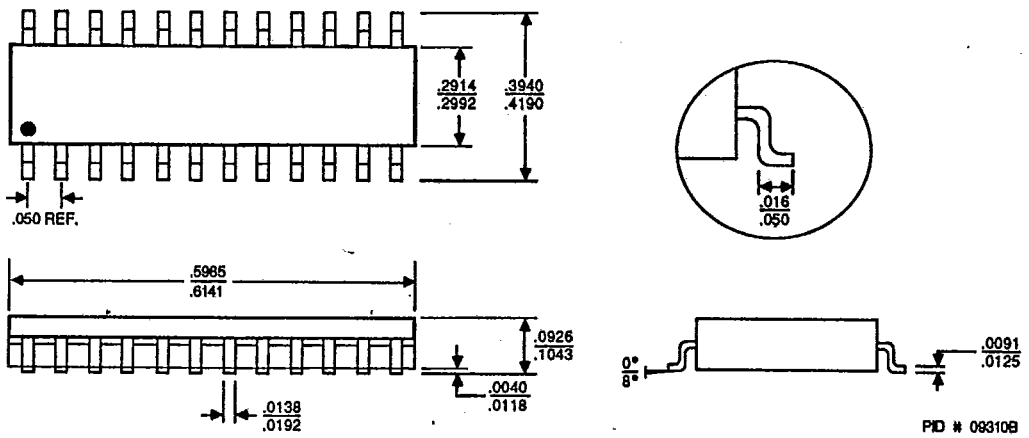


*For reference only.

PACKAGE OUTLINES (Cont'd.)

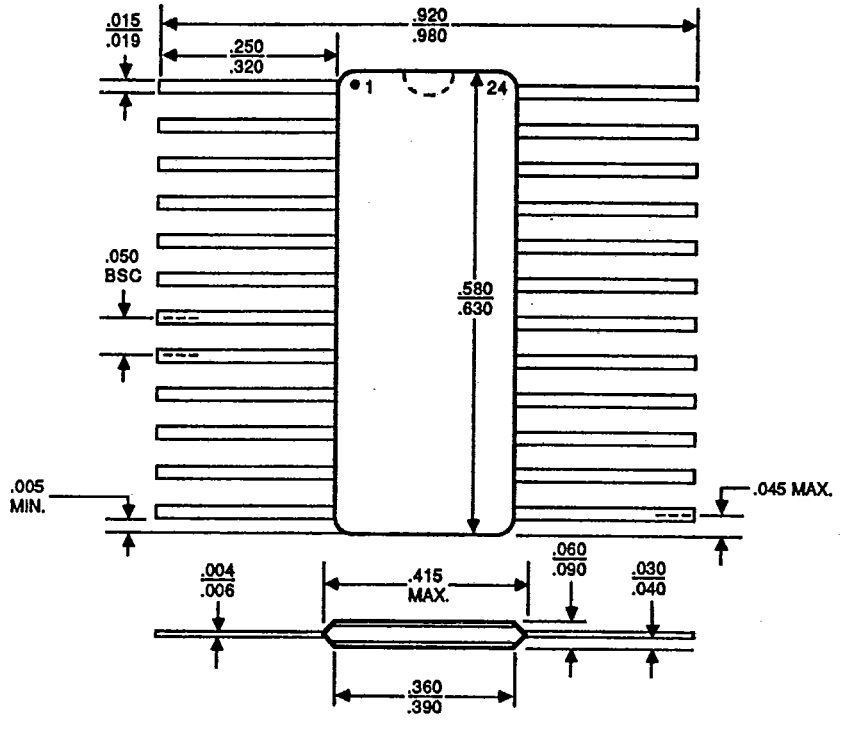
T-90-20

SO 024



PID # 09310B

CFM024

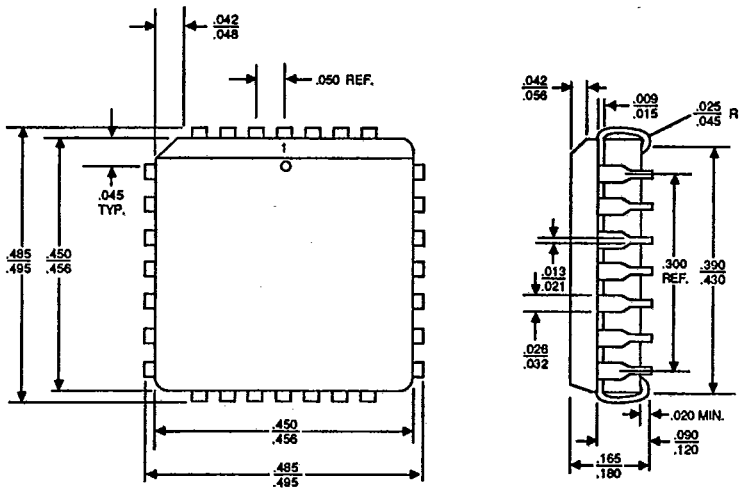


PID # 07371C

PACKAGE OUTLINES (Cont'd.)

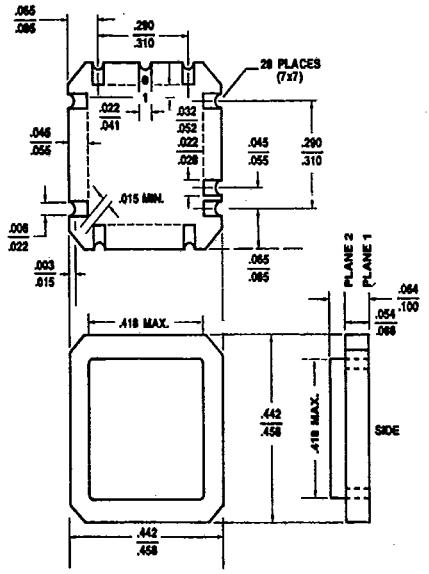
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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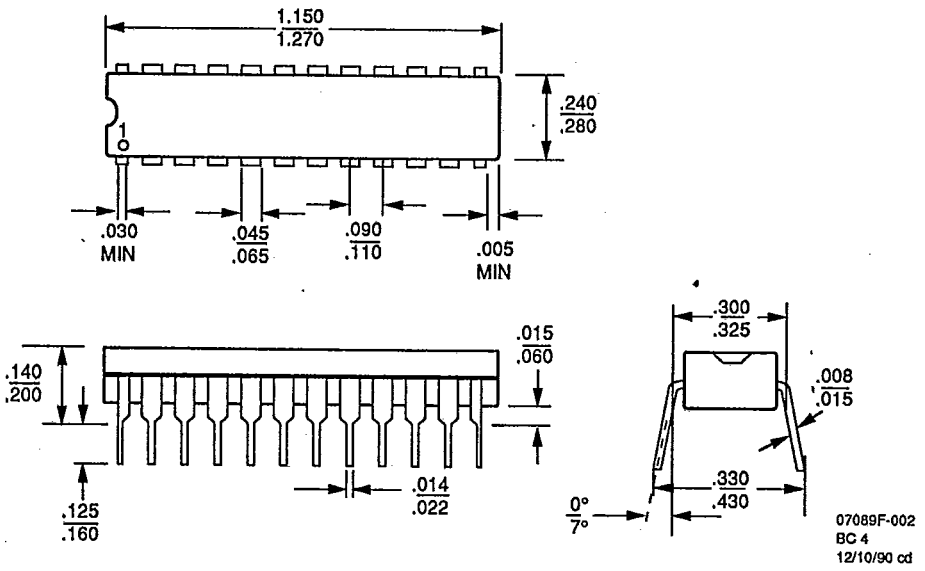
Printed in U.S.A. AIS-WCP-20M-01/88-0

T-90-20

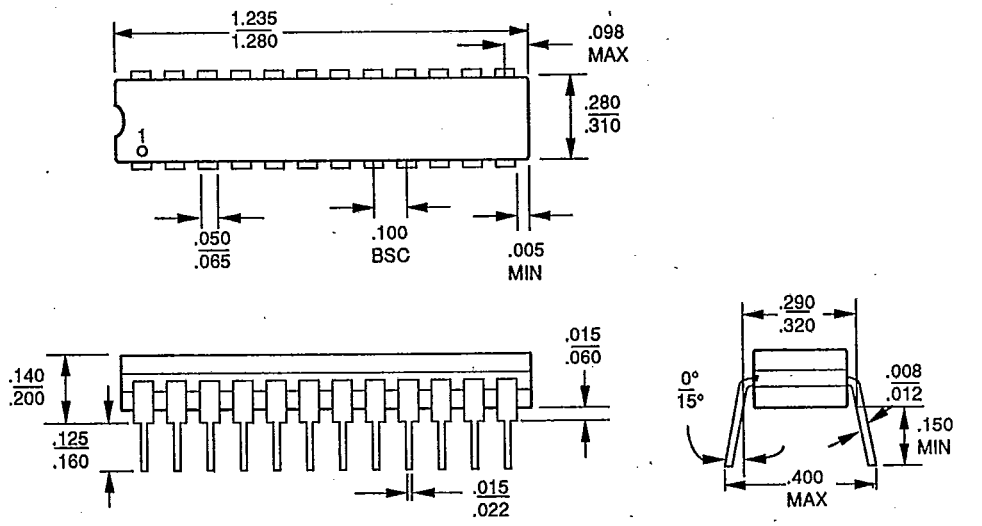
PD3024
24-Pin 300-mil Plastic SKINNYDIP



07089F-002
BC 4
12/10/90 cd

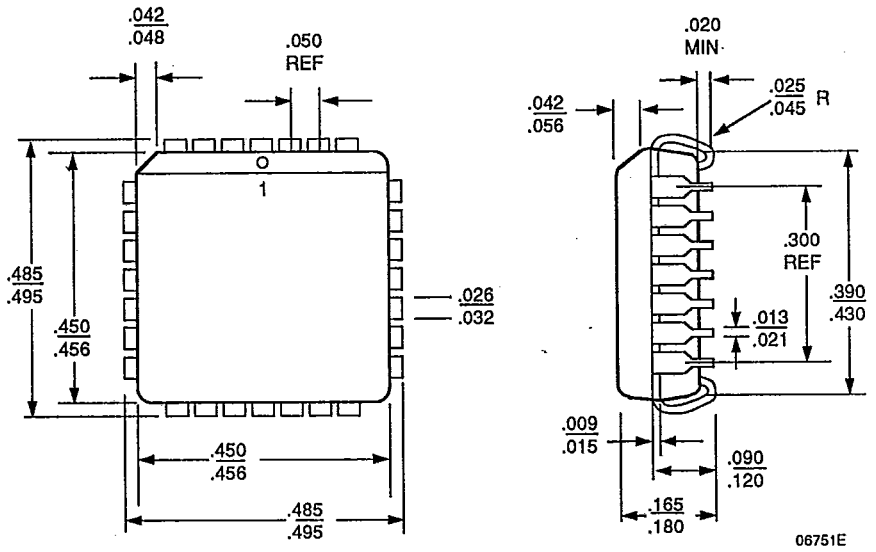
Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



06850C

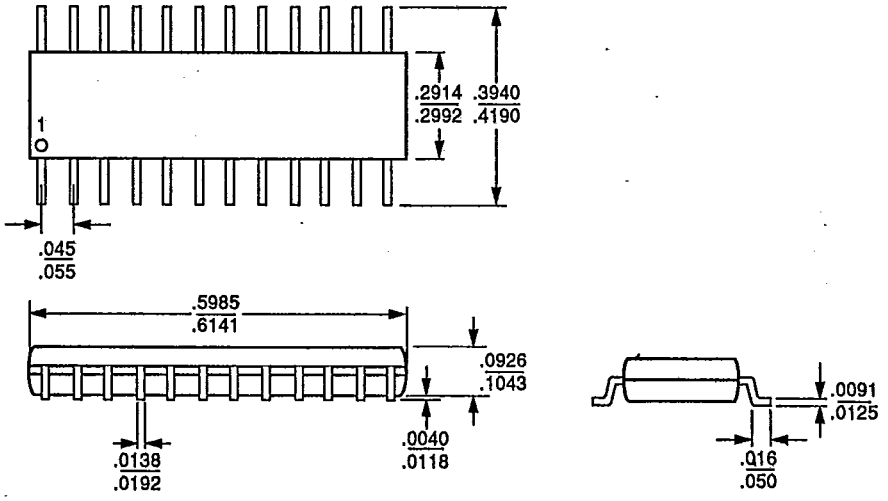
PL 028
28-Pin Plastic Leaded Chip Carrier



06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20



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