

74ACTQ153

Quiet Series Dual 4-Input Multiplexer

Features

- Outputs source/sink 24mA
- ACTQ153 has TTL-compatible inputs
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity

General Description

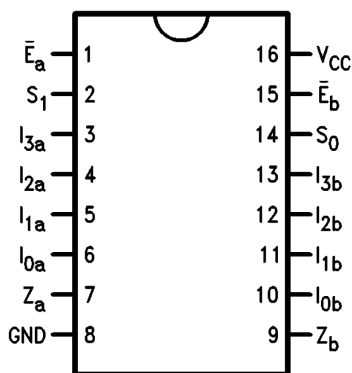
The ACTQ153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the ACTQ153 can act as a function generator and generate any two functions of three variables.

Ordering Information

Order Number	Package Number	Package Description
74ACTQ153SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

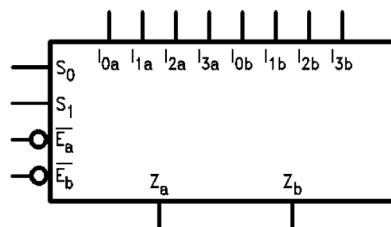
Connection Diagram



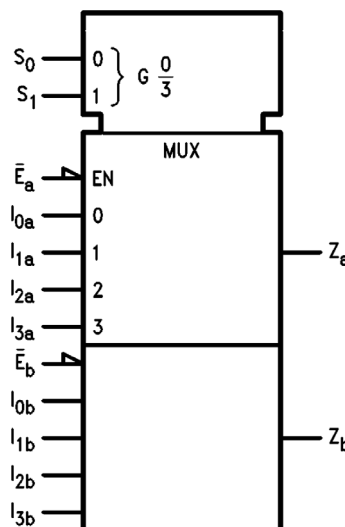
Pin Description

Pin Names	Description
I _{0a} –I _{3a}	Side A Data Inputs
I _{0b} –I _{3b}	Side B Data Inputs
S ₀ , S ₁	Common Select Inputs
$\bar{E}_a$	Side A Enable Input
$\bar{E}_b$	Side B Enable Input
Z _a	Side A Output
Z _b	Side B Output

Logic Symbols



IEEE/IEC



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Functional Description

The ACTQ153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\bar{E}_a$, $\bar{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\bar{E}_a$, $\bar{E}_b$) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW. The ACTQ153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

Truth Table

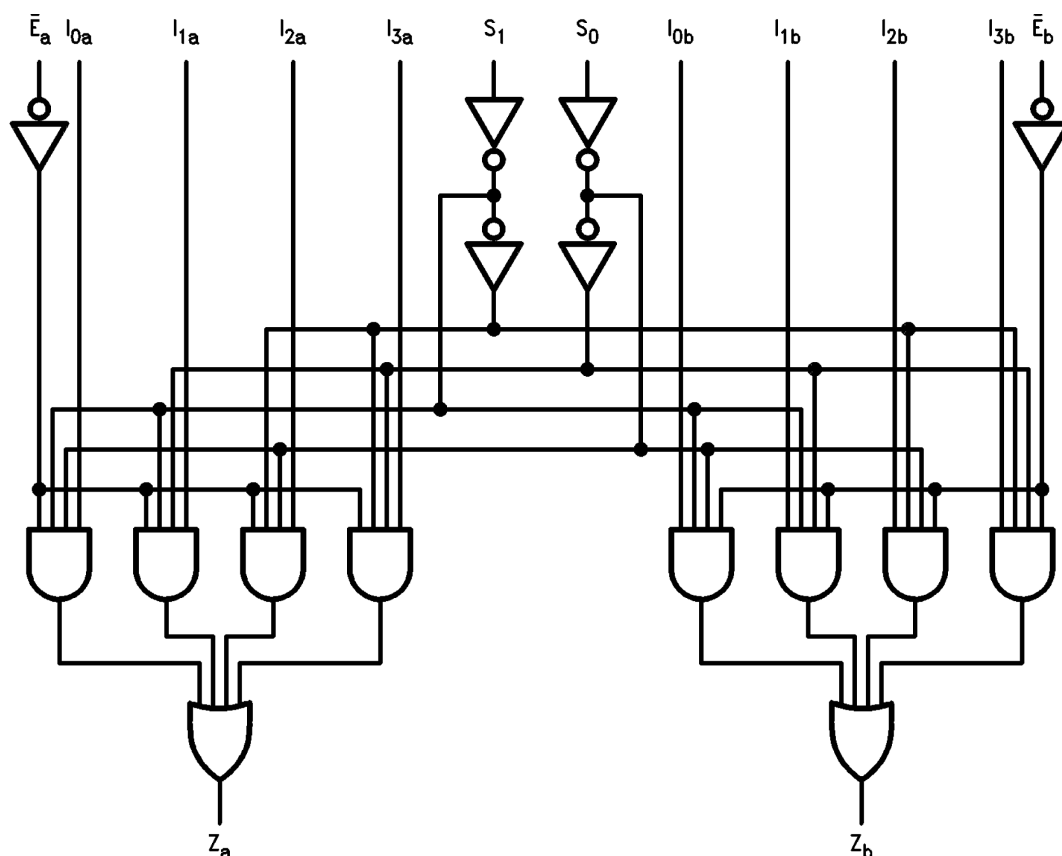
Select Inputs		Inputs (a or b)					Outputs
S_0	S_1	E	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5V to +7.0V
I_{IK}	DC Input Diode Current $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$	-20mA +20mA
V_I	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
I_{OK}	DC Output Diode Current $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$	-20mA +20mA
V_O	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
I_O	DC Output Source or Sink Current	$\pm 50mA$
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Output Pin	$\pm 50mA$
T_{STG}	Storage Temperature	-65°C to +150°C
	DC Latch-Up Source or Sink Current	$\pm 300mA$
T_J	Junction Temperature	140°C

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to 5.5V
V_I	Input Voltage	0V to V_{CC}
V_O	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate: V_{IN} from 0.8V to 2.0V, V_{CC} @ 4.5V, 5.5V	125mV/ns

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = +25°C		T _A = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V _{IL}	Maximum LOW Level Input Voltage	4.5	V _{OUT} = 0.1V or V _{CC} − 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V _{OH}	Minimum HIGH Level Output Voltage	4.5	I _{OUT} = −50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OH} = −24mA		3.86	3.76		
		5.5	I _{OH} = −24mA ⁽¹⁾		4.86	4.76		
V _{OL}	Maximum LOW Level Output Voltage	4.5	I _{OUT} = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V _{IN} = V _{IL} or V _{IH} ; I _{OL} = 24mA		0.36	0.44		
		5.5	I _{OL} = 24mA ⁽¹⁾		0.36	0.44		
I _{IN}	Maximum Input Leakage Current	5.5	V _I = V _{CC} , GND		±0.1	±1.0		μA
I _{CCT}	Maximum I _{CC} /Input	5.5	V _I = V _{CC} − 2.1V	0.6		1.5		μA
I _{OLD}	Minimum Dynamic Output Current ⁽²⁾	5.5	V _{OLD} = 1.65V Max.			75		mA
I _{OHD}		5.5	V _{OHD} = 3.85V Min.			−75		mA
I _{CC}	Maximum Quiescent Supply Current	5.5	V _{IN} = V _{CC} or GND		8.0	80.0		μA
V _{OLP}	Maximum HIGH Level Output Noise	5.0	Figures 1 & 2 ⁽³⁾⁽⁴⁾	1.1	1.5			V
V _{OLV}	Maximum LOW Level Output Noise	5.0	Figures 1 & 2 ⁽³⁾⁽⁴⁾	−0.6	−1.2			V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	⁽³⁾⁽⁵⁾	1.9	2.2			V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	⁽³⁾⁽⁵⁾	1.2	0.8			V

Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0ms, one output loaded at a time.
3. Worst case package.
4. Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One Data Input @ V_{IN} = GND.
5. Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to 5V. Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1MHz.

AC Electrical Characteristics

Symbol	Parameter	$V_{CC}(V)^{(6)}$	$T_A = +25^{\circ}C$, $C_L = 50pF$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$, $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, S_n to Z_n	5.0	3.0	7.0	11.5	2.0	13.5	ns
t_{PHL}	Propagation Delay, S_n to Z_n	5.0	3.0	7.0	11.5	2.5	13.5	ns
t_{PLH}	Propagation Delay, $\bar{E}_n$ to Z_n	5.0	2.0	6.5	10.5	2.0	12.5	ns
t_{PHL}	Propagation Delay, $\bar{E}_n$ to Z_n	5.0	3.0	6.0	9.5	2.5	11.0	ns
t_{PLH}	Propagation Delay, I_n to Z_n	5.0	2.5	5.5	9.5	2.0	11.0	ns
t_{PHL}	Propagation Delay, I_n to Z_n	5.0	2.0	5.5	9.5	2.0	11.0	ns

Note:

6. Voltage range 5.0 is $5.0V \pm 0.5V$.

Capacitance

Symbol	Parameter	Conditions	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = 5.0V$	4.5	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 5.0V$	65.0	pF

FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

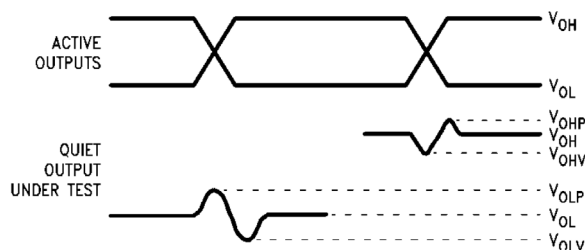
Hewlett Packard Model 8180A Word Generator

PC-163A Test Fixture

Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Notes:

7. V_{OHV} and V_{OLP} are measured with respect to ground reference.
8. Input pulses have the following characteristics:
 $f = 1\text{MHz}$, $t_r = 3\text{ns}$, $t_f = 3\text{ns}$, skew < 150ps.

Figure 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable.
- Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next decrease the input HIGH voltage level, V_{IH} , until the output begins to oscillate or steps out a min of 2ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

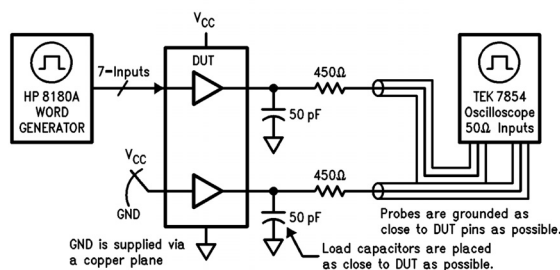
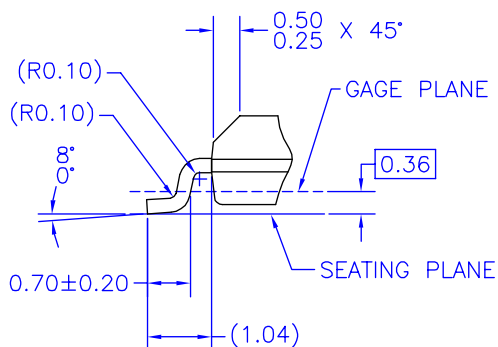
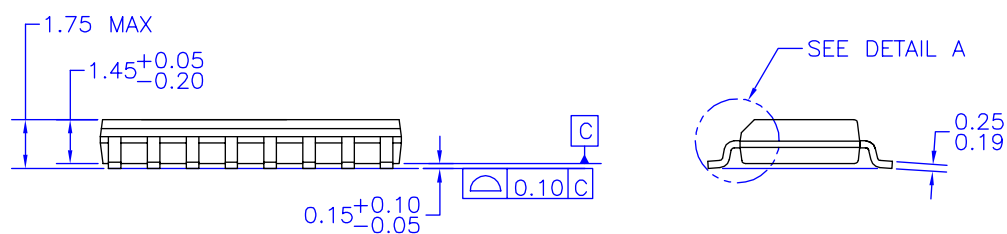
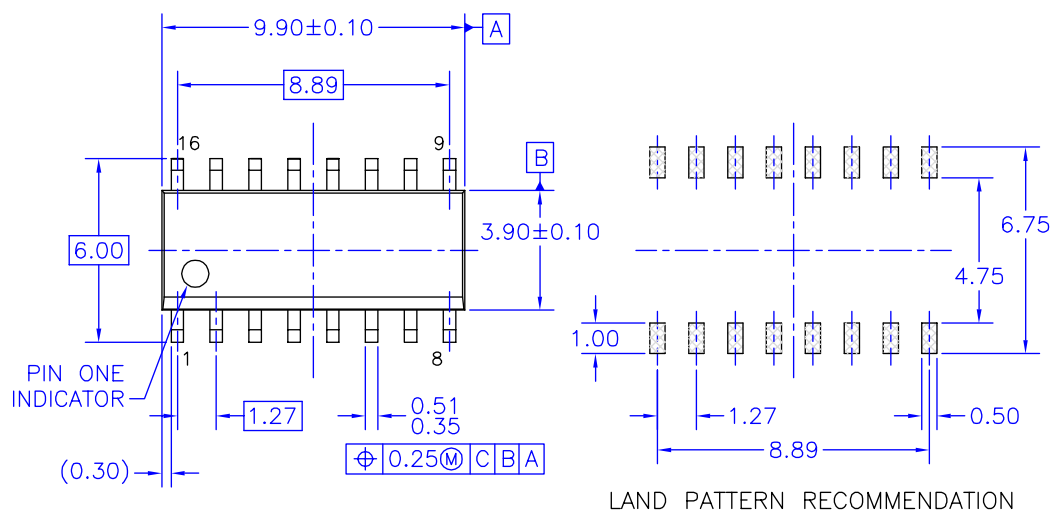


Figure 2. Simultaneous Switching Test Circuit

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.



DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AC, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MIN.
LEAD/TIN (SOLDER) ON COPPER.

M16AREVK

Figure 3. 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



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FACT [®]	PACMAN [™]	SuperSOT [™] 3	
FAST [®]	PDP-SPM [™]	SuperSOT [™] 6	
FASTr [™]	POP [™]	SuperSOT [™] 8	
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