19-2237; Rev 0; 10/01

EVALUATION KIT AVAILABLE

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

General Description

The MAX9316 is a low-skew, 1-to-5 differential driver designed for clock and data distribution. This device allows selection between two inputs: one differential and one single ended. The selected input is reproduced at five differential outputs. The differential input can be adapted to accept a single-ended input by connecting the on-chip V_{BB} supply to one input as a reference voltage.

The MAX9316 features low output-to-output skew (20ps), making it ideal for clock and data distribution across a backplane or board. For interfacing to differential HSTL and LVPECL signals, this device operates over a +3.0V to +3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal +3.3V supply. For differential LVECL operation, this device operates with a -3.0V to -3.8V supply.

The MAX9316 is offered in a space-saving 20-pin TSSOP and wide-body SO package.

Applications

Precision Clock Distribution

Low-Jitter Data Repeater

Data and Clock Driver and Buffer

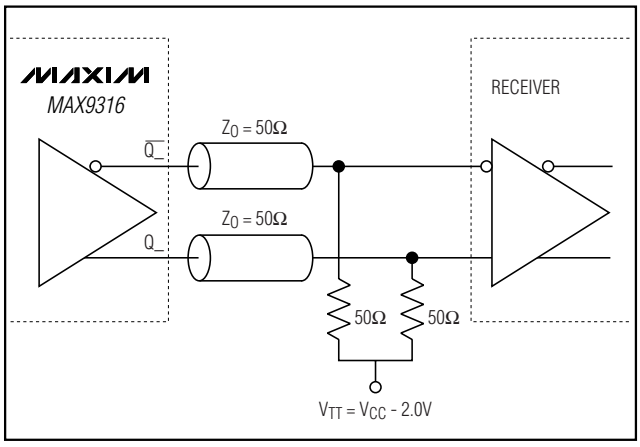
Central Office Backplane Clock Distribution

DSLAM Backplane

Base Station

ATE

Typical Application Circuit



Functional Diagram appears at end of data sheet.

Features

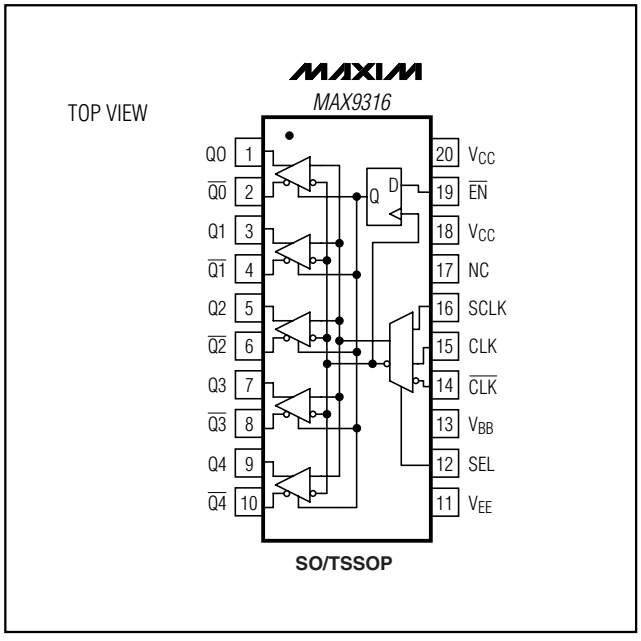
- ♦ **Guaranteed 400mV Differential Output at 1.5GHz**
- ♦ **Selectable Single-Ended or Differential Input**
- ♦ **130ps (max) Part-to-Part Skew at +25°C**
- ♦ **20ps Output-to-Output Skew**
- ♦ **365ps Propagation Delay**
- ♦ **Synchronous Output Enable/Disable**
- ♦ **On-Chip Reference for Single-Ended Inputs**
- ♦ **Input Biased to Low when Open**
- ♦ **Pin Compatible with MC100LVEL14**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9316EUP	-40°C to +85°C	20 TSSOP
MAX9316EWP*	-40°C to +85°C	20 Wide SO

**Future product—contact factory for availability.*

Pin Configuration



1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE}.....4.1V
Inputs (CLK, $\overline{CLK}$, SCLK, SEL, $\overline{EN}$)
to V_{EE}.....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
CLK to $\overline{CLK}$.....±3.0V
Continuous Output Current.....50mA
Surge Output Current.....100mA
V_{BB} Sink/Source Current.....±0.65mA
Continuous Power Dissipation (T_A = +70°C)
Single-Layer PC Board
20-Pin TSSOP (derate 7.69mW/°C above +70°C).....615mW
20-Pin Wide SO (derate 10mW/°C above +70°C).....800mW
Multilayer PC Board
20-Pin TSSOP (derate 10.9mW/°C above +70°C).....879mW
Junction-to-Ambient Thermal Resistance in Still Air
Single-Layer PC Board
20-Pin TSSOP.....+130°C/W
20-Pin Wide SO…….....+100°C/W
Multilayer PC Board
20-Pin TSSOP.....+91°C/W
Junction-to-Ambient Thermal Resistance with
500LFPM Airflow
Single-Layer PC Board
20-Pin TSSOP.....+96°C/W
20-Pin Wide SO…….....+58°C/W
Junction-to-Case Thermal Resistance
20-Pin TSSOP.....+20°C/W
20-Pin Wide SO…….....+20°C/W
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65°C to +150°C
ESD Protection
Human Body Model (Inputs and Outputs).....2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, SEL = high or low, $\overline{EN}$ = low, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SINGLE-ENDED INPUTS (SCLK, SEL, $\overline{EN}$)												
Input High Voltage	V_{IH}		V_{CC} - 1.145		V_{CC}	V_{CC} - 1.145		V_{CC}	V_{CC} - 1.145		V_{CC}	V
Input Low Voltage	V_{IL}		V_{EE}		V_{CC} - 1.495	V_{EE}		V_{CC} - 1.495	V_{EE}		V_{CC} - 1.495	V
Input Current	I_{IN}	$V_{IL(MIN)}$, $V_{IH(MAX)}$	-10		150	-10		150	-10		150	µA
DIFFERENTIAL INPUTS (CLK_, $\overline{CLK\_}$)												
Single-Ended Input High Voltage	V_{IH}	$\overline{CLK\_}$ connected to V_{BB}, Figure 1	V_{CC} - 1.145		V_{CC}	V_{CC} - 1.145		V_{CC}	V_{CC} - 1.145		V_{CC}	V
Single-Ended Input Low Voltage	V_{IL}	$\overline{CLK\_}$ connected to V_{BB}, Figure 1	V_{EE}		V_{CC} - 1.495	V_{EE}		V_{CC} - 1.495	V_{EE}		V_{CC} - 1.495	V
High Voltage of Differential Input	V_{IHD}		V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Low Voltage of Differential Input	V_{ILD}		V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	VEE		V_{CC} - 0.095	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = +3.0V to +3.8V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, SEL = high or low, $\overline{EN}$ = low, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Voltage	V_{IHD} - V_{ILD}		0.095		3.0	0.095		3.0	0.095		3.0	V
Input Current	I_{IN}	V_{IH}, V_{IL}, V_{IHD}, V_{ILD}	-150		150	-150		150	-150		150	µA
OUTPUTS (Q_, $\overline{Q\_}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 1	V_{CC} - 1.085		V_{CC} - 0.865	V_{CC} - 1.025		V_{CC} - 0.865	V_{CC} - 1.025		V_{CC} - 0.865	V
Single-Ended Output Low Voltage	V_{OL}	Figure 1	V_{CC} - 1.860		V_{CC} - 1.555	V_{CC} - 1.840		V_{CC} - 1.620	V_{CC} - 1.810		V_{CC} - 1.620	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1	550		910	550		910	550		910	mV
REFERENCE (V_{BB})												
Reference Voltage Output (Note 4)	V_{BB}	I_{BB} = ±0.5mA	V_{CC} - 1.40		V_{CC} - 1.24	V_{CC} - 1.40		V_{CC} - 1.24	V_{CC} - 1.40		V_{CC} - 1.24	V
SUPPLY												
Supply Current (Note 5)	I_{EE}			30	40		32	40		34	42	mA

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +3.0V to +3.8V, outputs are loaded with 50Ω ±1% to V_{CC} - 2V, input frequency = 1.5GHz, input transition time = 125ps (20% to 80%), SEL = high or low, $\overline{EN}$ = low, V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.15V, V_{IHD} - V_{ILD} = 0.15V to 3V, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V.) (Notes 1, 6)

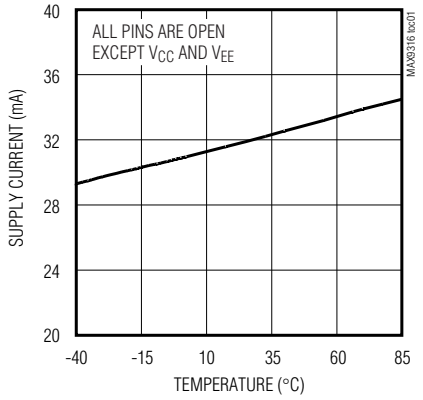
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CLK to Q_ Delay (Differential)	t_{PLHD1}, t_{PHLD1}	Figure 2	290		400	310		440	300		520	ps
SCLK to Q_ Delay	t_{PLHD3}, t_{PHLD3}	V_{IL} = V_{CC} - 1.55V, V_{IH} = V_{CC} - 1.09V, Figure 3	290		400	310		440	300		520	ps
Output-to-Output Skew (Note 7)	t_{SKOO}			5	30		20	40		20	50	ps
Part-to-Part Skew (Note 8)	t_{SKPP}				110			130			220	ps
Added Random Jitter (Note 9)	t_{RJ}	f_{IN} = 1.5GHz clock		0.8	1.2		0.8	1.2		0.8	1.2	ps (RMS)
Added Deterministic Jitter (Note 9)	t_{DJ}	1.5Gbps $2E^{23}$-1 PRBS pattern		50	70		50	70		50	70	ps (p-p)
Switching Frequency	f_{MAX}	(V_{OH} - V_{OL}) ≥ 400mV, Figure 2	1.5			1.5			1.5			GHz
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 2	80		120	90		130	90		145	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 4: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.
Note 5: All pins are open except V_{CC} and V_{EE}.
Note 6: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 7: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 8: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 9: Device jitter added to a jitter-free input signal.

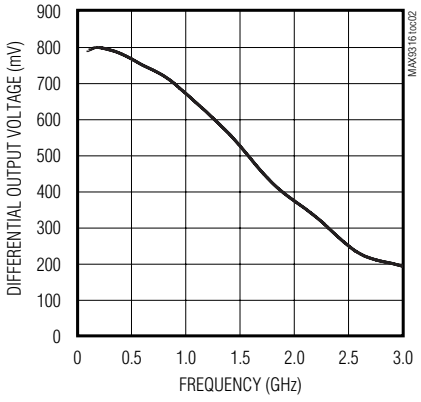
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.15V, input transition time = 125ps (20% to 80%), f_{IN} = 1.5GHz, outputs loaded with 50Ω to (V_{CC} - 2V), T_A = +25°C, unless otherwise noted.)

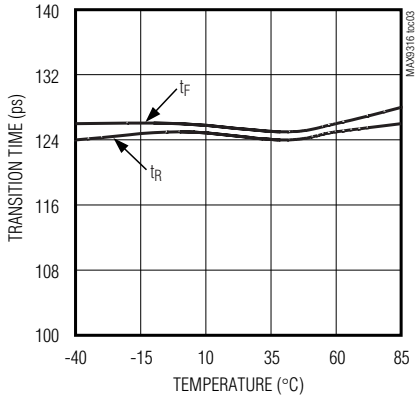
SUPPLY CURRENT vs. TEMPERATURE



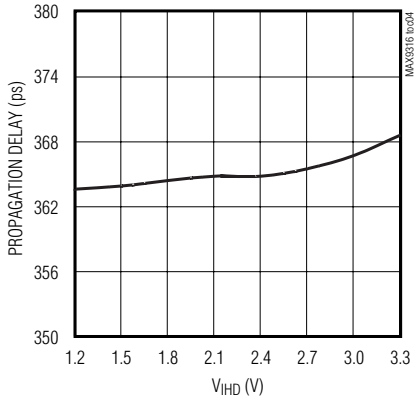
DIFFERENTIAL OUTPUT VOLTAGE (V_{OH} - V_{OL}) vs. FREQUENCY



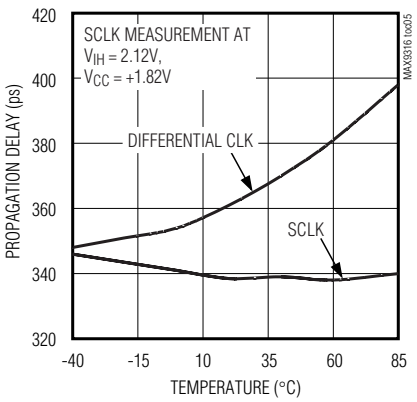
TRANSITION TIME vs. TEMPERATURE



PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Pin Description

PIN	NAME	FUNCTION
1	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
2	$\overline{Q0}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
3	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
4	$\overline{Q1}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
5	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
6	$\overline{Q2}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
7	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
8	$\overline{Q3}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
9	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
10	$\overline{Q4}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to (V_{CC} - 2V).
11	V_{EE}	Negative Supply Voltage
12	SEL	Clock Select Input (Single Ended). Drive low to select the CLK, $\overline{CLK}$ input. Drive high to select the SCLK input. The SEL threshold is equal to V_{BB}. Internal 60kΩ pulldown to V_{EE}.
13	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass with a 0.01µF ceramic capacitor to V_{CC}; otherwise, leave it unconnected.
14	$\overline{CLK}$	Inverting Differential Clock Input. Internal 75kΩ pullup to V_{CC} and 75kΩ pulldown to V_{EE}.
15	CLK	Noninverting Differential Clock Input. Internal 75kΩ pulldown to V_{EE}.
16	SCLK	Single-Ended Clock Input. Internal 75kΩ pulldown to V_{EE}.
17	NC	Not Internally Connected. Solder to PC board for package thermal dissipation.
18, 20	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
19	$\overline{EN}$	Output Enable Input. Outputs are synchronously enabled on the falling edge of the clock input when $\overline{EN}$ is low. Outputs are synchronously set to low on the falling edge of the clock input when $\overline{EN}$ is high. Internal 60kΩ pulldown to V_{EE}.

Detailed Description

The MAX9316 is a low-skew, 1-to-5 differential driver designed for clock or data distribution. A 2-to-1 MUX selects one of the two clock inputs, CLK, $\overline{CLK}$ and SCLK. The CLK and $\overline{CLK}$ input is differential while the SCLK is single ended. The MUX is switched by the single-ended SEL input. A logic low selects the CLK input and a logic high selects the SCLK input. The SEL logic threshold is set by the internal voltage reference V_{BB}. SEL input can be driven by V_{CC} and V_{EE} or by a single-ended LVPECL/LVECL signal. The selected input is reproduced at five differential outputs, Q0 to Q4.

Synchronous Enable

The MAX9316 is synchronously enabled and disabled with outputs in the low state to eliminate shortened clock pulses. $\overline{EN}$ is connected to the input of an edge-triggered D flip-flop. After power-up, drive $\overline{EN}$ low and toggle the selected clock input to enable the outputs. The outputs are enabled on the falling edge of the selected clock input after $\overline{EN}$ goes low. The outputs are disabled to a low state on the falling edge of the selected clock input after $\overline{EN}$ goes high. The threshold for $\overline{EN}$ is equal to V_{BB}.

Supply

For interfacing to differential HSTL and LVPECL signals, the V_{CC} range is from +3.0 to +3.8V (with V_{EE} ground-

ed), allowing high-performance clock or data distribution in systems with a nominal +3.3V supply. For interfacing to differential LVECL, the V_{EE} range is -3.0V to -3.8V (with V_{CC} grounded). Output levels are referenced to V_{CC} and are considered LVPECL or LVECL, depending on the level of the V_{CC} supply. With V_{CC} connected to a positive supply and V_{EE} connected to ground, the outputs are LVPECL. The outputs are LVECL when V_{CC} is connected to ground and V_{EE} is connected to a negative supply.

Input Bias Resistors

When the inputs are open, the internal bias resistors set the inputs to low state. The inverting input ($\overline{CLK}$) is biased with a 75kΩ pullup to V_{CC} and a 75kΩ pulldown to V_{EE}. The noninverting inputs (CLK) and the single-ended input (SCLK) are each biased with a 75kΩ pulldown to V_{EE}. The single-ended $\overline{EN}$ and SEL inputs are each biased with a 60kΩ pulldown to V_{EE}.

Differential Clock Input Limits

The maximum magnitude of the differential signal applied to the differential clock input is 3.0V. This limit also applies to the difference between any reference voltage input and a single-ended input. Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

Single-Ended Clock Input and V_{BB}

The differential clock input can be configured to accept a single-ended input. This is accomplished by connecting the on-chip reference voltage, V_{BB}, to the inverting or noninverting input of the differential input as a reference. For example, the differential CLK, $\overline{CLK}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{CLK}$ and connecting the single-ended input signal to CLK. Similarly, an inverting configuration is obtained by connecting V_{BB} to CLK and connecting the single-ended input to $\overline{CLK}$. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} and V_{EE} or with a single-ended LVPECL/LVECL signal. Note that the single-ended input must be least V_{BB} ±95mV or a differential input of at least 95mV to switch the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, leave it open. The V_{BB} reference can source or sink 0.5mA. Use V_{BB} only for an input that is on the same device as the V_{BB} reference.

Applications Information

Supply Bypassing

Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible, with the 0.01µF capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC} (if the V_{BB} reference is not used, it can be left open).

Controlled-Impedance Traces

Input and output trace characteristics affect the performance of the MAX9316. Connect input and output signals with 50Ω characteristic impedance traces. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through cables and connectors. Reduce skew within a differential pair by matching the electrical length of the traces.

Output Termination

Terminate outputs with 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q0 is used as a single-ended output, terminate both Q0 and $\overline{Q0}$.

Chip Information

TRANSISTOR COUNT: 616

PROCESS: Bipolar

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

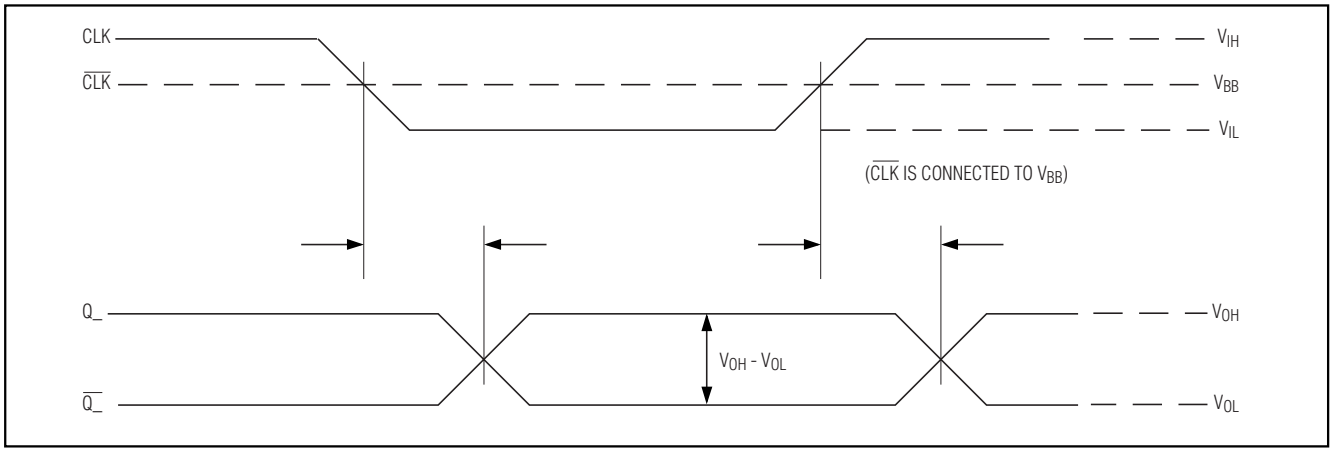


Figure 1. MAX9316 Switching Characteristics with Single-Ended Input

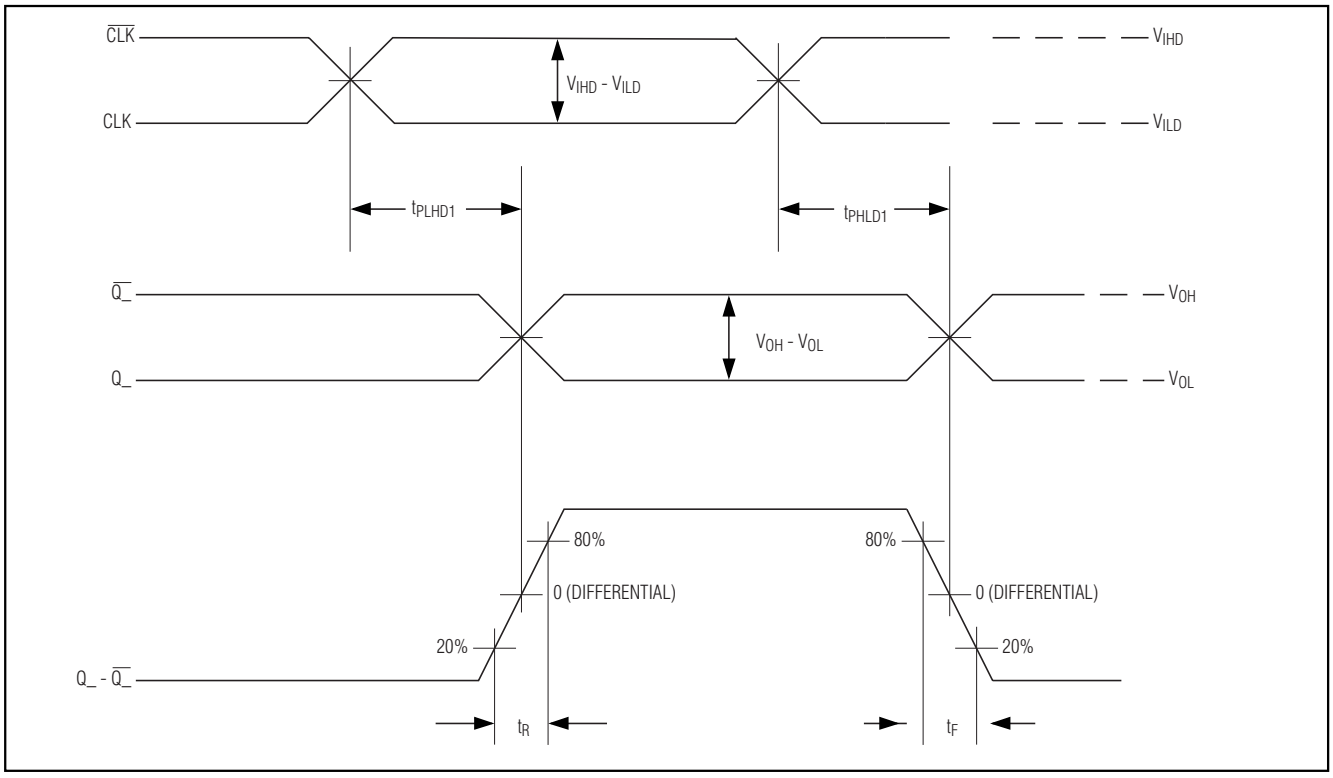


Figure 2. MAX9316 Timing Diagram

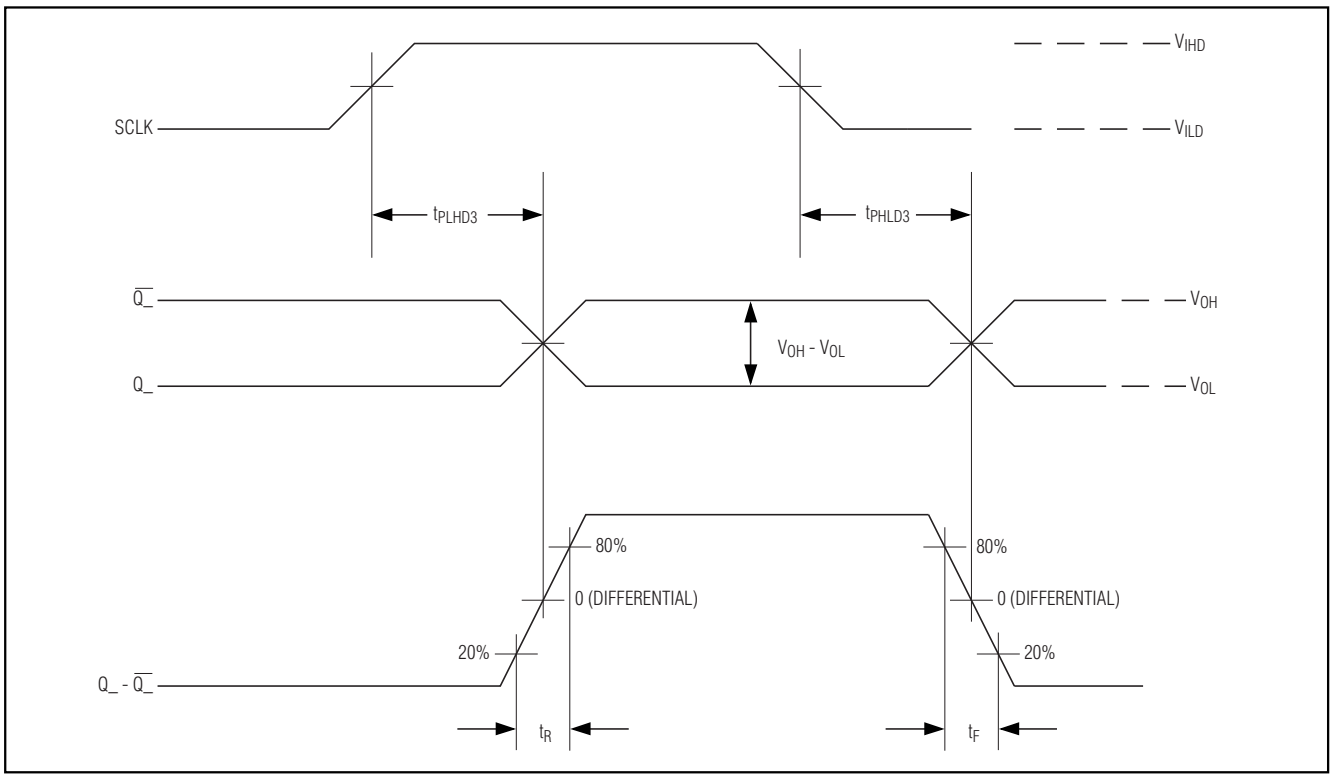


Figure 3. MAX9316 Timing Diagram for SCLK

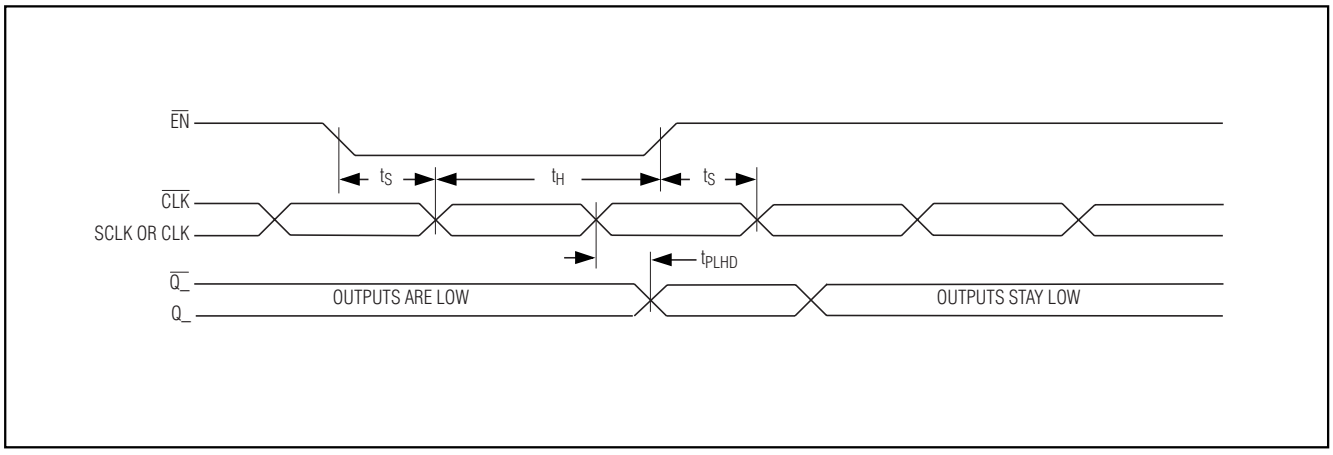
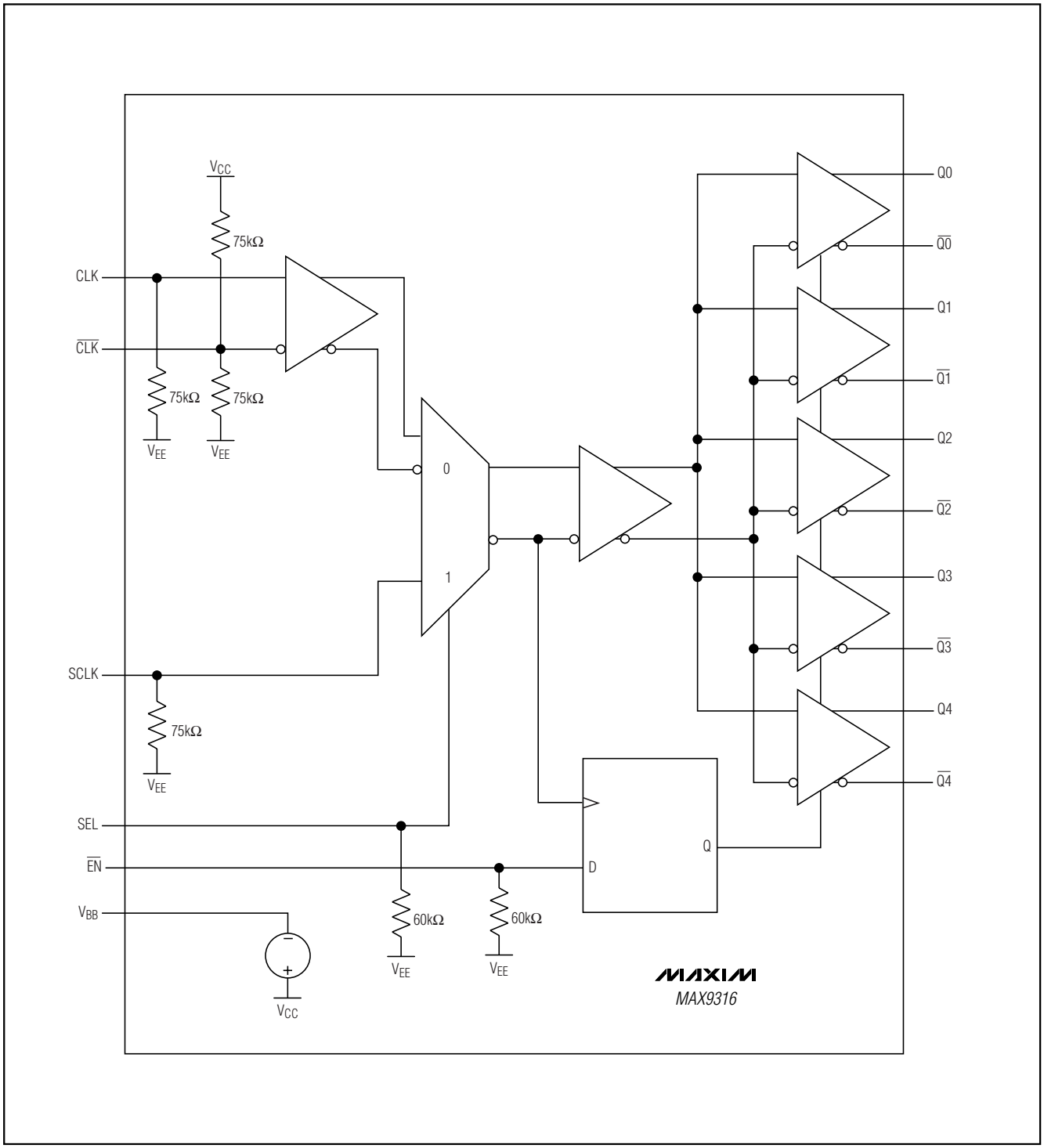


Figure 4. MAX9316 $\overline{EN}$ Timing Diagram

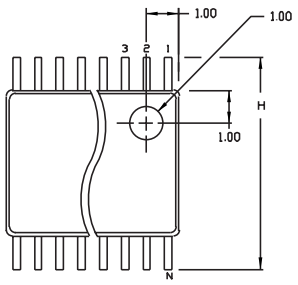
1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Functional Diagram

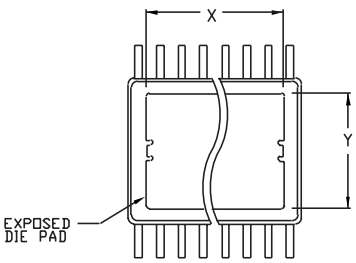


Package Information

TSSOP.EPS

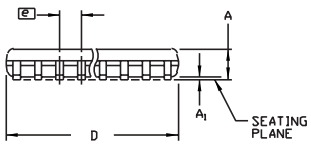


TOP VIEW

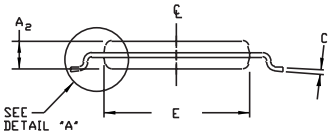


BOTTOM VIEW

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

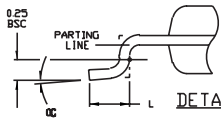


SIDE VIEW

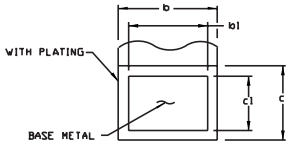


END VIEW

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222



DETAIL 'A'



LEAD TIP DETAIL

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

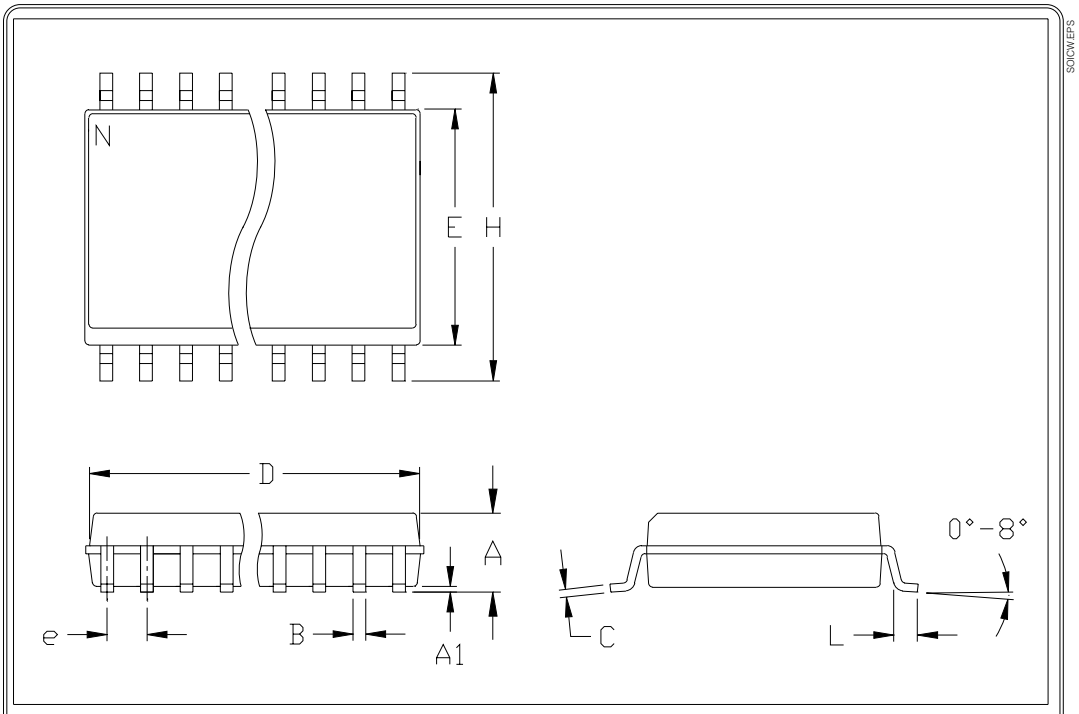
MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	C	1/1

1:5 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .300"
TITLE

1/1

21-0042 A
DOCUMENT CONTROL NUMBER REV