

FEATURES

0.5 Ω typical on resistance
0.8 Ω maximum on resistance at 125°C
1.65 V to 3.6 V operation
Operating temperature range: -40°C to +125°C
Guaranteed leakage specifications up to 125°C
High current carrying capability: 300 mA continuous
Rail-to-rail switching operation
Fast switching times: <20 ns
Typical power consumption: <0.1 μ W

APPLICATIONS

Cellular phones
 PDAs
 MP3 players
 Power routing
 Battery-powered systems
 PCMCIA cards
 Modems
 Audio and video signal routing
 Communication systems

GENERAL DESCRIPTION

The **ADG836L** is a low voltage CMOS device containing two independently selectable single-pole, double-throw (SPDT) switches. This device offers ultralow on resistance of less than 0.8 Ω over the full temperature range. The **ADG836L** is fully specified for 3.3 V, 2.5 V, and 1.8 V supply operation.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The **ADG836L** exhibits break-before-make switching action.

The **ADG836L** is available in a 10-lead package.

FUNCTIONAL BLOCK DIAGRAM

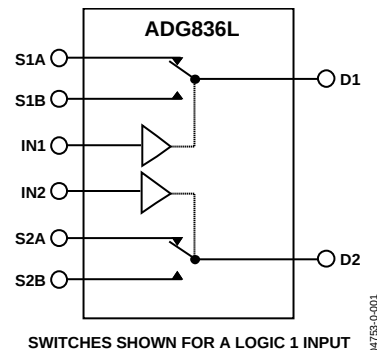


Figure 1.

PRODUCT HIGHLIGHTS

1. Less than 0.8 Ω over full temperature range of -40°C to +125°C.
2. Single 1.65 V to 3.6 V operation.
3. Compatible with 1.8 V CMOS logic.
4. High current handling capability (300 mA continuous current at 3.3 V).
5. Low THD + N (0.02% typical).
6. Small 10-lead MSOP package.

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REVISION HISTORY

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Changes to Table 1	3	Added Terminology Section.....	13
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6/2016—Rev. A to Rev. B		5/2004—Rev. 0 to Rev. A	
Updated Format	Universal	Updated Ordering Guide	14
Change to On Resistance Match Between Channels (ΔR_{ON})		4/2004—Revision 0: Initial Version	
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SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted. Temperature range for Y version is $-40^{\circ}\text{C to }+125^{\circ}\text{C}$.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	$V_{DD} = 2.7\text{ V}$
On Resistance (R_{ON})	0.5			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$
	0.75	0.85	0.9	Ω max	See Figure 18
On Resistance Match Between Channels (ΔR_{ON})	0.04	0.075	0.08	Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0.65\text{ V}$, $I_S = 10\text{ mA}$
	0.095	0.095	0.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.1			Ω typ	$V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$
	0.18	0.18	0.19	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$
	± 1	± 10	± 100	nA max	See Figure 19
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = 0.6\text{ V}$ or 3.3 V (see Figure 20)
	± 1	± 15	± 120	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	21			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	26	28	29	ns max	$V_S = 1.5\text{ V}/0\text{ V}$ (see Figure 21)
t_{OFF}	4			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
	7	8	9	ns max	$V_S = 1.5\text{ V}$ (see Figure 21)
Break-Before-Make Time Delay (t_{BBM})	17			ns typ	$R_L = 50\ \Omega$, $C_L = 35\text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5\text{ V}$ (see Figure 22)
Charge Injection	40			pC typ	$V_S = 1.5\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$ (see Figure 23)
Off Isolation	−67			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$ (see Figure 24)
Channel-to-Channel Crosstalk	−90			dB typ	S1A to S2A/S1B to S2B (see Figure 27), $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$
	−67			dB typ	S1A to S1B/S2A to S2B (see Figure 26), $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 100\text{ kHz}$
Total Harmonic Distortion (THD + N)	0.02			%	$R_L = 32\ \Omega$, $f = 20\text{ Hz to }20\text{ kHz}$, $V_S = 2\text{ V p-p}$
Insertion Loss	−0.05			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ (see Figure 25)
−3 dB Bandwidth	57			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$ (see Figure 25)
C_S (Off)	25			pF typ	
C_D , C_S (On)	75			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V
		1	4	μA max	

¹ Guaranteed by design, not subject to production test.

$V_{DD} = 2.5 \text{ V} \pm 0.2 \text{ V}$, $GND = 0 \text{ V}$, unless otherwise noted. Temperature range for Y version is -40°C to $+125^{\circ}\text{C}$.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.65			Ω typ	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$
	0.84	0.92	1.0	Ω max	See Figure 18
On Resistance Match Between Channels (ΔR_{ON})	0.04			Ω typ	$V_{DD} = 2.3 \text{ V}$, $V_S = 0.7 \text{ V}$, $I_S = 10 \text{ mA}$
	0.1	0.1	0.105	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.16			Ω typ	$V_{DD} = 2.3 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$
	0.25	0.25	0.26	Ω max	
LEAKAGE CURRENTS					$V_{DD} = 2.7 \text{ V}$
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_S = 0.6 \text{ V}/2.4 \text{ V}$, $V_D = 2.4 \text{ V}/0.6 \text{ V}$
	± 0.4	± 4	± 45	nA max	See Figure 19
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = 0.6 \text{ V}$ or 2.4 V (see Figure 20)
	± 0.6	± 12	± 90	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			1.7	V min	
Input Low Voltage, V_{INL}			0.7	V max	
Input Current					
I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS ¹					
t_{ON}	23			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	29	30	31	ns max	$V_S = 1.5 \text{ V}/0 \text{ V}$ (see Figure 21)
t_{OFF}	5			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	7	8	9	ns max	$V_S = 1.5 \text{ V}$ (see Figure 21)
Break-Before-Make Time Delay (t_{BBM})	17			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1.5 \text{ V}$ (see Figure 22)
Charge Injection	30			pC typ	$V_S = 1.25 \text{ V}$, $R_S = 0 \Omega$, $C_L = 1 \text{ nF}$ (see Figure 23)
Off Isolation	−67			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$ (see Figure 24)
Channel-to-Channel Crosstalk	−90			dB typ	S1A to S2A/S1B to S2B; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$ (see Figure 27)
	−67			dB typ	S1A to S1B/S2A to S2B; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$ (see Figure 26)
Total Harmonic Distortion (THD + N)	0.022			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 1.5 \text{ V p-p}$
Insertion Loss	−0.06			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ (see Figure 25)
−3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ (see Figure 25)
C_S (Off)	25			pF typ	
C_D , C_S (On)	75			pF typ	
POWER REQUIREMENTS					$V_{DD} = 2.7 \text{ V}$
I_{DD}	0.003			μA typ	Digital inputs = 0 V or 2.7 V
		1	4	μA max	

¹ Guaranteed by design, not subject to production test.

$V_{DD} = 1.65 \text{ V} \pm 1.95 \text{ V}$, GND = 0 V, unless otherwise noted. Temperature range for Y version is -40°C to $+125^{\circ}\text{C}$.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	1			Ω typ	$V_{DD} = 1.8 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$ See Figure 18
	1.6	2.4	2.4	Ω max	
	2.7	4.2	4.2	Ω typ	$V_{DD} = 1.65 \text{ V}$, $V_S = 0 \text{ V}$ to V_{DD} , $I_S = 10 \text{ mA}$
On Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	$V_{DD} = 1.65 \text{ V}$, $V_S = 0.7 \text{ V}$, $I_S = 10 \text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage I_S (Off)	± 0.2			nA typ	$V_{DD} = 1.95 \text{ V}$ $V_S = 0.6 \text{ V}/1.65 \text{ V}$, $V_D = 1.65 \text{ V}/0.6 \text{ V}$
	± 0.4	± 4	± 25	nA max	See Figure 19
Channel On Leakage I_D , I_S (On)	± 0.2			nA typ	$V_S = V_D = 0.6 \text{ V}$ or 1.65 V (see Figure 20)
	± 0.6	± 10	± 75	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			$0.65 V_{DD}$	V min	
Input Low Voltage, V_{INL}			$0.35 V_{DD}$	V max	
Input Current I_{INL} or I_{INH}	0.005			μA typ	$V_{IN} = V_{INL}$ or V_{INH}
			± 0.1	μA max	
C_{IN} , Digital Input Capacitance	4			pF typ	
DYNAMIC CHARACTERISTICS¹					
t_{ON}	28			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	37	38	39	ns max	$V_S = 1.5 \Omega/0 \text{ V}$ (see Figure 21)
t_{OFF}	7			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
	9	10	11	ns max	$V_S = 1.5 \text{ V}$ (see Figure 21)
Break-before-Make Time Delay (t_{BBM})	21			ns typ	$R_L = 50 \Omega$, $C_L = 35 \text{ pF}$
			5	ns min	$V_{S1} = V_{S2} = 1 \text{ V}$ (see Figure 22)
Charge Injection	20			pC typ	$V_S = 1 \text{ V}$, $R_S = 0 \text{ V}$, $C_L = 1 \text{ nF}$ (see Figure 23)
Off Isolation	−67			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$, (see Figure 24)
Channel-to-Channel Crosstalk	−90			dB typ	S1A to S2A/S1B to S2B; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$ (see Figure 27)
	−67			dB typ	S1A to S1B/S2A to S2B; $R_L = 50 \Omega$, $C_L = 5 \text{ pF}$, $f = 100 \text{ kHz}$ (see Figure 26)
Total Harmonic Distortion (THD + N)	0.14			%	$R_L = 32 \Omega$, $f = 20 \text{ Hz}$ to 20 kHz , $V_S = 1.2 \text{ V p-p}$
Insertion Loss	−0.08			dB typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ (see Figure 25)
−3 dB Bandwidth	57			MHz typ	$R_L = 50 \Omega$, $C_L = 5 \text{ pF}$ (see Figure 25)
C_S (OFF)	25			pF typ	
C_D , C_S (On)	75			pF typ	
POWER REQUIREMENTS					
I_{DD}	0.003			μA typ	$V_{DD} = 1.95 \text{ V}$ Digital inputs = 0 V or 1.95 V
		1.0	4	μA max	

¹ Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	$-0.3\text{ V to }+4.6\text{ V}$
Analog Inputs ¹	$-0.3\text{ V to }V_{DD} + 0.3\text{ V}$
Digital Inputs ²	$-0.3\text{ V to }4.6\text{ V or }10\text{ mA,}$ whichever occurs first
Peak Current, S or D	
3.3 V Operation	500 mA
2.5 V Operation	460 mA
1.8 V Operation	420 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sxx or Dx	
3.3 V Operation	300 mA
2.5 V Operation	275 mA
1.8 V Operation	250 mA
Operating Temperature Range	$-40^\circ\text{C to }+125^\circ\text{C}$
Storage Temperature Range	$-65^\circ\text{C to }+150^\circ\text{C}$
Junction Temperature	150°C
MSOP Package	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
IR Reflow, Peak Temperature <20 sec	235°C

¹ Overvoltages at INx, Sxx, or Dx are clamped by internal diodes. Current must be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

TRUTH TABLE

Table 5.

Logic	Switch A	Switch B
0	Off	On
1	On	Off

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

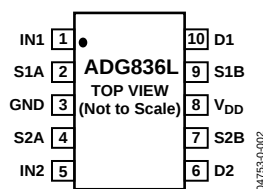
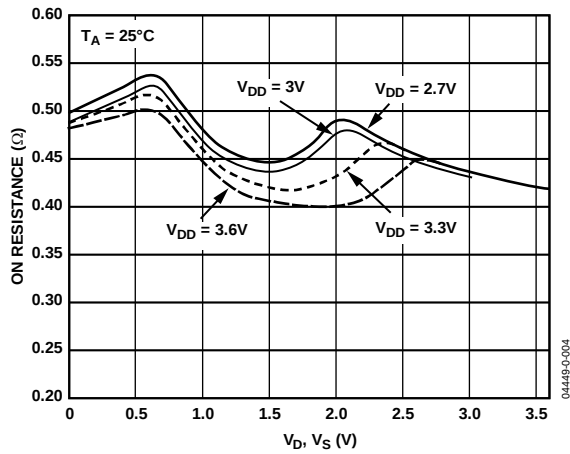
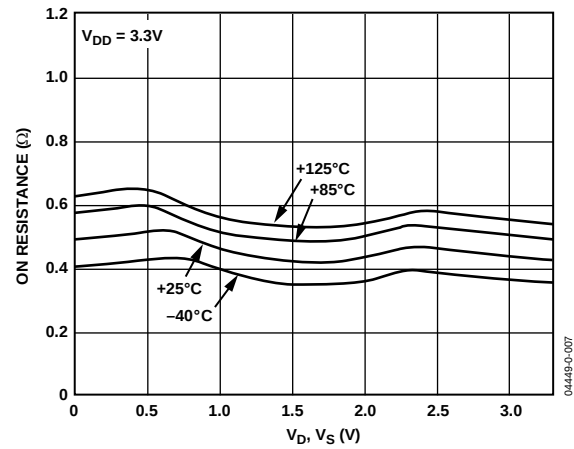
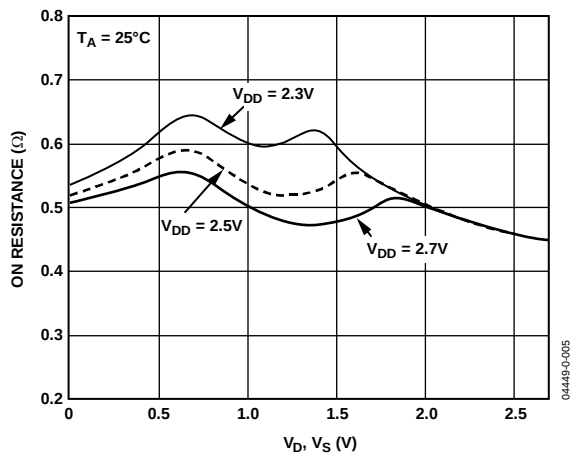
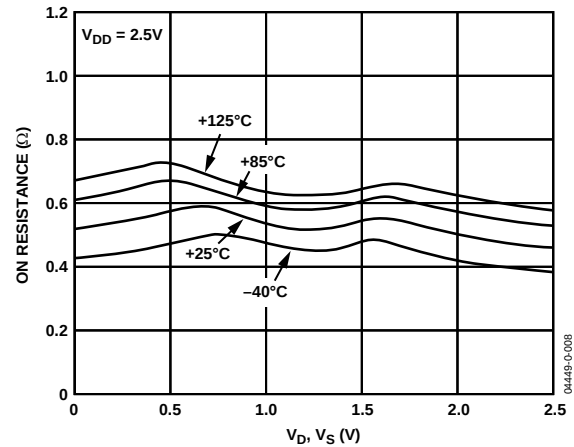
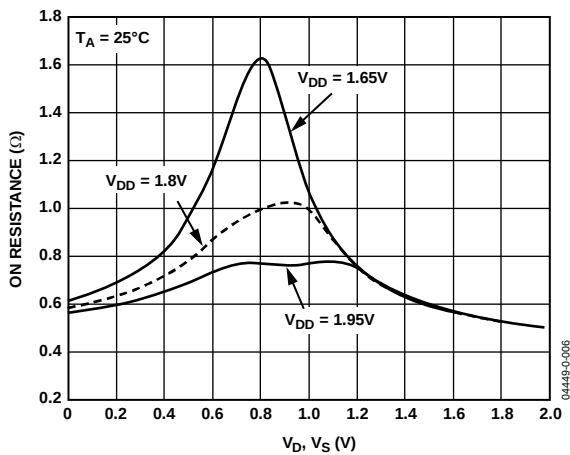
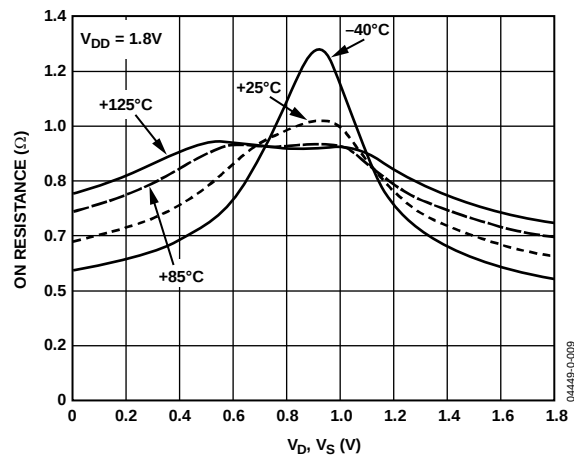


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5	IN1, IN2	Logic Control Inputs.
2, 4, 7, 9	S1A, S2A, S2B, S1B	Source Terminals. These pins may be an input or output.
3	GND	Ground (0 V) Reference.
6, 10	D2, D1	Drain Terminals. These pins may be an input or output.
8	VDD	Most Positive Power Supply Potential.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 3. On Resistance vs. V_D (V_S), $V_{DD} = 2.7\text{ V to } 3.6\text{ V}$ Figure 6. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 3.3\text{ V}$ Figure 4. On Resistance vs. V_D (V_S), $V_{DD} = 2.5\text{ V} \pm 0.2\text{ V}$ Figure 7. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 2.5\text{ V}$ Figure 5. On Resistance vs. V_D (V_S), $V_{DD} = 1.8\text{ V} \pm 0.15\text{ V}$ Figure 8. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 1.8\text{ V}$

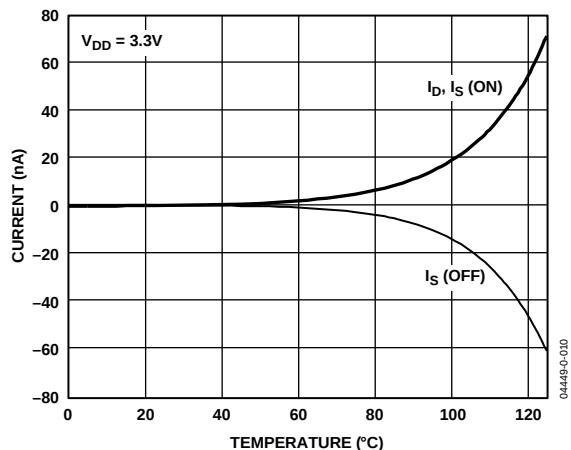
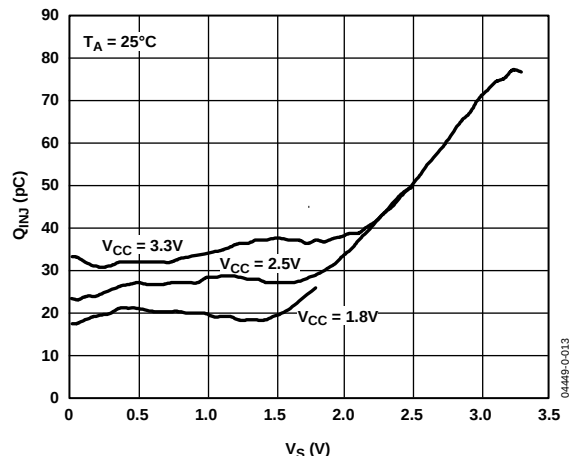
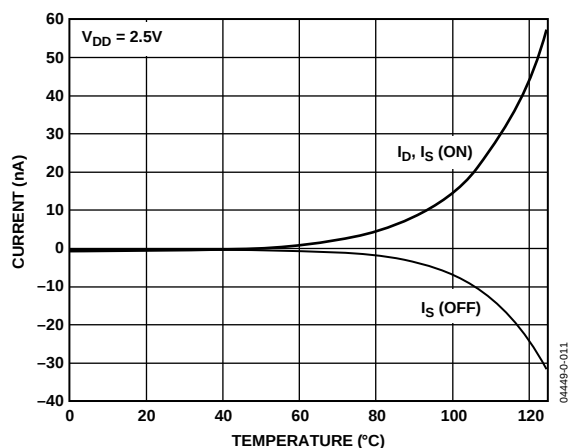
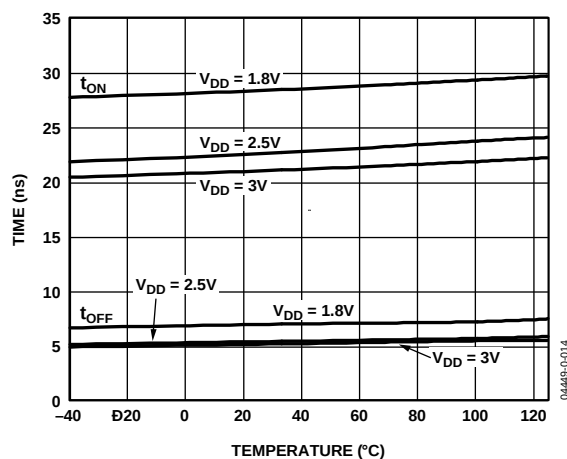
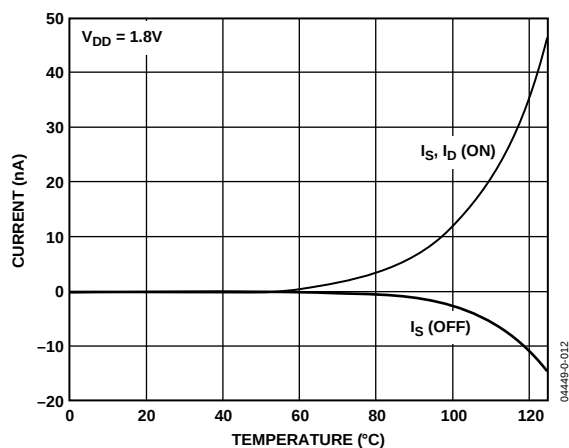
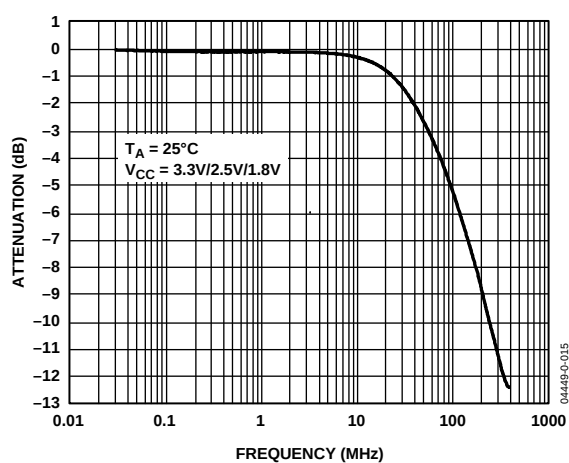
Figure 9. Leakage Current vs. Temperature, $V_{DD} = 3.3V$ Figure 12. Charge Injection (Q_{INJ}) vs. Source Voltage (V_S)Figure 10. Leakage Current vs. Temperature, $V_{DD} = 2.5V$ Figure 13. t_{ON}/t_{OFF} Time vs. TemperatureFigure 11. Leakage Current vs. Temperature, $V_{DD} = 1.8V$ 

Figure 14. Bandwidth

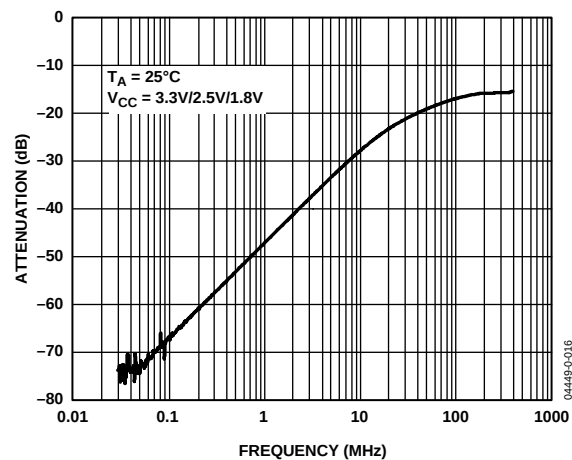


Figure 15. Off Isolation vs. Frequency

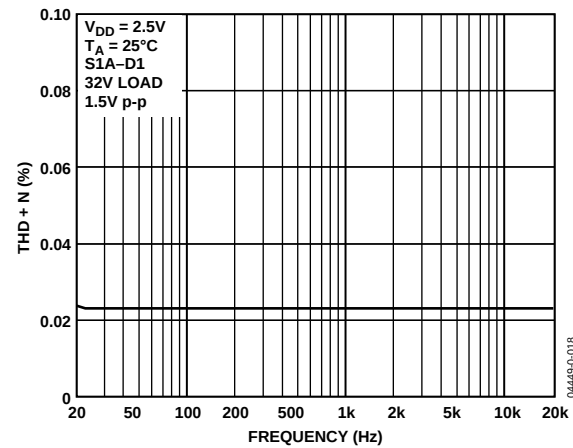


Figure 17. Total Harmonic Distortion + Noise (THD + N) vs. Frequency

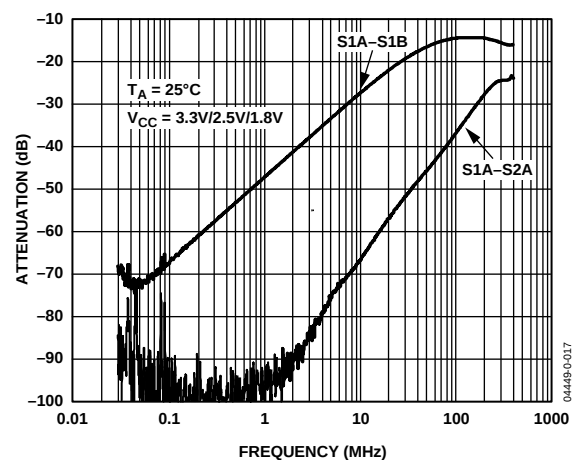


Figure 16. Crosstalk vs. Frequency

TEST CIRCUITS

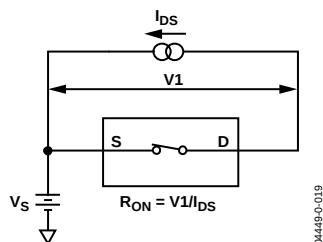


Figure 18. On Resistance

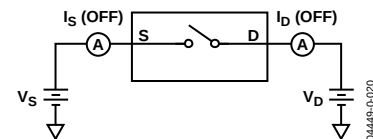


Figure 19. Off Leakage

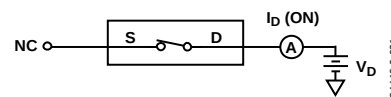


Figure 20. On Leakage

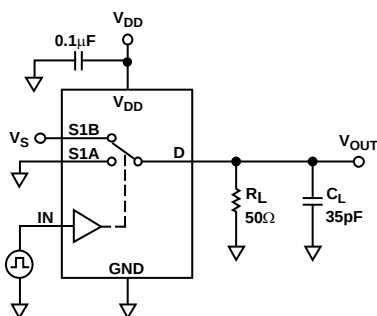
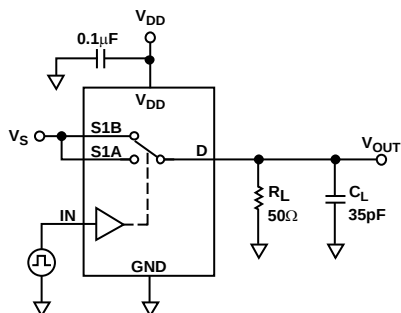
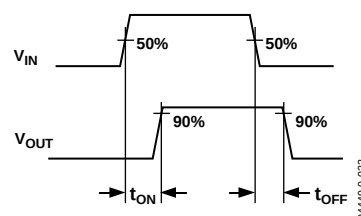
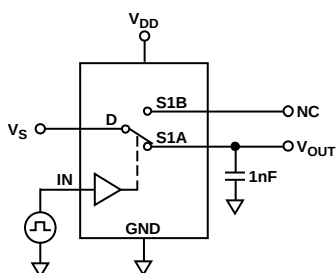
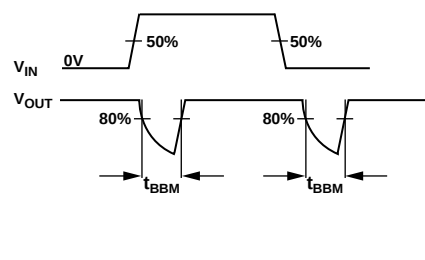
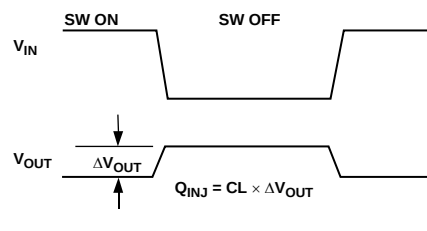
Figure 21. Switching Times, t_{ON} , t_{OFF} Figure 22. Break-Before-Make Time Delay, t_{BBM} 

Figure 23. Charge Injection



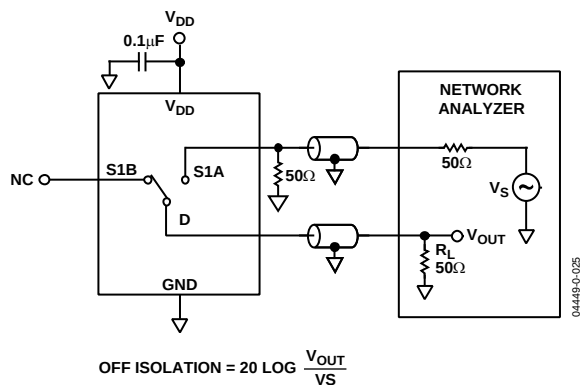


Figure 24. Off Isolation

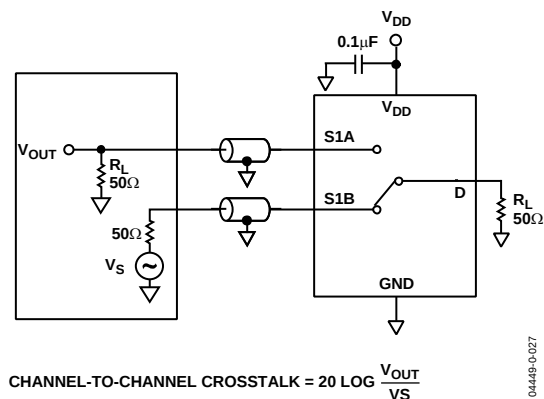


Figure 26. Channel-to-Channel Crosstalk (S1A to S1B)

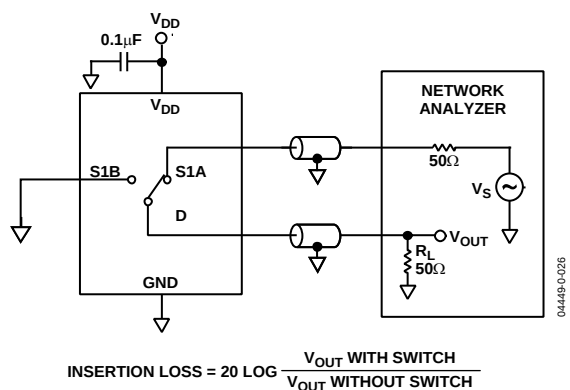


Figure 25. Bandwidth

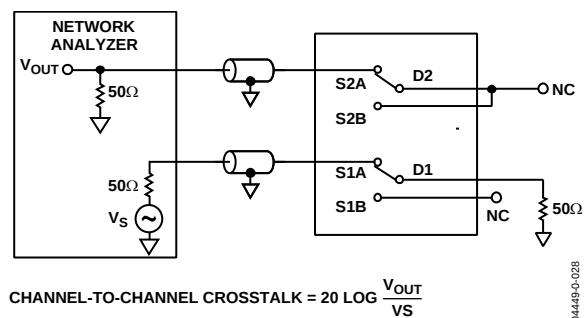


Figure 27. Channel-to-Channel Crosstalk (S1A to S2A)

TERMINOLOGY

I_{DD}

Positive supply current.

V_D (V_S)

Analog voltage on terminals, D and S.

R_{ON}

Ohmic resistance between terminals, D and S.

R_{FLAT (ON)}

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured

ΔR_{ON}

On resistance match between any two channels.

I_S (Off)

Source leakage current with the switch off.

I_D (Off)

Drain leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL} (I_{INH})

Input current of the digital input.

C_S (Off)

Off switch source capacitance. Measured with reference to ground.

C_D (Off)

Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BMM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during on-off switching.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

–3 dB Bandwidth

The frequency at which the output is attenuated by 3 dB.

On Response

The frequency response of the on switch.

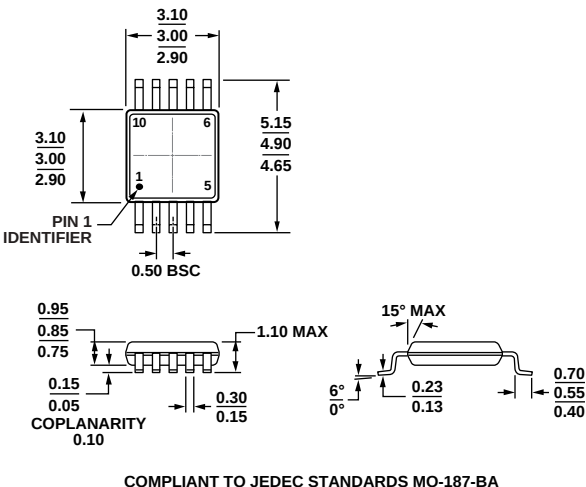
Insertion Loss

The loss due to the on resistance of the switch.

THD + N

The ratio of the harmonic amplitudes plus noise of a signal, to the fundamental.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA
Figure 28. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADG836LYRM	–40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	SQA
ADG836LYRMZ	–40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	S1D
ADG836LYRM-REEL7	–40°C to +125°C	10-Lead Mini Small Outline Package [MSOP]	RM-10	SQA

¹ Z = RoHS Compliant Part.