



QUALITY
SEMICONDUCTOR, INC.

High Speed CMOS 3.3V 16-Bit Bidirectional Transceiver

QS74LCX16245

FEATURES/BENEFITS

- 5V tolerant inputs and outputs
- $10\mu\text{A}$ I_{CCQ} quiescent power supply current
- Hot insertable
- 2.0V-3.6V V_{CC} supply operation
- $\pm 24\text{mA}$ balanced output drive
- Power down high impedance inputs and outputs
- C speed performance: $t_{\text{PD}} = 4.1\text{ns}$
- Input hysteresis for noise immunity
- Meets or exceeds JEDEC Standard 36 specifications
- Multiple power and ground pins for low noise
- Operating temperature range:
-40°C to +85°C
- Latch-up performance exceeds 500mA
- ESD performance:
Human body model > 2000V
Machine model > 200V
- Packages available:
48-pin TSSOP
48-pin SSOP

DESCRIPTION

The QS74LCX16245 is a 16-bit transceiver that is ideal for driving bidirectional address and data buses. This device can be used as either two independent 8-bit transceivers or one 16-bit transceiver determined by the Direction and Output Enable controls. The 3.3V LCX family features low power, low switching noise, and fast switching speeds for low power portable applications as well as high-end, advanced workstation applications. 5V tolerant inputs and outputs allow this LCX product to be used in mixed 5V and 3.3V applications. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. To accommodate hot-plug or live insertion applications, this product is designed not to load an active bus when V_{CC} is removed.

Figure 1. Functional Block Diagram

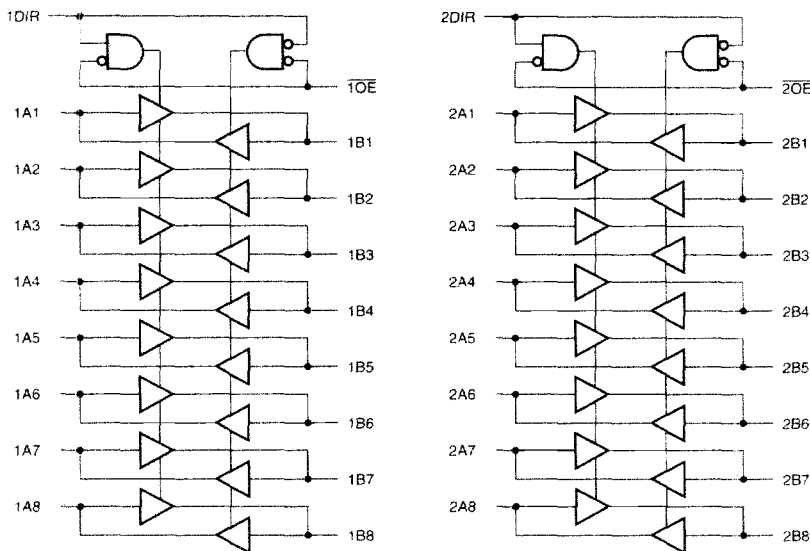


Figure 2. Pin Configuration
(All Pins Top View)

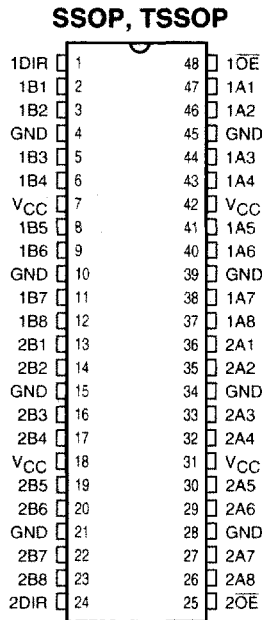


Table 1. Pin Description

Name	Description
xDIR	Transmit/Receive Input
xOE	Output Enable Inputs
xAx	Bus A
xBx	Bus B

Table 2. Function Table

Inputs		Outputs
xOE	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Hi-Z

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Table 3. Capacitance

Symbol	Pins	Typ	Unit	Conditions
C _{IN}	Input Capacitance	7.0	pF	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz
C _{I/O}	I/O Capacitance	8.0	pF	V _{IN} = 0V, V _{OUT} = 0V, f = 1MHz
C _{PD}	Power Dissipation Capacitance	20	pF	V _{CC} = 3.3V, V _{IN} = 0 or V _{CC} f = 10MHz

Note: Capacitance is characterized but not production tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to +7.0V
DC Output Voltage V _{OUT}	
Outputs HIGH-Z	-0.5V to +7.0V
Outputs Active	-0.5V to V _{CC} + 0.5V
DC Input Voltage V _{IN}	-0.5V to 7.0V
DC Input Diode Current with V _{IN} < 0	-50mA
DC Output Diode Current	
V _O < 0	-50mA
V _O > V _{CC}	+50mA
DC Output Source/Sink Current (I _{OH} /I _{OL})	±50mA
DC Supply Current per Supply Pin	±100mA
DC Ground Current per Ground Pin	±100mA
T _{STG} Storage Temperature	-65°C to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage, Operating	2.0	3.6	V
V_{IN}	Input Voltage	0	5.5	V
V_{OUT}	Output Voltage in Active State	0	V_{CC}	V
V_{OUT}	Output Voltage in "OFF" State	0	5.5	V
I_{OH}/I_{OL}	Output Current $V_{CC} = 3.0 - 3.6V$ $V_{CC} = 2.7V$	—	± 24 ± 12	mA
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	-40	+85	°C

Table 6. DC Electrical Characteristics Over Operating RangeIndustrial Temperature Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Typ ⁽²⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.7V, I_{OH} = -100\mu A$ $V_{CC} = 2.7V, I_{OH} = -12mA$ $V_{CC} = 3.0V, I_{OH} = -18mA$ $V_{CC} = 3.0V, I_{OH} = -24mA$	$V_{CC}-0.2$ 2.2 2.4 2.2	— — — —	— — — —	V
V_{OL}	Output LOW Voltage	$V_{CC} = 2.7V, I_{OL} = 100\mu A$ $V_{CC} = 2.7V, I_{OL} = 12mA$ $V_{CC} = 3.0V, I_{OL} = 16mA$ $V_{CC} = 3.0V, I_{OL} = 24mA$	— — — —	— — — —	0.2 0.4 0.4 0.5	V
ΔV_T	Input Hysteresis ⁽³⁾	$V_{TLH} - V_{THL}$ for All Inputs	—	150	—	mV
I_I	Input Leakage Current	$V_I = 0V, V_I = 5.5V, V_{CC} = 3.6V$	—	—	± 1.0	μA
I_{OZ}	High-Z I/O Leakage	$V_O = 0V, V_O = 5.5V$ $V_I = V_{IH}$ or $V_{IL}, V_{CC} = 3.6V$	—	—	± 1.0	μA
I_{OS}	Short Circuit Current ^(3,4)	$V_{CC} = 3.6V, V_O = GND$	-60	—	-240	mA
I_{OFF}	Power Off Leakage	$V_{CC} = 0V, V_I$ or $V_O = 5.5V$	—	—	10	μA
V_{IK}	Input Clamp Voltage	$V_{CC} = 2.7V, I_{IN} = -18mA$	—	-0.7	-1.2	V

Notes:

1. For conditions shown as Max or Min use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, and $T_A = 25^\circ\text{C}$.
3. These parameters are guaranteed by characterization, but not production tested.
4. Not more than one output should be tested at one time. Duration of test should not exceed one second.

Table 7. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Typ ⁽²⁾	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = 3.6V$, Freq = 0 $V_{IN} = GND$ or V_{CC}	0.1	10	μA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.6V$, $V_{IN} = V_{CC}-0.6V^{(3)}$	2.0	30	μA
I_{CCD}	Supply Current per Input per MHz ⁽⁴⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle $x\overline{OE} = GND$	50	75	$\mu A/MHz$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = 3.6V$, Outputs Open One Bit Toggling @ 50% Duty Cycle $x\overline{OE} = GND$, $f_i = 10MHz$	$V_{IN} = V_{CC}-0.6V$ $V_{IN} = GND$ 0.5 ⁽⁵⁾	0.8 ⁽⁵⁾	mA
		$V_{CC} = 3.6V$, Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle $x\overline{OE} = GND$, $f_i = 2.5MHz$	$V_{IN} = V_{CC}-0.6V$ $V_{IN} = GND$ 2.0 ⁽⁵⁾	3.3 ⁽⁵⁾	

Notes:

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
- Per TTL driven input. All Other Inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$
 I_{CCQ} = Quiescent Current (I_{CCL} , I_{CCH} , and I_{CCZ}).
 ΔI_{CC} = Power Supply Current for a TTL-High Input ($V_{IN} = V_{CC}-0.6V$).
 D_H = Duty Cycle for TTL High Inputs.
 N_T = Number of TTL High Inputs.
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
 f = Average Switching Frequency per Output
 N_O = Number of Outputs Switching

Table 8. Dynamic Switching Characteristics⁽¹⁾

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ C$	Units
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50pF$, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V

Note:

- Characterized but not production tested.

Table 9. Switching Characteristics Over Operating RangeIndustrial Temperature Range, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. $C_{\text{LOAD}} = 50\text{pF}$, $R_{\text{LOAD}} = 500\Omega$ unless otherwise noted.

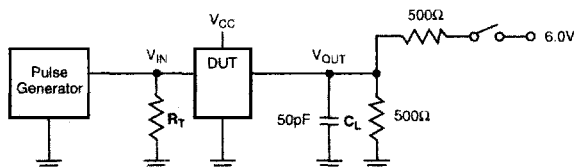
Symbol	Description ⁽¹⁾	16245				16245C		Unit
		$V_{CC} = 3.3 \pm 0.3V$		$V_{CC} = 2.7V^{(2)}$		$V_{CC} = 3.3 \pm 0.3V$		
		Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay A to B, B to A	1.5	4.5	1.5	5.2	1.5	4.1	ns
t_{PZH} t_{PZL}	Output Enable Time xOE to A or B	1.5	6.5	1.5	7.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾ xOE to A or B	1.5	6.4	1.5	6.9	1.5	4.8	ns
t_{PZH} t_{PZL}	Output Enable Time ⁽²⁾ xDIR to A or B	1.5	6.5	1.5	7.2	1.5	5.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time ⁽²⁾ xDIR to A or B	1.5	6.4	1.5	6.9	1.5	4.8	ns
$t_{SK}(O)$	Output Skew ⁽³⁾	—	0.5	—	—	—	0.5	ns

Notes:

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. Guaranteed by characterization.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

TEST CIRCUIT AND WAVEFORMS

Figure 3. Test Circuit



SWITCH POSITION

Test	Switch
Open Drain	
Disable LOW	6V
Enable LOW	
Disable HIGH	GND
Enable HIGH	
All Other Inputs	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse generator.

Figure 4. Setup, Hold, and Release Timing

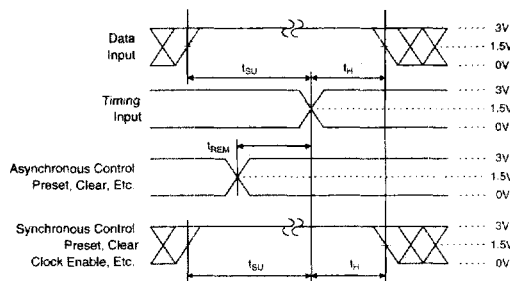


Figure 6. Pulse Width

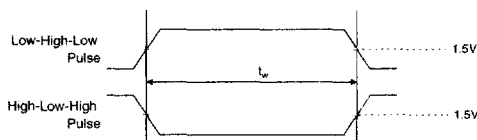


Figure 5. Enable and Disable Timing

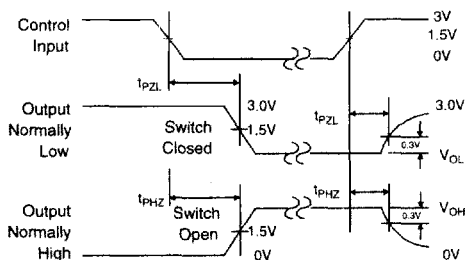
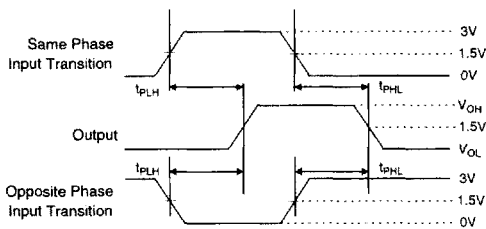


Figure 7. Propagation Delay



Notes:

1. Input Control Enable = LOW and input Control Disable = HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$;
 $Z_{OUT} \leq 50\Omega$; t_F , $t_R \leq 2.5\text{ns}$.