

18-BIT STEREO AUDIO CODEC, SINGLE-ENDED ANALOG INPUT/OUTPUT

FEATURES

- **Monolithic 18-Bit $\Delta\Sigma$ ADC and DAC**
- **16- or 18-Bit Input/Output Data**
- **Accepts Seven Alternate Formats**
- **Stereo ADC:**
 - **Single-Ended Voltage Input**
 - **64 \times Oversampling Digital Filter**
 - **Pass-Band Ripple: ± 0.05 dB**
 - **Stop-Band Attenuation: -65 dB**
 - **High Performance:**
 - **THD+N: -88 dB**
 - **SNR: 94 dB**
 - **Dynamic Range: 94 dB**
 - **Digital High-Pass Filter**
- **Stereo DAC**
 - **Single-Ended Voltage Output**
 - **Analog Low-Pass Filter**
 - **8 \times Oversampling Digital Filter**
 - **Pass-Band Ripple: ± 0.17 dB**
 - **Stop-Band Attenuation: 35 dB**
 - **High Performance:**
 - **THD+N: -90 dB**
 - **SNR: 98 dB**
 - **Dynamic Range: 97 dB**
- **Special Features (PCM3000)**
 - **Digital De-Emphasis**
 - **Digital Attenuation (256 Steps)**
 - **Soft Mute**
 - **Digital Loopback**
- **Sample Rate: 4 kHz to 48 kHz**
- **System Clock: 256 f_s , 384 f_s , 512 f_s**

- **Single 5-V Power Supply**
- **Small Package: SSOP-28**

APPLICATIONS

- **Sampling Keyboards**
- **Digital Mixers**
- **Mini-Disk Recorders**
- **Hard-Disk Recorders**
- **Karaoke Systems**
- **DSP-Based Car Stereo**
- **DAT Recorders**
- **Video Conferencing**

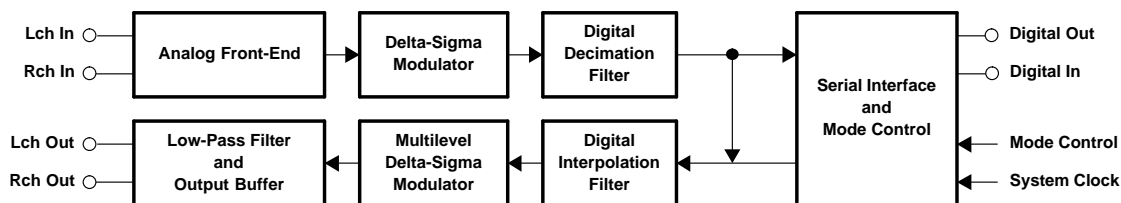
DESCRIPTION

The PCM3000/3001 is a low-cost, single-chip stereo audio codec (analog-to-digital and digital-to-analog converter) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64-times oversampling. The ADCs include a digital decimation filter and the DACs include an 8-times oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. The PCM3000/3001 operates with left-justified, right-justified, I²S or DSP data formats.

The PCM3000 can be programmed with a three-wire serial interface for special features and data formats. The PCM3001 can be pin-programmed for data formats.

The PCM3000 and PCM3001 are fabricated using a highly advanced CMOS process and are available in a small 28-pin SSOP package. The PCM3000/3001 are suitable for a wide variety of cost-sensitive consumer applications where good performance is required.



B0006-03



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CC} = 5\text{ V}$, $f_S = 44.1\text{ kHz}$, $\text{SYSCLK} = 384\text{ f}_S$, CLKIO input, and 18-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|-----------------------------------|-------------------------------------|---------------|-----------|---------------|------------------------------|
| DIGITAL INPUT/OUTPUT | | | | | | |
| Input Logic | | | | | | |
| $V_{IH}^{(1)}$ | Input logic level | | 2 | | | VDC |
| $V_{IL}^{(1)}$ | | | | | 0.8 | |
| $I_{IN}^{(2)}$ | Input logic current | | | | ± 1 | μA |
| $I_{IN}^{(3)}$ | | | | | -120 | |
| $V_{IH}^{(4)}$ | Input logic level | | $0.64 V_{DD}$ | | | VDC |
| $V_{IL}^{(4)}$ | | | | | $0.28 V_{DD}$ | |
| $I_{IN}^{(4)}$ | Input logic current | | | | ± 40 | μA |
| Output Logic | | | | | | |
| $V_{OH}^{(5)}$ | Output logic level | $I_{OUT} = -1.6\text{ mA}$ | 4.5 | | | VDC |
| $V_{OL}^{(5)}$ | | $I_{OUT} = 3.2\text{ mA}$ | | | 0.5 | |
| $V_{OH}^{(6)}$ | Output logic level | $I_{OUT} = -3.2\text{ mA}$ | 4.5 | | | |
| $V_{OL}^{(6)}$ | | $I_{OUT} = 3.2\text{ mA}$ | | | 0.5 | |
| Clock Frequency | | | | | | |
| f_S | Sampling frequency | | $4^{(7)}$ | 44.1 | 48 | kHz |
| | System clock frequency | 256 f_S | 1.024 | 11.2896 | 12.288 | MHz |
| | | 384 f_S | 1.536 | 16.9344 | 18.432 | |
| | | 512 f_S | 2.048 | 22.5792 | 24.576 | |
| ADC CHARACTERISTICS | | | | | | |
| Resolution | | | | 18 | | Bits |
| DC Accuracy | | | | | | |
| | Gain mismatch, channel-to-channel | | | ± 1 | ± 5 | % of FSR |
| | Gain error | | | ± 2 | ± 5 | |
| | Gain drift | | | ± 20 | | ppm of FSR/ $^\circ\text{C}$ |
| | Bipolar zero error | High-pass filter off ⁽⁸⁾ | | ± 1.7 | | % of FSR |
| | Bipolar zero drift | High-pass filter off ⁽⁸⁾ | | ± 20 | | ppm of FSR/ $^\circ\text{C}$ |

(1) Pins 16, 17, 18, 22, 25, 26, 27, 28: LRCIN, BCKIN, DIN, CLKIO, MC/FMT2, MD/FMT1, ML/FMT0, RSTB

(2) Pins 16, 17, 18, 22: LRCIN, BCKIN, DIN, CLKIO (Schmitt-trigger input)

(3) Pins 25, 26, 27, 28: MC/FMT2, MD/FMT1, ML/FMT0, RSTB (Schmitt-trigger input, 70-k Ω internal pullup resistor)

(4) Pin 20: XT1

(5) Pins 19, 22: DOUT, CLKIO

(6) Pin 21: XTO

(7) Refer to Application Bulletin [SBAA033](#) for information relating to operation at lower sampling frequencies.

(8) High-pass filter disabled (PCM3000 only) to measure dc offset

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CC} = 5\text{ V}$, $f_S = 44.1\text{ kHz}$, $\text{SYSCLK} = 384 f_S$, CLKIO input, and 18-bit data, unless otherwise noted

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-------------|-------------|-------------|------------------------------|
| Dynamic Performance⁽⁹⁾ | | | | | |
| THD+N | $f = 1\text{ kHz}$, $V_{IN} = -0.5\text{ dB}$ | | -88 | -80 | dB |
| | $f = 1\text{ kHz}$, $V_{IN} = -60\text{ dB}$ | | -31 | | |
| Dynamic range | $f = 1\text{ kHz}$, A-weighted | 90 | 94 | | dB |
| Signal-to-noise ratio | $f = 1\text{ kHz}$, A-weighted | 90 | 94 | | dB |
| Channel separation | | 88 | 92 | | dB |
| Digital Filter Performance | | | | | |
| Pass band | | | | $0.454 f_S$ | Hz |
| Stop band | | $0.583 f_S$ | | | Hz |
| Pass-band ripple | | | | ± 0.05 | dB |
| Stop-band attenuation | | -65 | | | dB |
| Delay time (latency) | | | $17.4/f_S$ | | s |
| Digital High-Pass Filter Response | | | | | |
| Cutoff frequency | -3 dB | | $0.019 f_S$ | | mHz |
| ANALOG INPUT | | | | | |
| Voltage range | 0 dB (full scale) | | 2.9 | | Vp-p |
| Center voltage | | | 2.1 | | VDC |
| Input impedance | | | 15 | | k Ω |
| Antialiasing Filter | | | | | |
| Cutoff frequency | -3 dB, $C_{EXT} = 470\text{ pF}$ | | 170 | | kHz |
| DAC CHARACTERISTICS | | | | | |
| Resolution | | | 18 | | Bits |
| DC Accuracy | | | | | |
| Gain mismatch, channel-to-channel | | | ± 1 | ± 5 | % of FSR |
| Gain error | | | ± 1 | ± 5 | % of FSR |
| Gain drift | | | ± 20 | | ppm of FSR/ $^\circ\text{C}$ |
| Bipolar zero error | | | ± 1 | | % of FSR |
| Bipolar zero drift | | | ± 20 | | ppm of FSR/ $^\circ\text{C}$ |
| Dynamic Performance⁽⁹⁾ | | | | | |
| THD+N | $V_{OUT} = 0\text{ dB}$ (full scale) | | -90 | -80 | dB |
| | $V_{OUT} = -60\text{ dB}$ | | -34 | | |
| Dynamic range | EIAJ A-weighted | 90 | 97 | | dB |
| Signal-to-noise ratio (idle channel) | EIAJ A-weighted | 92 | 98 | | dB |
| Channel separation | | 90 | 95 | | dB |
| Digital Filter Performance | | | | | |
| Pass band | | | | $0.445 f_S$ | Hz |
| Stop band | | $0.555 f_S$ | | | Hz |
| Pass-band ripple | | | | ± 0.17 | dB |
| Stop-band attenuation | | -35 | | | dB |
| Delay time | | | $11.1/f_S$ | | s |

(9) $f_{IN} = 1\text{ kHz}$, using the System Two™ audio measurement system by Audio Precision™, rms mode with 20-kHz LPF, 400-Hz HPF used for performance calculation or measurement.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{CC} = 5\text{ V}$, $f_s = 44.1\text{ kHz}$, $\text{SYSCLK} = 384 f_s$, CLKIO input, and 18-bit data, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|--------------------|--------------------------------|-----|---------------|-----|---------------------------|
| Analog Output | | | | | | |
| Voltage range | | | | 0.62 V_{CC} | | Vp-p |
| Center voltage | | | | 0.5 V_{CC} | | VDC |
| Load impedance | | AC load | 5 | | | k Ω |
| Analog Low-Pass Filter | | | | | | |
| Frequency response | | $f = 20\text{ kHz}$ | | -0.16 | | dB |
| POWER SUPPLY REQUIREMENTS | | | | | | |
| V_{CC} | Voltage range | | 4.5 | 5 | 5.5 | VDC |
| V_{DD} | | | 4.5 | 5 | 5.5 | VDC |
| $I_{CC}, I_{DD}^{(10)}$ | Supply current | $V_{CC} = V_{DD} = 5\text{ V}$ | | 32 | 50 | mA |
| | Power dissipation | $V_{CC} = V_{DD} = 5\text{ V}$ | | 160 | 250 | mW |
| TEMPERATURE RANGE | | | | | | |
| T_A | Operation | | -25 | | 85 | $^\circ\text{C}$ |
| T_{stg} | Storage | | -55 | | 125 | $^\circ\text{C}$ |
| θ_{JA} | Thermal resistance | | | 100 | | $^\circ\text{C}/\text{W}$ |

(10) With no load on XTO and CLKIO

PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE | PACKAGE CODE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA | QUANTITY |
|----------|-------------|--------------|-----------------|-----------------|-----------------|----------|
| PCM3000E | 28-pin SSOP | DB | PCM3000E | PCM3000E | Rails | 47 |
| | | | | PCM3000E/2K | Tape and reel | 2000 |
| PCM3001E | | | PCM3001E | PCM3001E | Rails | 47 |
| | | | | PCM3001E/2K | Tape and reel | 2000 |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

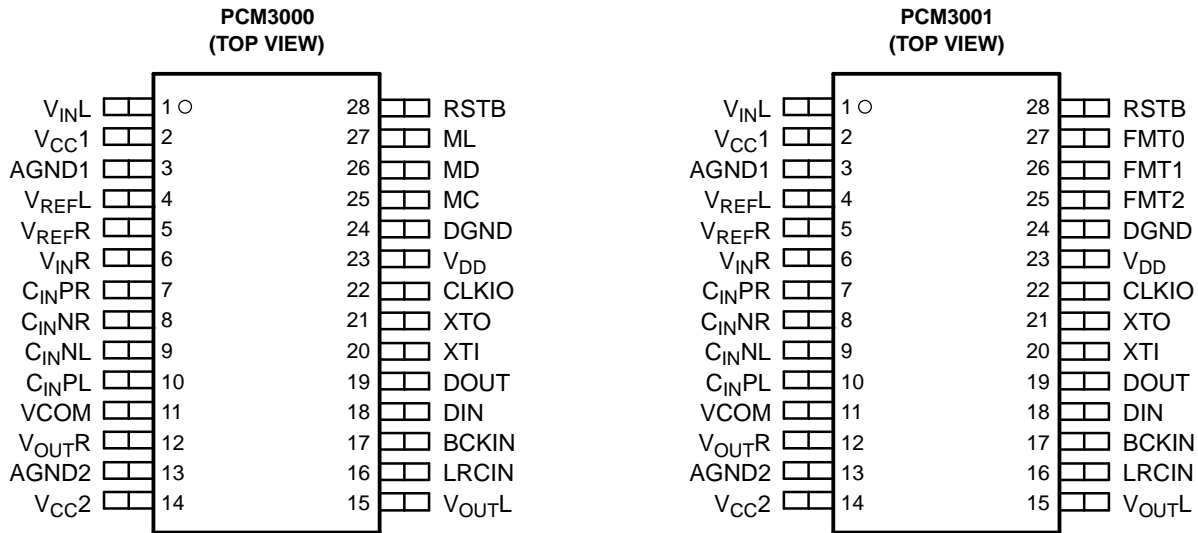
| | |
|--|---|
| Supply voltage: V_{DD}, V_{CC1}, V_{CC2} | -0.3 V to 6.5 V |
| Supply voltage differences | $\pm 0.1\text{ V}$ |
| GND voltage differences | $\pm 0.1\text{ V}$ |
| Digital input voltage | -0.3 to $V_{DD} + 0.3\text{ V}$, < 6.5 V |
| Analog input voltage | -0.3 to $V_{CC1}, V_{CC2} + 0.3\text{ V}$, < 6.5 V |
| Power dissipation | 300 mW |
| Input current (any pins except supplies) | $\pm 10\text{ mA}$ |
| Operating temperature | -25 $^\circ\text{C}$ to 85 $^\circ\text{C}$ |
| Storage temperature | -55 $^\circ\text{C}$ to 125 $^\circ\text{C}$ |
| Lead temperature, soldering | 260 $^\circ\text{C}$, 5 s |
| Package temperature (IR reflow, peak) | 235 $^\circ\text{C}$ |

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|----------------|------------|------------|------------|--------------|
| Analog supply voltage, V_{CC1} , V_{CC2} | | 4.5 | 5 | 5.5 | VDC |
| Digital supply voltage, V_{DD} | | 4.5 | 5 | 5.5 | VDC |
| Analog input voltage, full scale (–0 dB) | | | 2.9 | | Vp-p |
| Digital input logic family | | | TTL | | |
| Digital input clock frequency | System clock | 8.192 | | 24.576 | MHz |
| | Sampling clock | 32 | | 48 | kHz |
| Analog output load resistance | | 5 | | | k Ω |
| Analog output load capacitance | | | 50 | | pF |
| Digital output load capacitance | | | 10 | | pF |
| Operating free-air temperature, T_A | | –25 | | 85 | $^{\circ}$ C |

PIN CONFIGURATION—PCM3000/3001



P0007-01

PIN ASSIGNMENTS—PCM3000

| NAME | PIN | I/O | DESCRIPTION |
|-------------------|-----|-----|---|
| AGND1 | 3 | – | ADC analog ground |
| AGND2 | 13 | – | DAC analog ground |
| BCKIN | 17 | I | Bit clock input ⁽¹⁾ |
| C _{INNL} | 9 | – | ADC antialias filter capacitor (–), Lch |
| C _{INNR} | 8 | – | ADC antialias filter capacitor (–), Rch |
| C _{INPL} | 10 | – | ADC antialias filter capacitor (+), Lch |
| C _{INPR} | 7 | – | ADC antialias filter capacitor (+), Rch |
| CLKIO | 22 | I/O | Buffered oscillator output or external clock input ⁽¹⁾ |
| DGND | 24 | – | Digital ground |
| DIN | 18 | I | Data input ⁽¹⁾ |
| DOUT | 19 | O | Data output |
| LRCIN | 16 | I | Sample rate clock input (f _s) ⁽¹⁾ |
| MC | 25 | I | Serial mode control, bit clock |
| MD | 26 | I | Serial mode control, data |
| ML | 27 | I | Serial mode control, strobe pulse |
| RSTB | 28 | I | Reset, active-low ⁽¹⁾⁽²⁾ |
| V _{CC1} | 2 | – | ADC analog power supply |
| V _{CC2} | 14 | – | DAC analog power supply |
| V _{DD} | 23 | – | Digital power supply |
| VCOM | 11 | – | DAC output common |
| V _{INL} | 1 | I | ADC analog input, Lch |
| V _{INR} | 6 | I | ADC analog input, Rch |
| V _{OUTL} | 15 | O | DAC analog output, Lch |
| V _{OUTR} | 12 | O | DAC analog output, Rch |
| V _{REFL} | 4 | – | ADC input reference, Lch |
| V _{REFR} | 5 | – | ADC input reference, Rch |

(1) Schmitt-trigger input
(2) With 70-kΩ typical internal pullup resistor

PIN ASSIGNMENTS—PCM3000 (continued)

| NAME | PIN | I/O | DESCRIPTION |
|------|-----|-----|-------------------|
| XTI | 20 | I | Oscillator input |
| XTO | 21 | O | Oscillator output |

PIN ASSIGNMENTS—PCM3001

| NAME | PIN | I/O | DESCRIPTION |
|-------------------|-----|-----|---|
| AGND1 | 3 | – | ADC analog ground |
| AGND2 | 13 | – | DAC analog ground |
| BCKIN | 17 | I | Bit clock input ⁽¹⁾ |
| C _{INL} | 9 | – | ADC antialias filter capacitor (–), Lch |
| C _{INR} | 8 | – | ADC antialias filter capacitor (–), Rch |
| C _{INPL} | 10 | – | ADC antialias filter capacitor (+), Lch |
| C _{INPR} | 7 | – | ADC antialias filter capacitor (+), Rch |
| CLKIO | 22 | I/O | Buffered oscillator output or external clock input ⁽¹⁾ |
| DGND | 24 | – | Digital ground |
| DIN | 18 | I | Data input ⁽¹⁾ |
| DOUT | 19 | O | Data output |
| FMT0 | 27 | I | Audio data format control 0 ⁽¹⁾⁽²⁾ |
| FMT1 | 26 | I | Audio data format control 1 ⁽¹⁾⁽²⁾ |
| FMT2 | 25 | I | Audio data format control 2 ⁽¹⁾⁽²⁾ |
| LRCIN | 16 | I | Sample rate clock input (f _S) ⁽¹⁾ |
| RSTB | 28 | I | Reset, active-low ⁽¹⁾⁽²⁾ |
| V _{CC1} | 2 | – | ADC analog power supply |
| V _{CC2} | 14 | – | DAC analog power supply |
| V _{DD} | 23 | – | Digital power supply |
| VCOM | 11 | – | DAC output common |
| V _{INL} | 1 | I | ADC analog input, Lch |
| V _{INR} | 6 | I | ADC analog input, Rch |
| V _{OUTL} | 15 | O | DAC analog output, Lch |
| V _{OUTR} | 12 | O | DAC analog output, Rch |
| V _{REFL} | 4 | – | ADC input reference, Lch |
| V _{REFR} | 5 | – | ADC input reference, Rch |
| XTI | 20 | I | Oscillator input |
| XTO | 21 | O | Oscillator output |

(1) Schmitt-trigger input

(2) With 70-k Ω typical internal pullup resistor

TYPICAL PERFORMANCE CURVES OF ADC SECTION

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, $f_{IN} = 1\text{ kHz}$, $f_S = 44.1\text{ kHz}$, 18-bit data, $V_{IN} = 2.9\text{ Vp-p}$, and $\text{SYSCLK} = 384 f_S$, unless otherwise noted

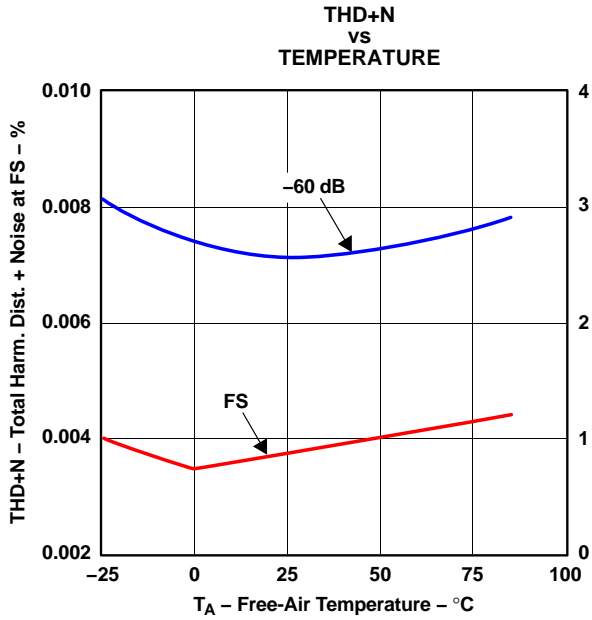


Figure 1.

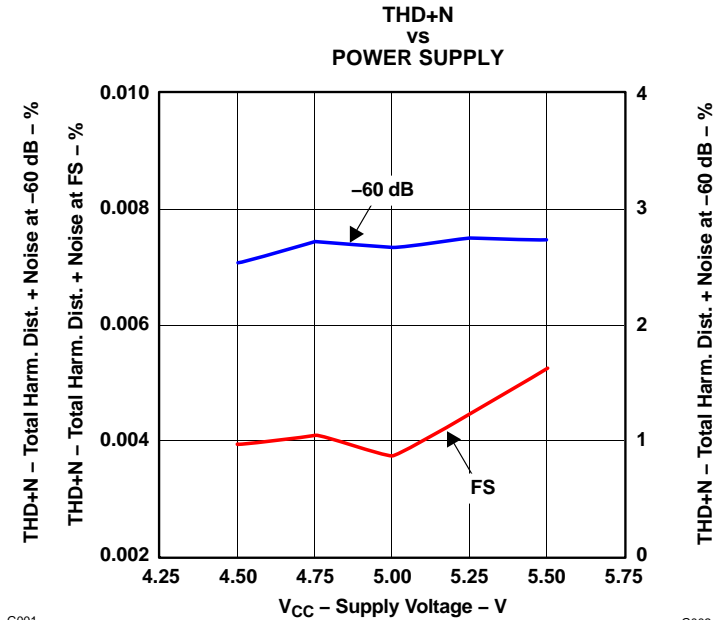


Figure 2.

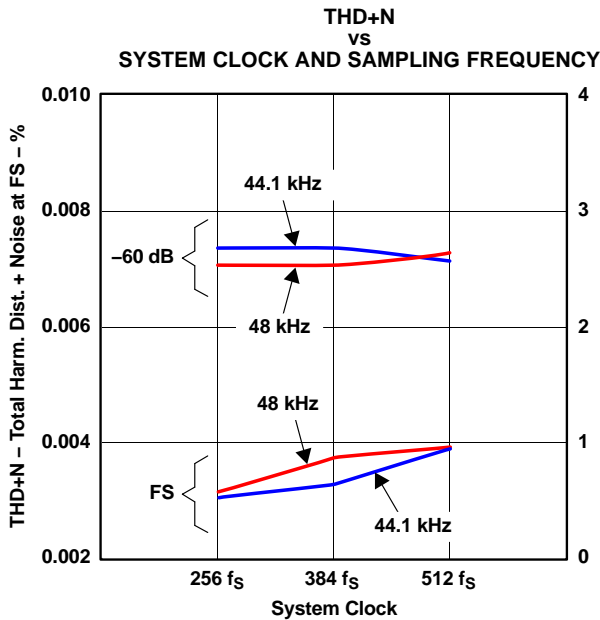


Figure 3.

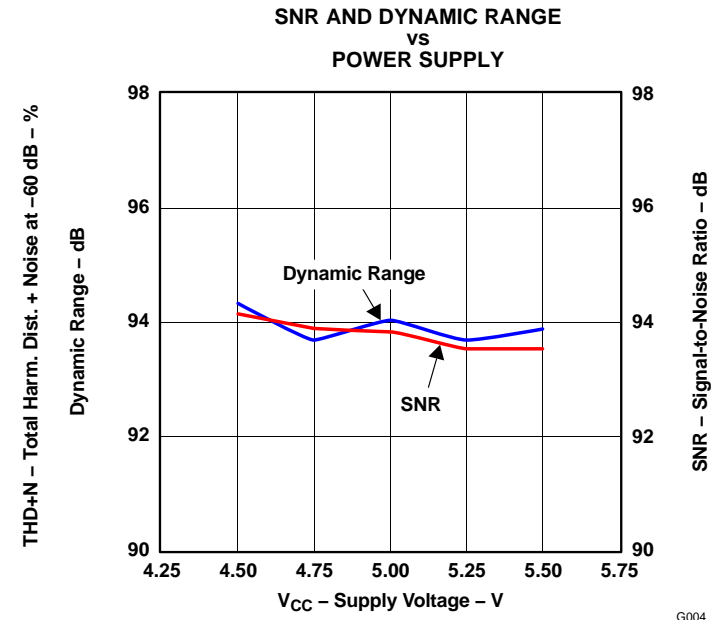


Figure 4.

TYPICAL PERFORMANCE CURVES OF ADC SECTION (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, $f_{IN} = 1\text{ kHz}$, $f_S = 44.1\text{ kHz}$, 18-bit data, $V_{IN} = 2.9\text{ Vp-p}$, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

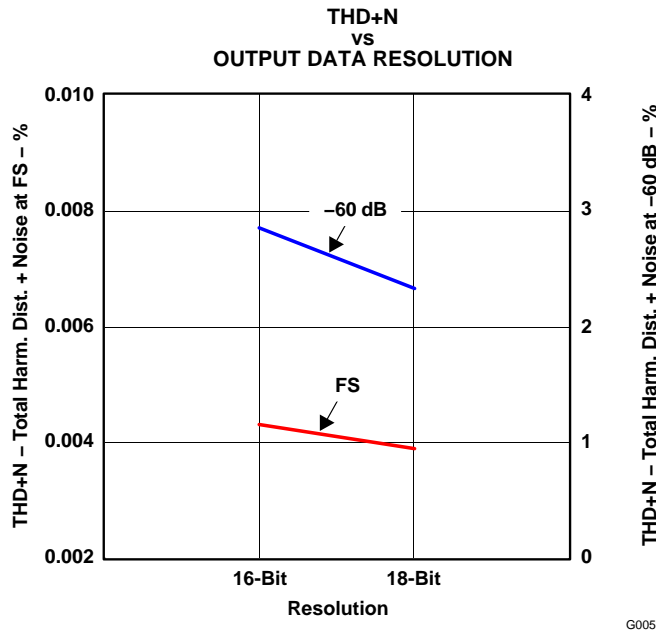


Figure 5.

TYPICAL PERFORMANCE CURVES OF DAC SECTION

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, $f_{IN} = 1\text{ kHz}$, $f_S = 44.1\text{ kHz}$, 18-bit data, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

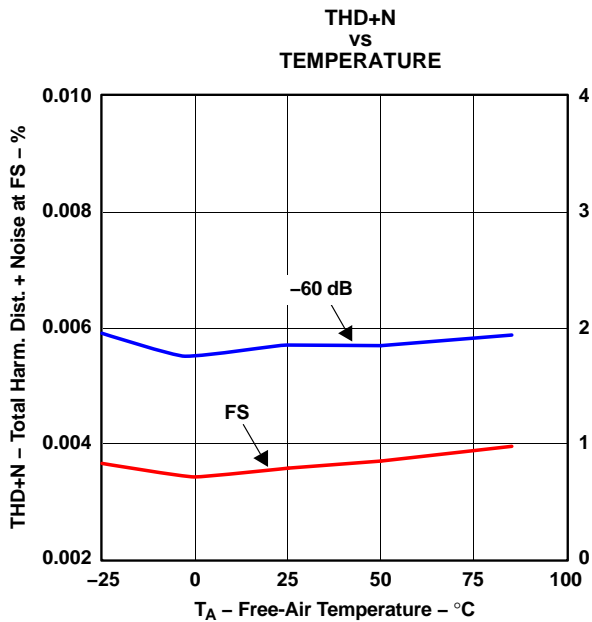


Figure 6.

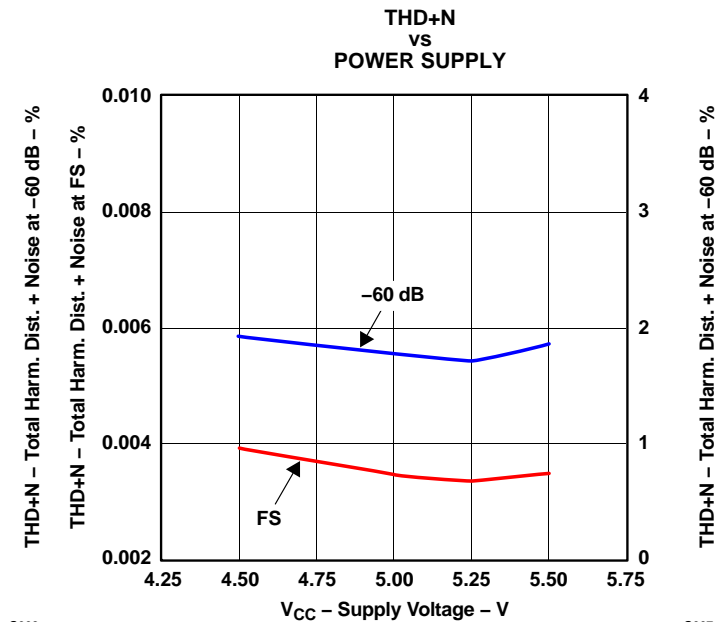


Figure 7.

TYPICAL PERFORMANCE CURVES OF DAC SECTION (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, $f_{IN} = 1\text{ kHz}$, $f_S = 44.1\text{ kHz}$, 18-bit data, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

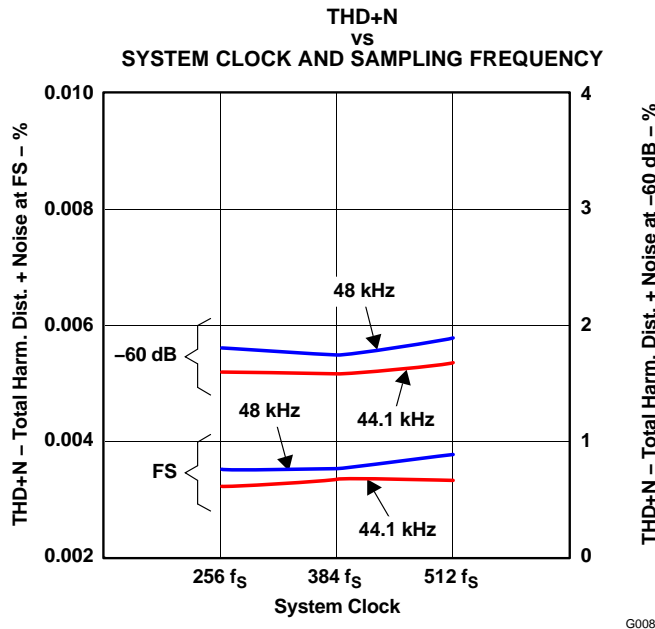


Figure 8.

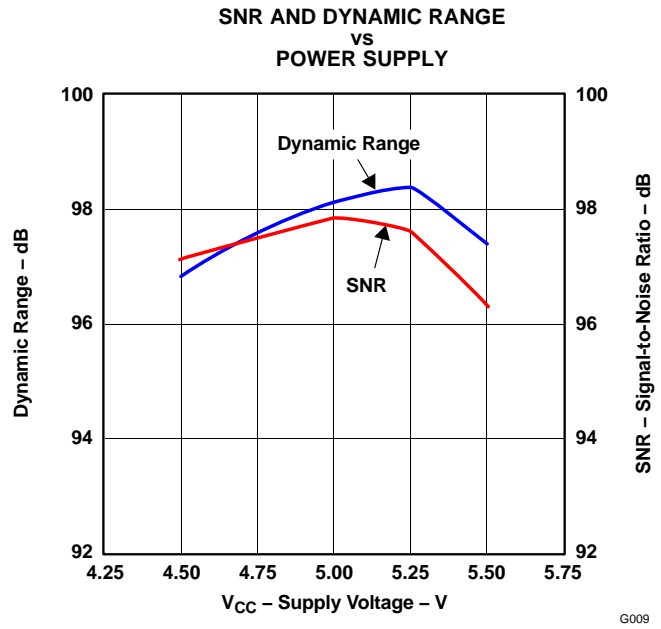


Figure 9.

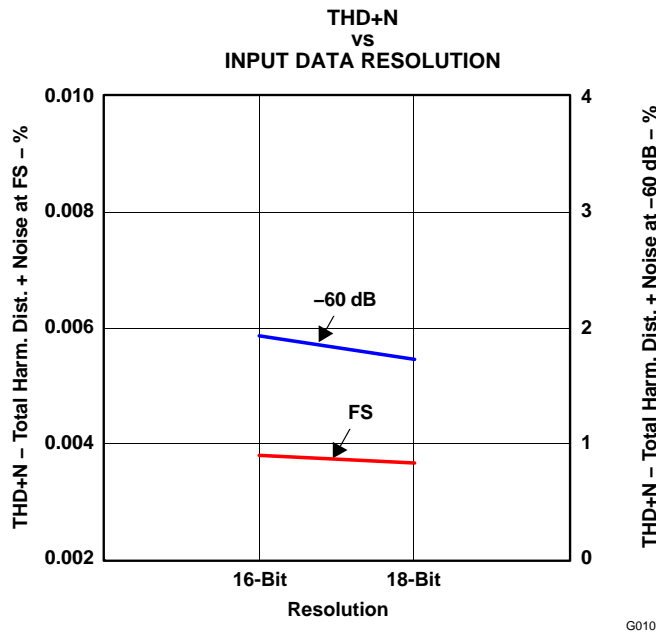


Figure 10.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

DECIMATION FILTER

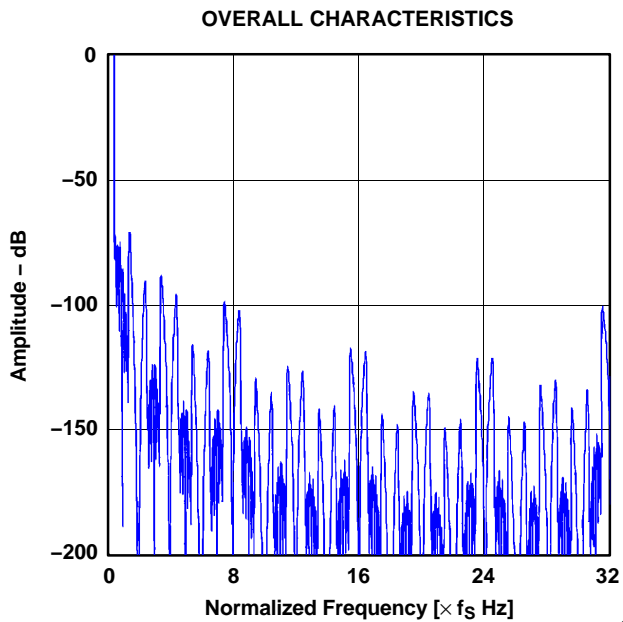


Figure 11.

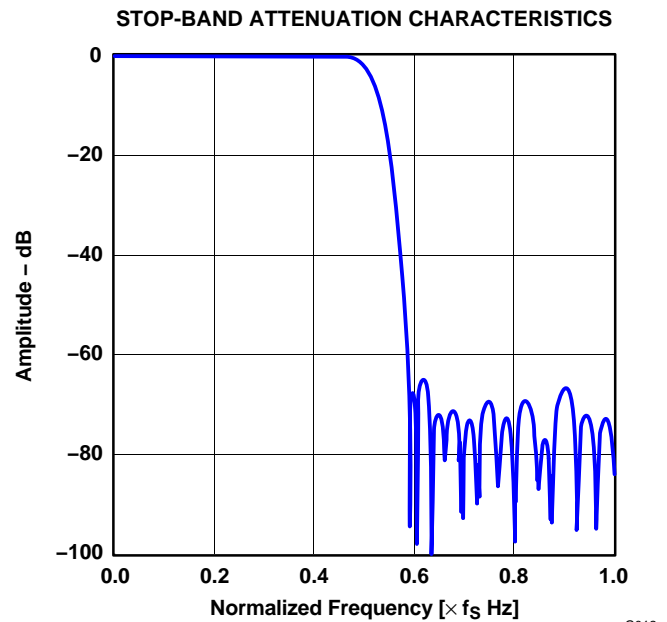


Figure 12.

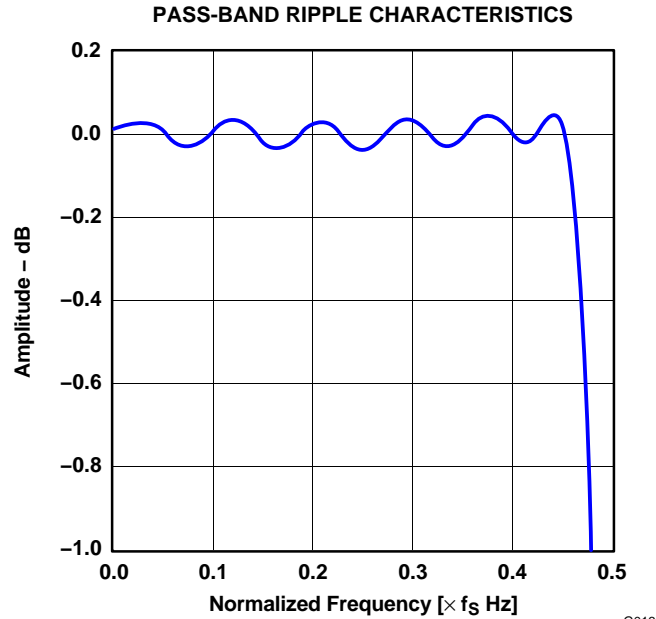


Figure 13.

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (ADCs) (continued)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, and $\text{SYSCLK} = 384 f_S$, unless otherwise noted

HIGH-PASS FILTER

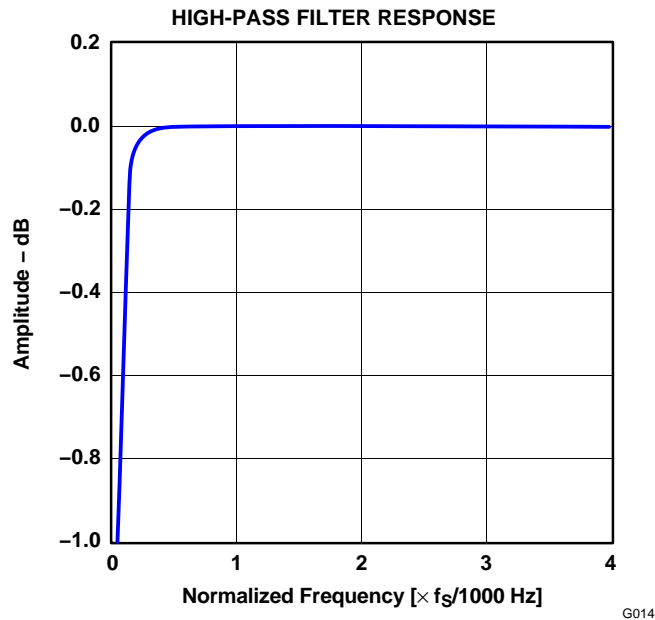


Figure 14.

ANTI_ALIASING FILTER

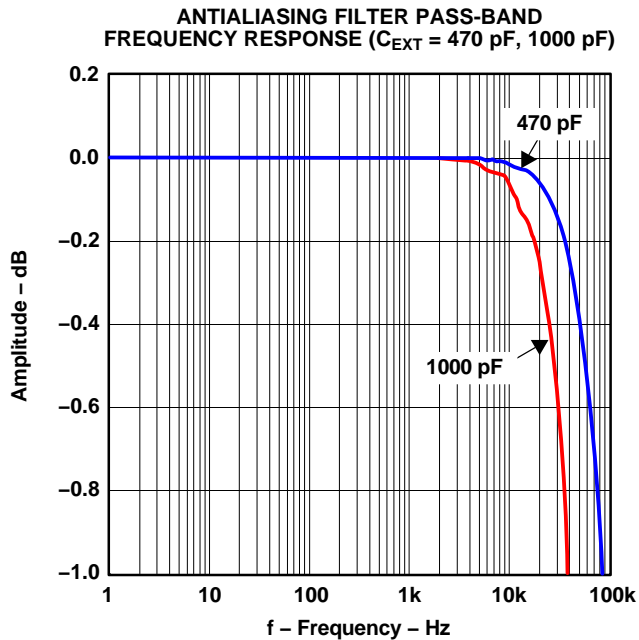


Figure 15.

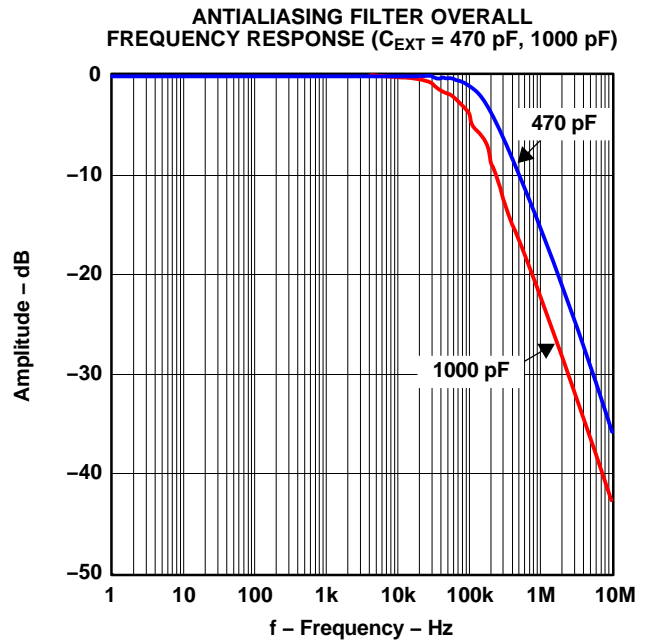
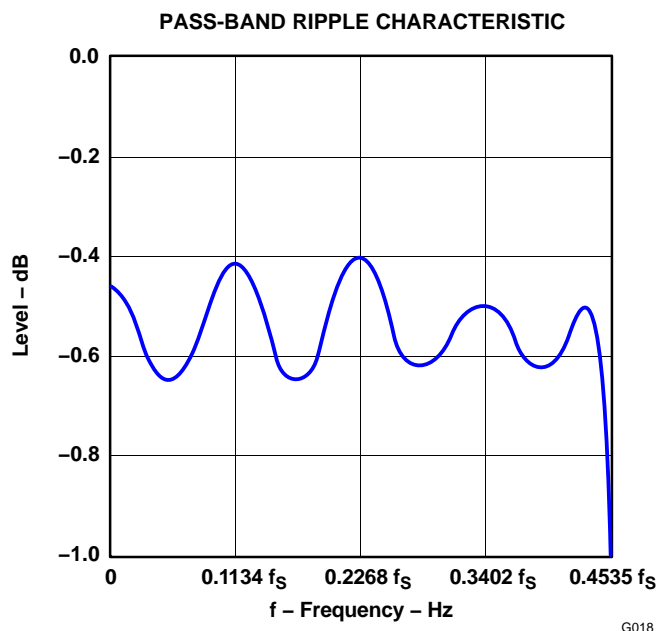
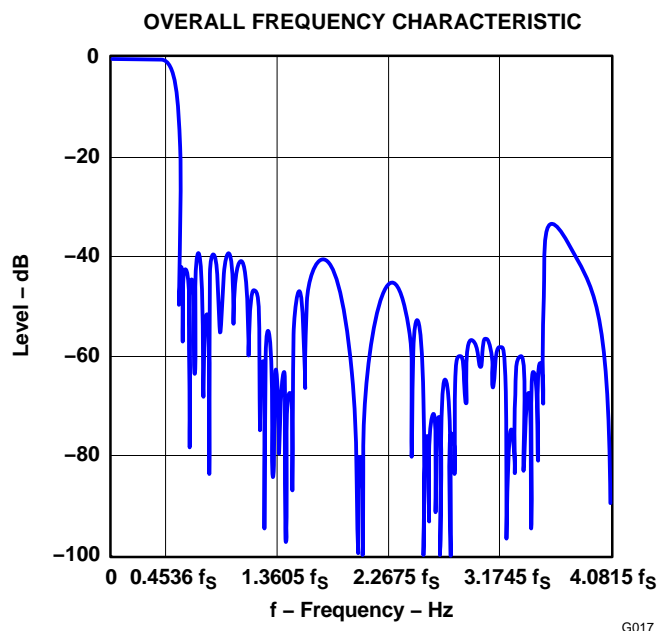


Figure 16.

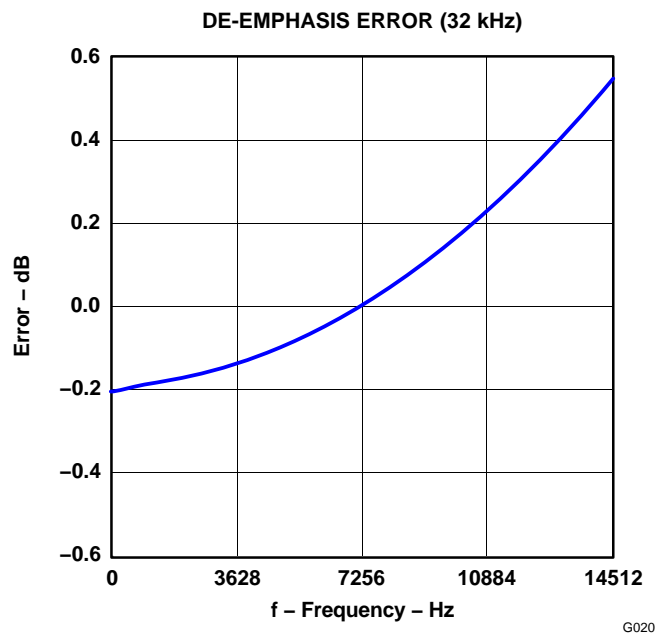
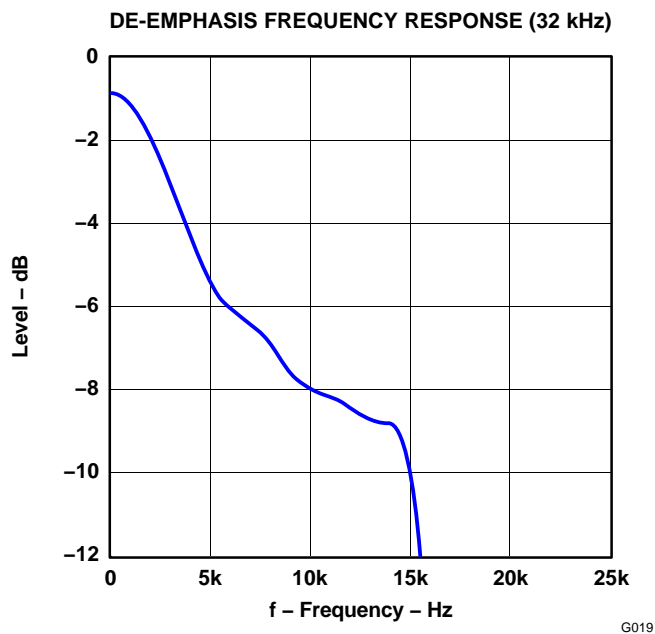
TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs)

All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

DIGITAL FILTER



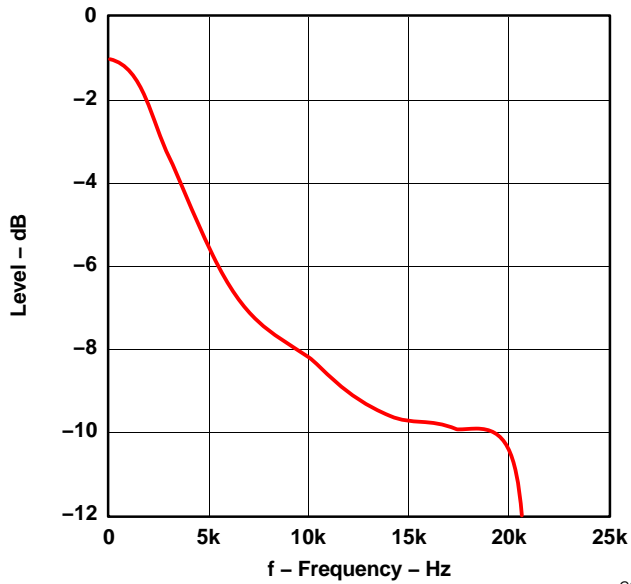
DE-EMPHASIS FILTER



TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

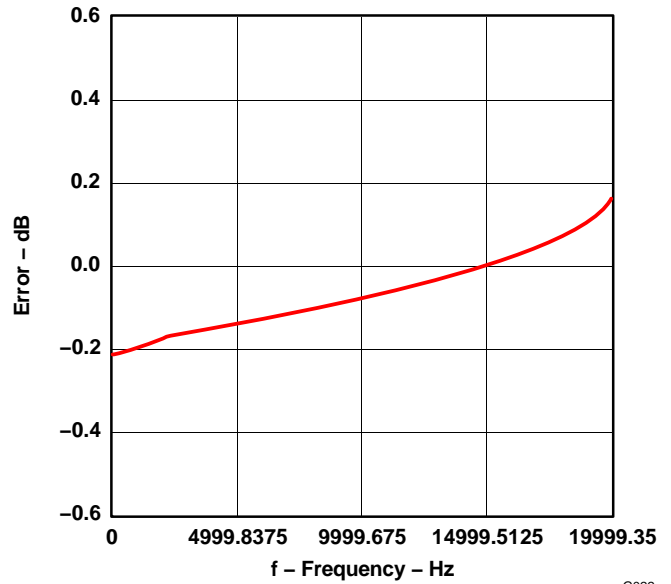
All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

DE-EMPHASIS FREQUENCY RESPONSE (44.1 kHz)



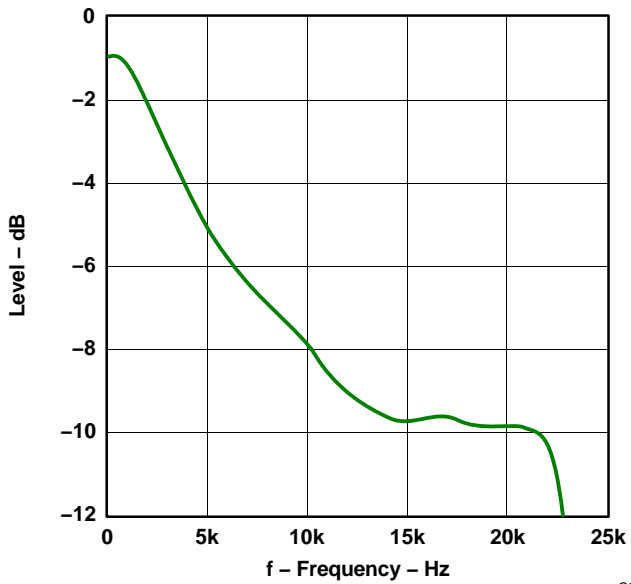
G021

DE-EMPHASIS ERROR (44.1 kHz)



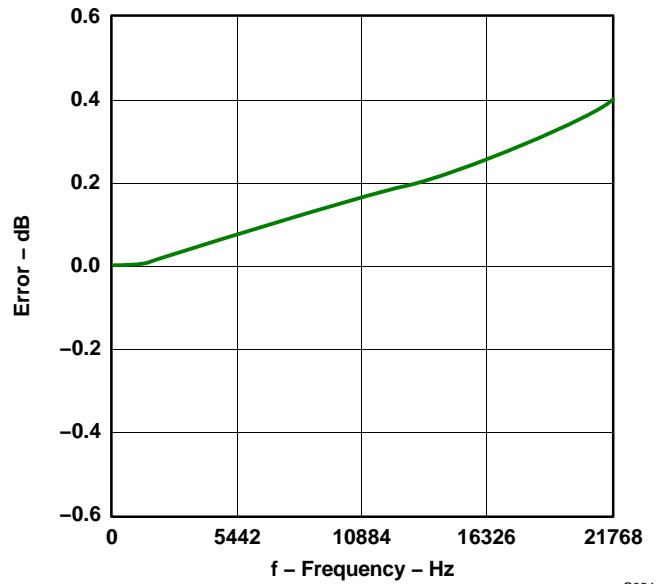
G022

DE-EMPHASIS FREQUENCY RESPONSE (48 kHz)



G023

DE-EMPHASIS ERROR (48 kHz)



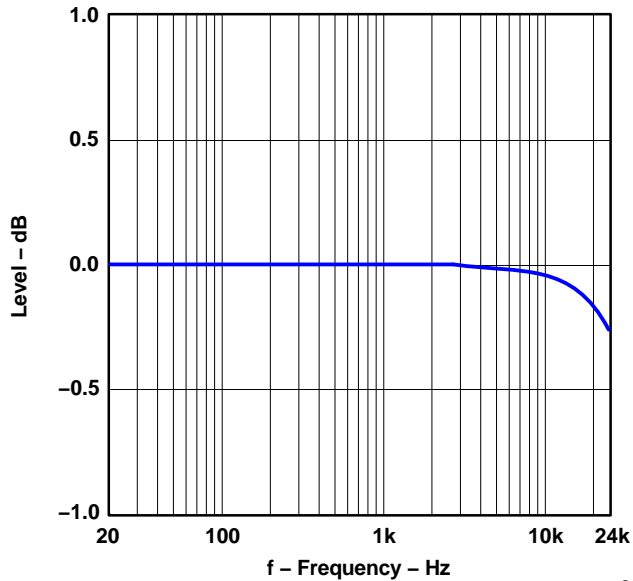
G024

TYPICAL PERFORMANCE CURVES OF INTERNAL FILTERS (DACs) (continued)

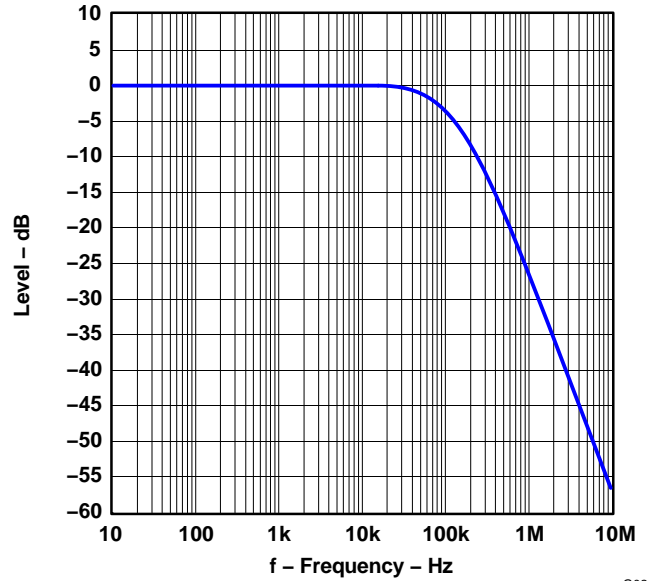
All specifications at $T_A = 25^\circ\text{C}$, $V_{CC} = V_{DD} = 5\text{ V}$, and $\text{SYSCLK} = 384\text{ f}_S$, unless otherwise noted

ANALOG LOW-PASS FILTER

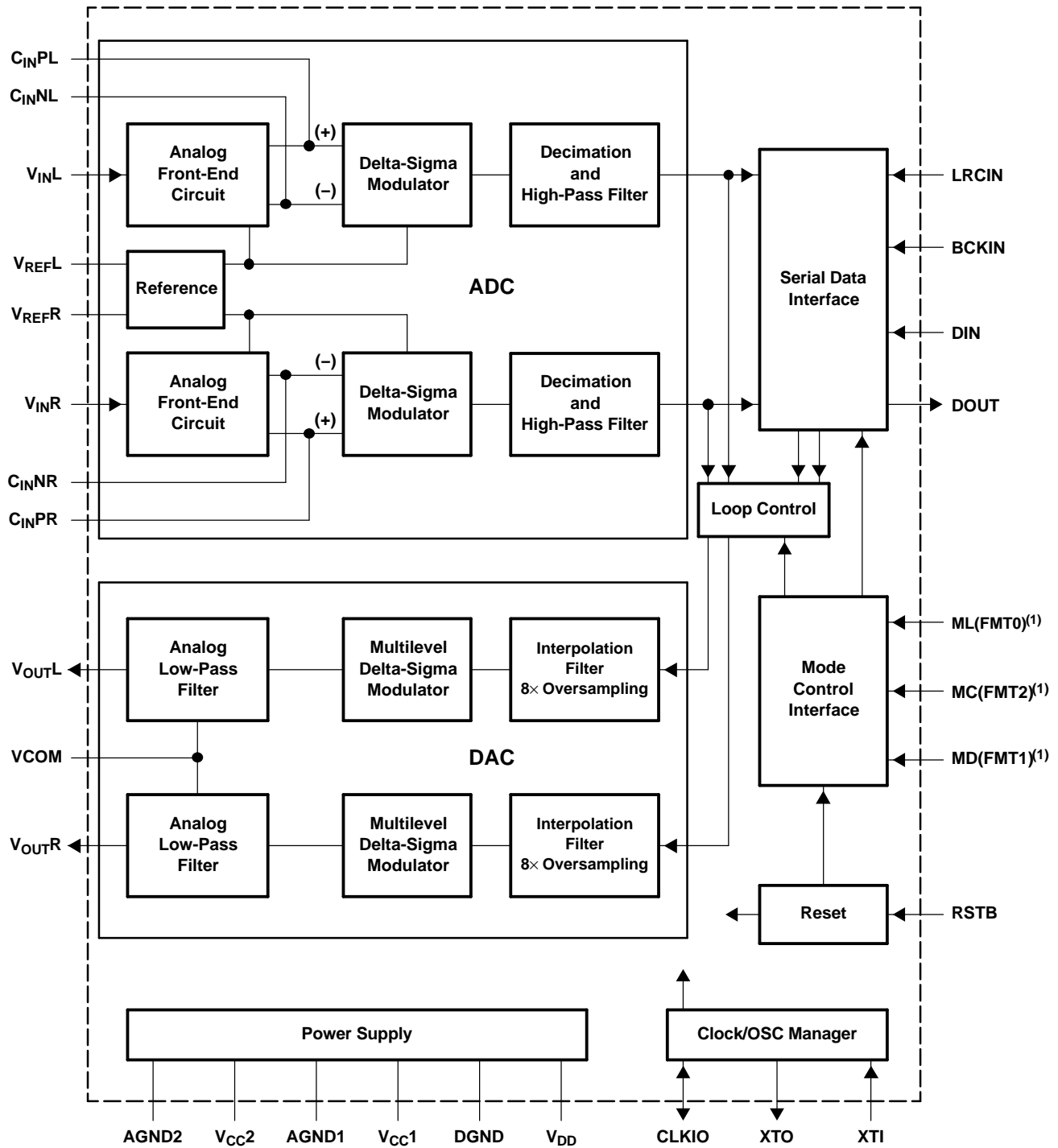
INTERNAL ANALOG FILTER FREQUENCY RESPONSE
(20 Hz–24 kHz, EXPANDED SCALE)



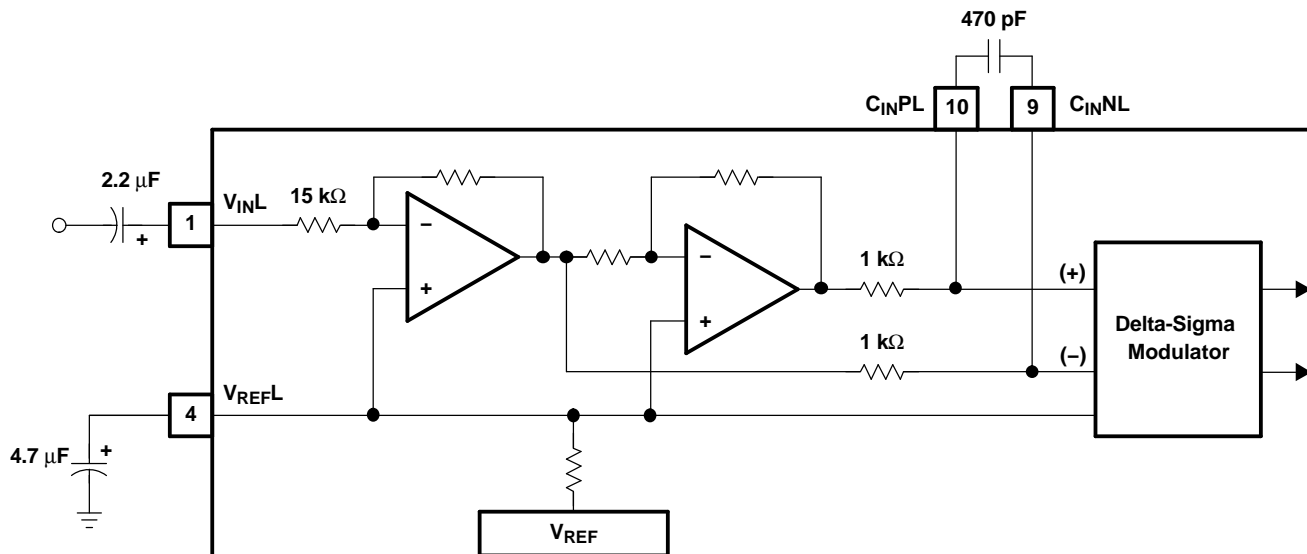
INTERNAL ANALOG FILTER FREQUENCY RESPONSE
(10 Hz–10 MHz)



Block Diagram



B0004-05



S0011-04

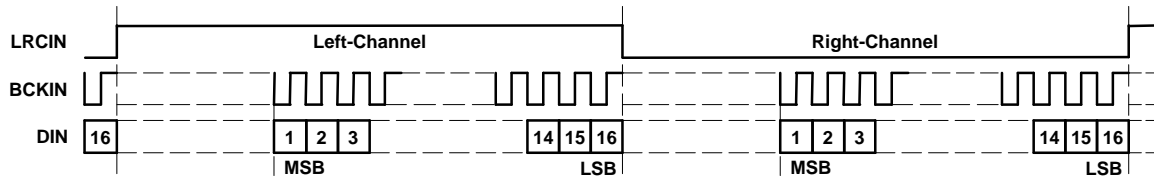
Figure 17. Analog Front-End (Single-Channel)

PCM AUDIO INTERFACE

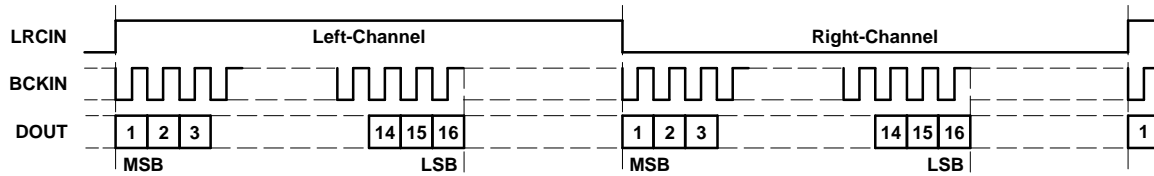
The four-wire digital audio interface for the PCM3000/3001 is on LRCIN (pin 16), BCKIN (pin 17), DIN (pin 18), and DOUT (pin 19). The PCM3000/3001 can operate with seven different data formats. For the PCM3000, these formats are selected through program register 3 in the software mode. For the PCM3001, data formats are selected by pin-strapping the three format pins. Figure 18, Figure 19, Figure 20 and Figure 21 illustrate the audio data input/output format. Figure 22 shows the audio data input/output timing. The PCM3000/3001 can accept 32, 48, or 64 bit clocks (BCKIN) during one clock of LRCIN. Only formats 0, 2, and 6 can be selected when 32 bit clocks/LRCIN are applied.

FORMAT 0: FMT[2:0] = 000

DAC: 16-Bit, MSB-First, Right-Justified

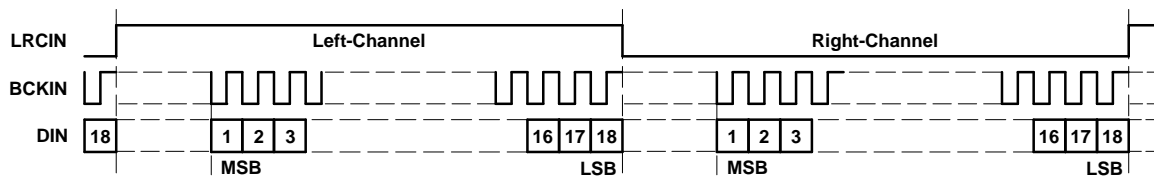


ADC: 16-Bit, MSB-First, Left-Justified

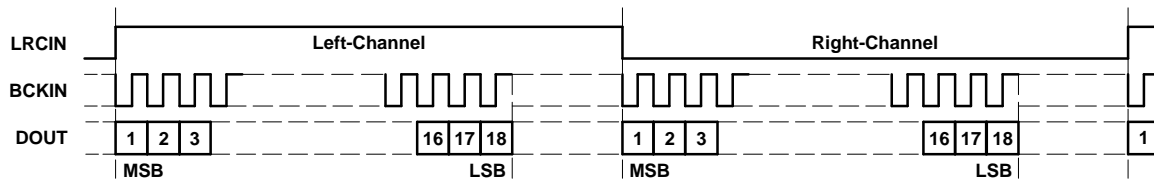


FORMAT 1: FMT[2:0] = 001

DAC: 18-Bit, MSB-First, Right-Justified



ADC: 18-Bit, MSB-First, Left-Justified

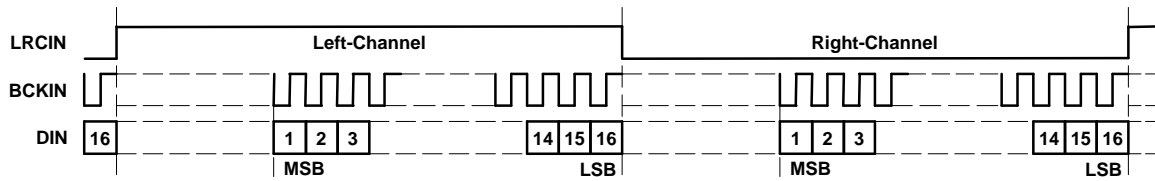


T0016-07

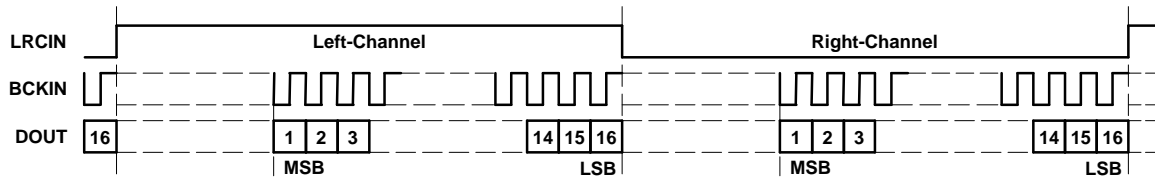
Figure 18. Audio Data Input/Output Format (Formats 0 and 1)

FORMAT 2: FMT[2:0] = 010

DAC: 16-Bit, MSB-First, Right-Justified

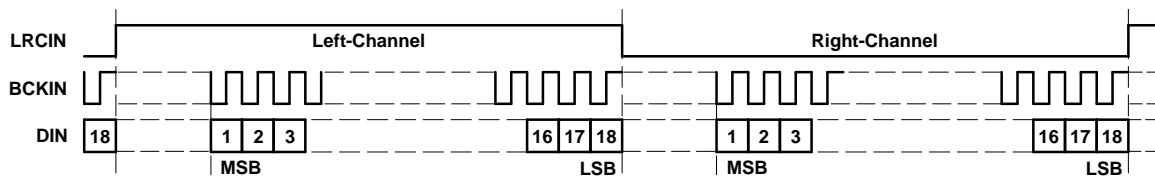


ADC: 16-Bit, MSB-First, Right-Justified

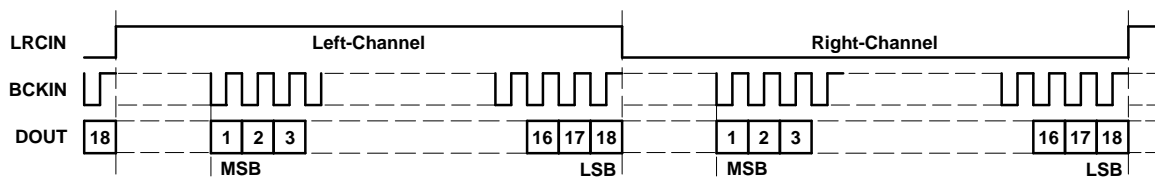


FORMAT 3: FMT[2:0] = 011

DAC: 18-Bit, MSB-First, Right-Justified



ADC: 18-Bit, MSB-First, Right-Justified

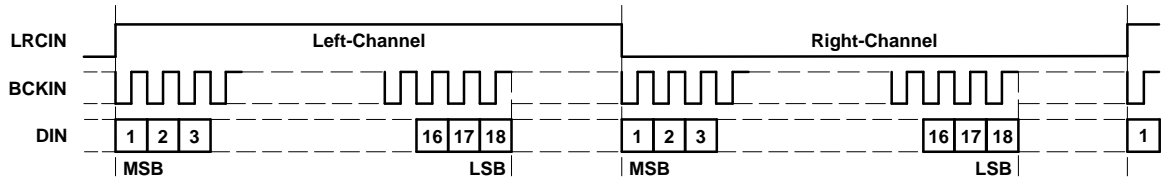


T0016-08

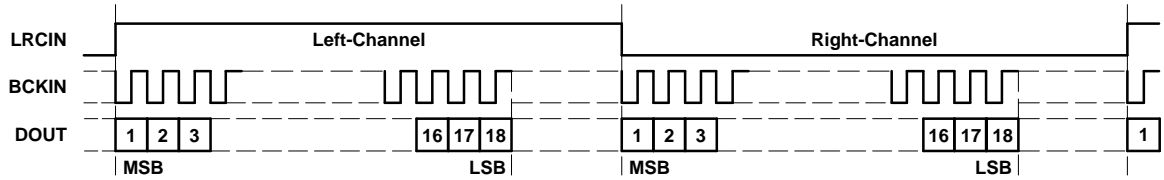
Figure 19. Audio Data Input/Output Format (Formats 2 and 3)

FORMAT 4: FMT[2:0] = 100

DAC: 18-Bit, MSB-First, Left-Justified

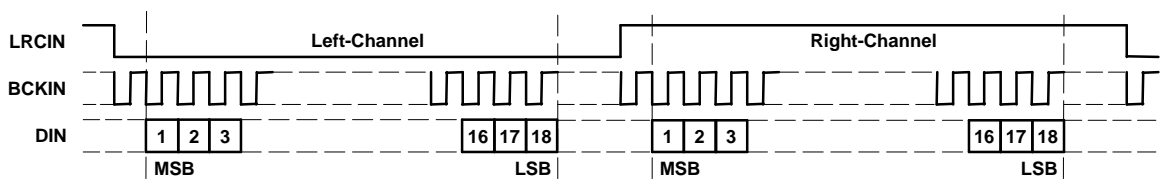


ADC: 18-Bit, MSB-First, Left-Justified

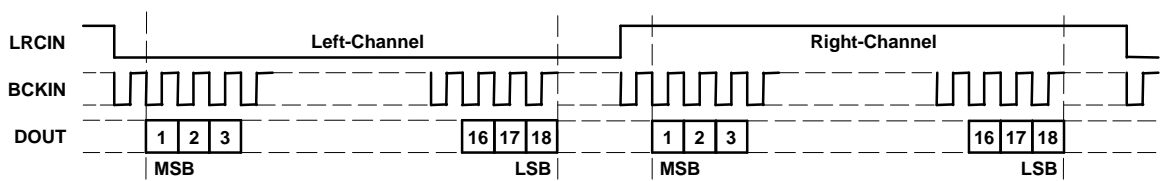


FORMAT 5: FMT[2:0] = 101

DAC: 18-Bit, MSB-First, I²S



ADC: 18-Bit, MSB-First, I²S

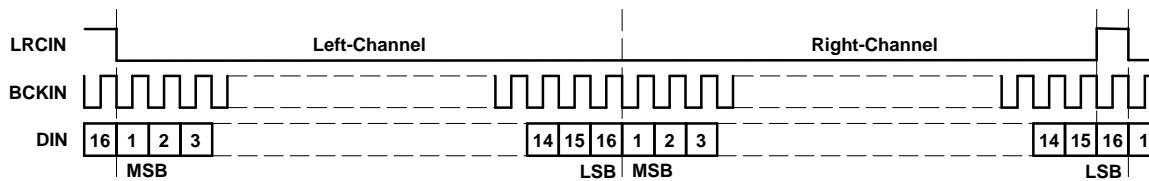


T0016-09

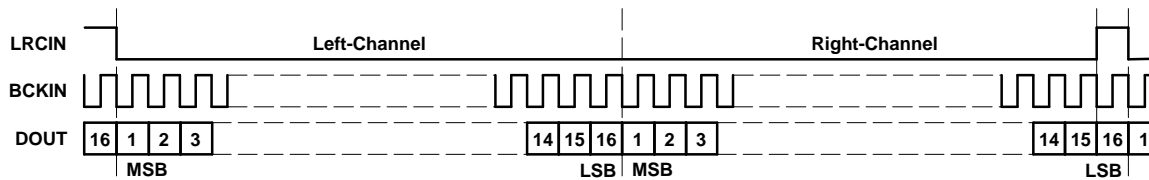
Figure 20. Audio Data Input/Output Format (Formats 4 and 5)

FORMAT 6: FMT[2:0] = 110

DAC: 16-Bit, MSB-First, DSP-Frame

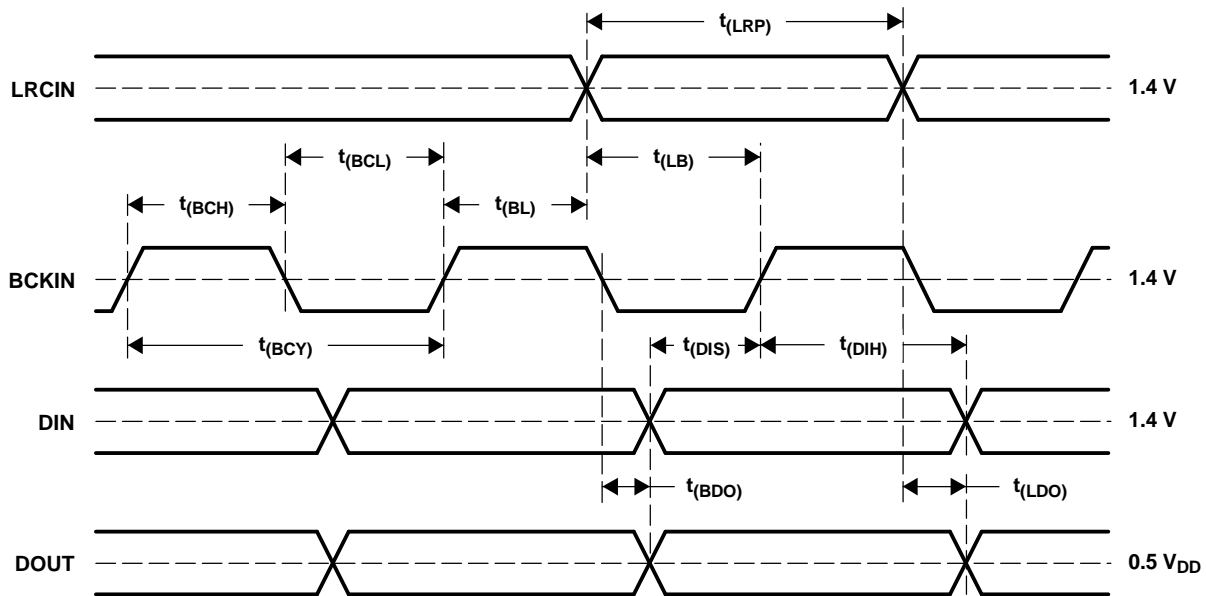


ADC: 16-Bit, MSB-First, DSP-Frame



T0016-10

Figure 21. Audio Data Input/Output Format (Format 6)



T0021-02

| | | |
|---------------------------------------|--------------|-------------------|
| BCKIN pulse cycle time | $t_{(BCY)}$ | 300 ns (min) |
| BCKIN pulse duration, HIGH | $t_{(BCH)}$ | 120 ns (min) |
| BCKIN pulse duration, LOW | $t_{(BCL)}$ | 120 ns (min) |
| BCKIN rising edge to LRCIN edge | $t_{(BL)}$ | 40 ns (min) |
| LRCIN edge to BCKIN rising edge | $t_{(LB)}$ | 40 ns (min) |
| LRCIN pulse duration | $t_{(LRP)}$ | $t_{(BCY)}$ (min) |
| DIN setup time | $t_{(DIS)}$ | 40 ns (min) |
| DIN hold time | $t_{(DIH)}$ | 40 ns (min) |
| DOUT delay time to BCKIN falling edge | $t_{(BDO)}$ | 40 ns (max) |
| DOUT delay time to LRCIN edge | $t_{(LDO)}$ | 40 ns (max) |
| Rising time of all signals | $t_{(RISE)}$ | 20 ns (max) |
| Falling time of all signals | $t_{(FALL)}$ | 20 ns (max) |

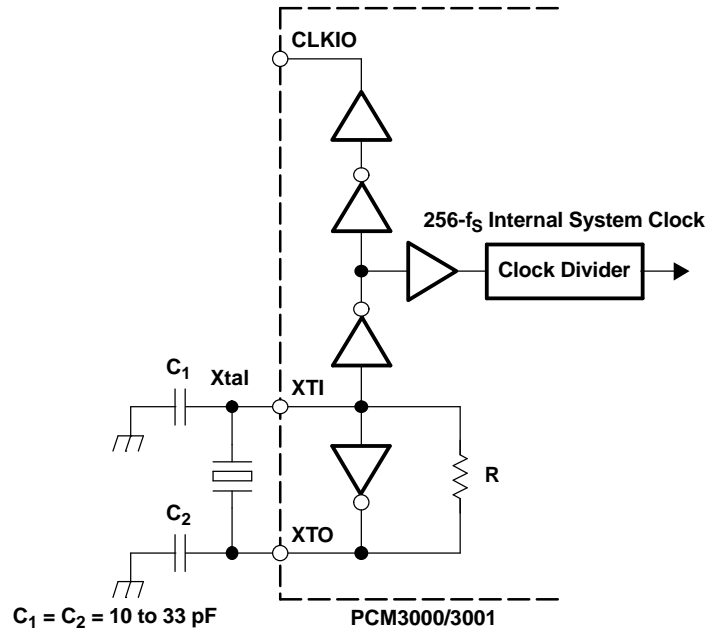
Figure 22. Audio Data Input/Output Timing

SYSTEM CLOCK

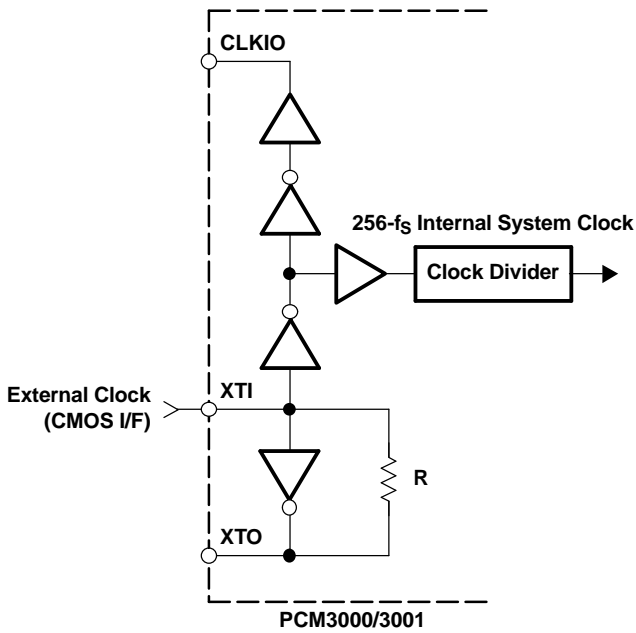
The system clock for the PCM3000/3001 must be either $256 f_s$, $384 f_s$, or $512 f_s$, where f_s is the audio sampling frequency. The system clock can be either a crystal oscillator placed between XTI (pin 20) and XTO (pin 21), or an external clock input. If an external clock is used, the clock is provided to either XTI or CLKIO (pin 22), and XTO is open. The PCM3000/3001 has an XTI clock detection circuit which senses if an XTI clock is operating. When the external clock is delivered to XTI, CLKIO is a buffered output of XTI. When XTI is connected to ground, the external clock must be tied to CLKIO. For best performance, the external-clock-input-2 circuit in Figure 23 is recommended.

The PCM3000/3001 also has a system-clock detection circuit which automatically senses if the system clock is operating at $256 f_s$, $384 f_s$, or $512 f_s$. When a $384 f_s$ or $512 f_s$ system clock is used, the clock is divided into $256 f_s$ automatically. The $256 f_s$ clock is used to operate the digital filters and the modulators.

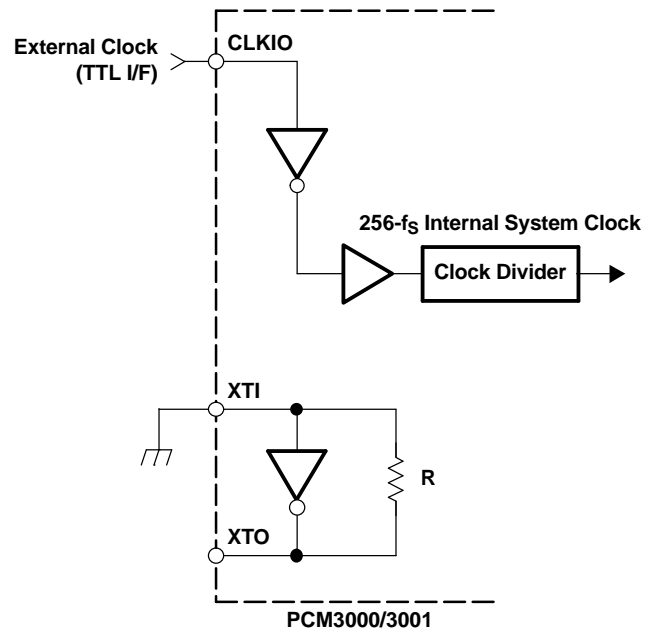
Table 1 lists the relationship of typical sampling frequencies and system clock frequencies, and Figure 23 and Figure 24 illustrate the typical system clock connections and external system clock timing.



Crystal Resonator Connection (Xtal must be fundamental mode, parallel resonant)



External Clock Input 1 : (XTO is open)



External Clock Input 2 : (XTO is open)

S0017-01

Figure 23. System Clock Connections

Table 1. System Clock Frequencies

| SAMPLING RATE FREQUENCY (kHz) | SYSTEM CLOCK FREQUENCY (MHz) | | |
|-------------------------------|------------------------------|--------------------|--------------------|
| | 256 f _S | 384 f _S | 512 f _S |
| 32 | 8.1920 | 12.2880 | 16.3840 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 |
| 48 | 12.2880 | 18.4320 | 24.5760 |

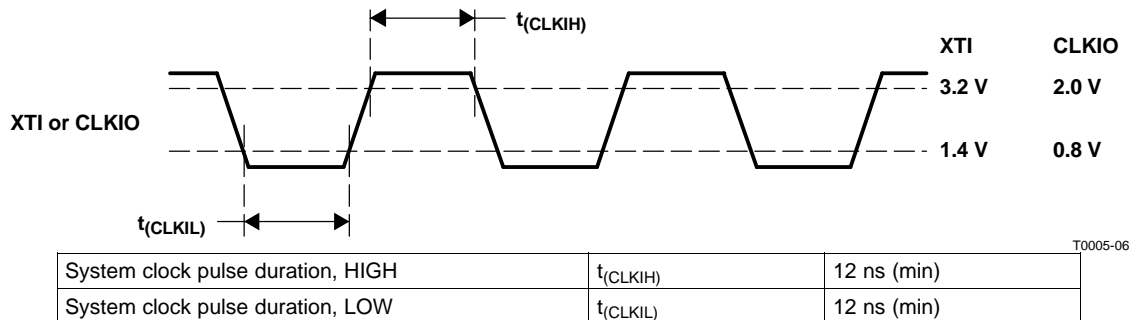


Figure 24. External System Clock Timing

POWER-ON RESET

The PCM3000/3001 has internal power-on reset circuitry. Power-on reset occurs when the system clock (XTI or CLKIO) is active and V_{DD} > 4 V. For the PCM3001, the system clock must complete a minimum of 3 complete cycles prior to V_{DD} > 4 V to ensure proper reset operation. The initialization sequence requires 1024 system cycles for completion, as shown in Figure 25. Figure 26 shows the state of the DAC and ADC outputs during and after the reset sequence.

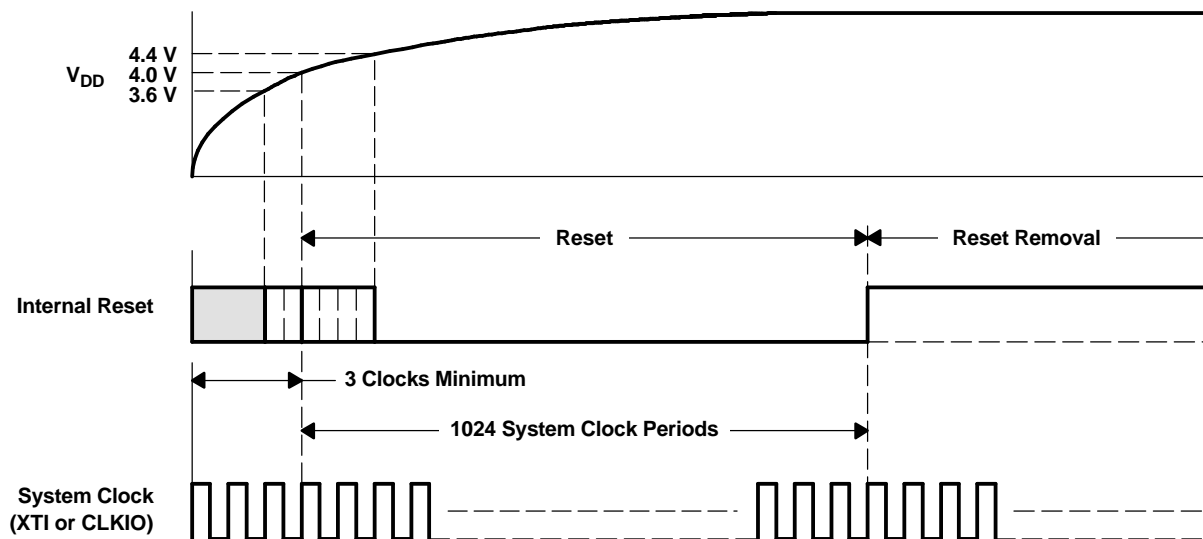
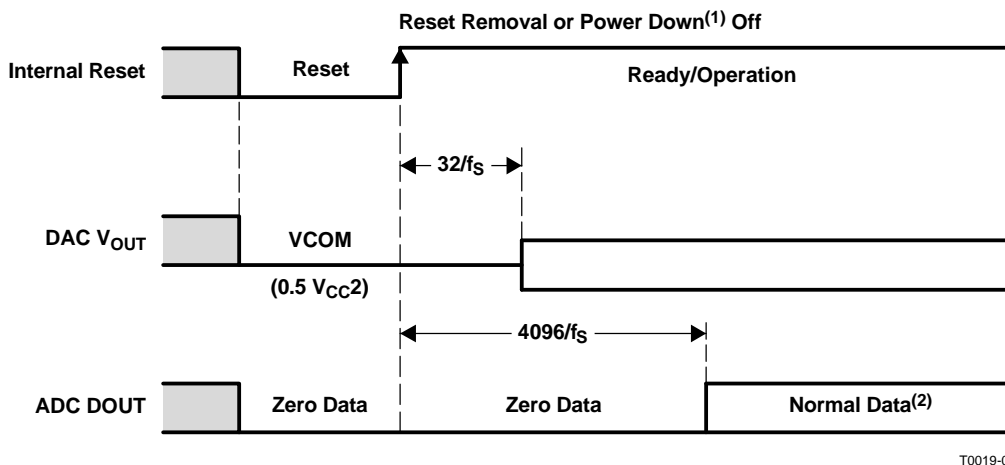


Figure 25. Internal Power-On Reset Timing



- (1) Power down is for PCM3000 only.
- (2) The HPF transient response (exponentially attenuated signal from $\pm 1.5\%$ dc with 200-ms time constant) appears initially.

Figure 26. DAC Output and ADC Output for Reset and Power Down

EXTERNAL RESET

The PCM3000/3001 includes a reset input, RSTB (pin 28). As shown in Figure 27, the external reset signal must drive RSTB low for a minimum of 40 nanoseconds while the system clock is active in order to initiate the reset sequence. Initialization starts on the rising edge of RSTB, and requires 1024 system clock cycles for completion. Figure 26 shows the state of the DAC and ADC outputs during and after the reset sequence.

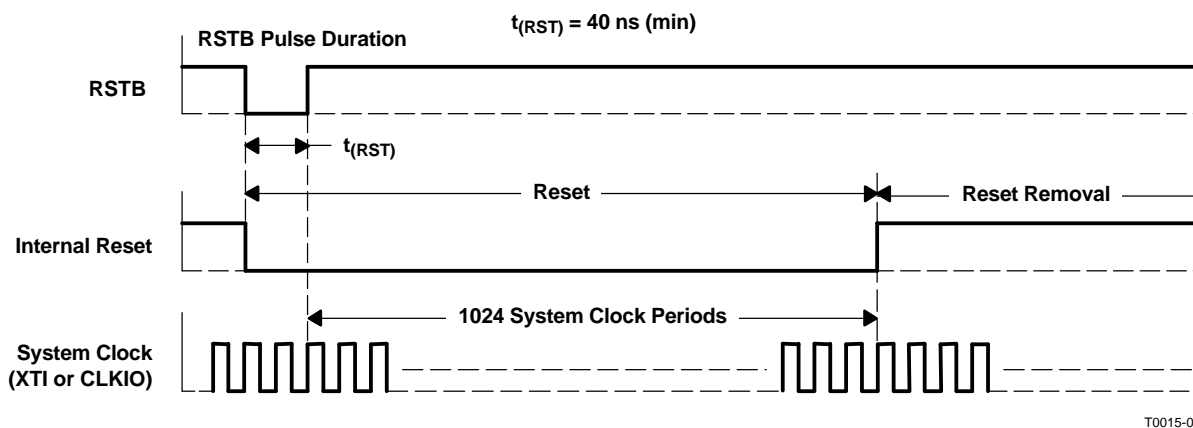
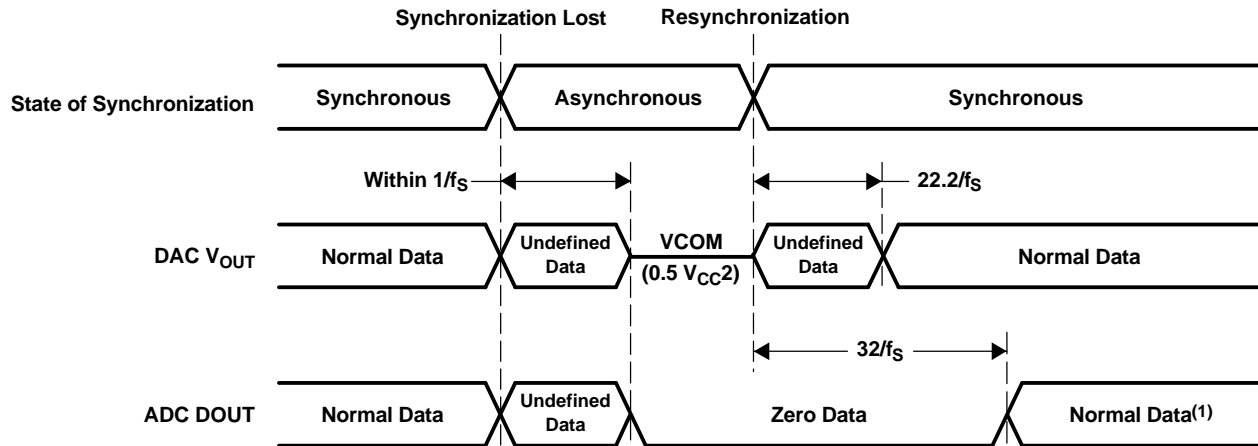


Figure 27. External Forced-Reset Timing

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

The PCM3000/3001 operates with LRCIN synchronized to the system clock. The codec does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization of LRCIN and the system clock. If the synchronization between the system clock and LRCIN changes more than 6 bit clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC stops within $1/f_s$, and the analog output is forced to bipolar zero ($V_{CC2}/2$) until the system clock is resynchronized to LRCIN. Internal operation of the ADC also stops within $1/f_s$, and the digital output codes are set to bipolar zero until resynchronization occurs. If LRCIN is synchronized within 5 or fewer bit clocks to the system clock, operation remains normal.

Figure 28 illustrates the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($< 1/f_s$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which cause output noise.



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- (1) The HPF transient response (exponentially attenuated signal from $\pm 1.5\%$ dc with 200-ms time constant) appears initially.

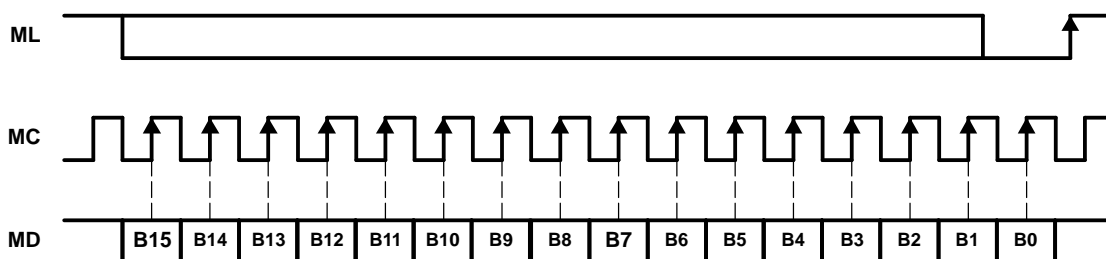
Figure 28. DAC Output and ADC Output For Loss of Synchronization

OPERATIONAL CONTROL

The PCM3000 can be controlled in the software mode with a three-wire serial interface on MC (pin 25), MD (pin 26), and ML (pin 27). Table 2 indicates selectable functions, and Figure 29 and Figure 30 illustrate control data input format and timing. The PCM3001 only allows for control of data format.

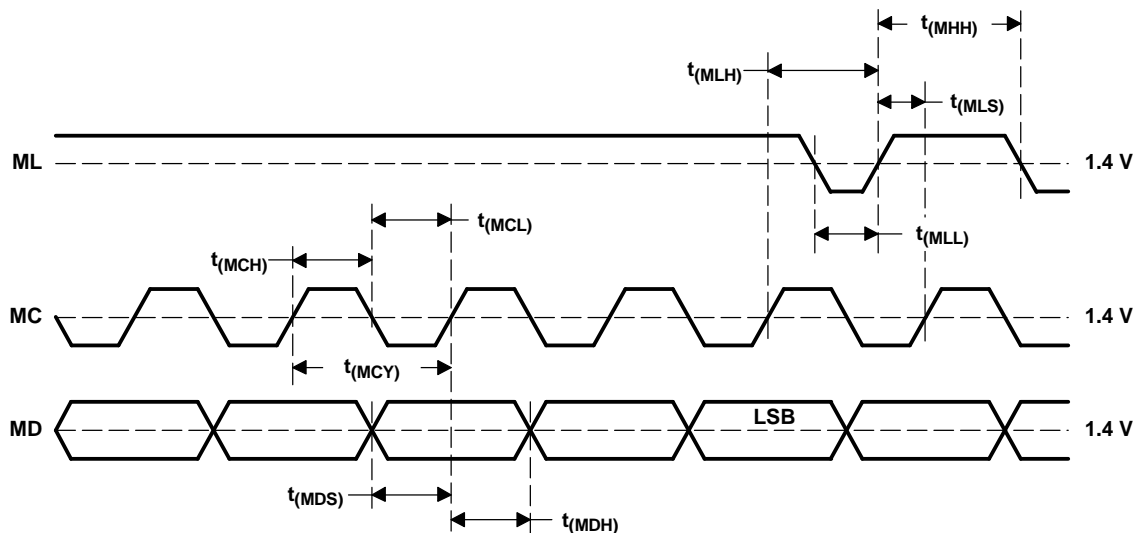
Table 2. Selectable Functions

| FUNCTION | ADC/DAC | DEFAULT (PCM3000) |
|---|---------|---|
| Audio data format (7 selectable formats) | ADC/DAC | DAC: 16-bit, MSB-first, right-justified ADC: 16-bit, MSB-first, left-justified |
| LRCIN polarity | ADC/DAC | Left/right = high/low |
| Loopback control | ADC/DAC | OFF |
| Left-channel attenuation | DAC | 0 dB |
| Right-channel attenuation | DAC | 0 dB |
| Attenuation control | DAC | Left channel and right channel = individual control |
| Infinite zero detection | DAC | OFF |
| DAC output control | DAC | Output enabled |
| Soft mute control | DAC | OFF |
| De-emphasis (OFF, 32 kHz, 44.1 kHz, 48 kHz) | DAC | OFF |
| Power-down control | ADC | OFF |
| High-pass filter operation | ADC | ON |



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Figure 29. Control Data Input Format



| | | |
|--|-------------|---------------------------------------|
| MC pulse cycle time | $t_{(MCY)}$ | 100 ns (min) |
| MC pulse duration, LOW | $t_{(MCL)}$ | 40 ns (min) |
| MC pulse duration, HIGH | $t_{(MCH)}$ | 40 ns (min) |
| MD setup time | $t_{(MDS)}$ | 40 ns (min) |
| MD hold time | $t_{(MDH)}$ | 40 ns (min) |
| ML low-level time | $t_{(MLL)}$ | 40 ns + 1 SYSCLK ⁽¹⁾ (min) |
| ML high-level time | $t_{(MHH)}$ | 40 ns + 1 SYSCLK ⁽¹⁾ (min) |
| ML setup time ⁽²⁾ | $t_{(MLS)}$ | 40 ns (min) |
| ML hold time ⁽³⁾ | $t_{(MLH)}$ | 40 ns (min) |
| SYSCLK (period): 1/256 f_s or 1/384 f_s or 1/512 f_s | | |

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- (1) SYSCLK: system clock cycle
 (2) ML rising edge to the next MC rising edge
 (3) MC rising edge for LSB-to-ML rising edge

Figure 30. Control Data Input Timing

MAPPING OF PROGRAM REGISTERS

| | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|------------|-----|-----|-----|-----|-----|-----|----|------|------|-----|-----|------|------|------|------|-----|
| REGISTER 0 | res | res | res | res | res | A1 | A0 | LDL | AL7 | AL6 | AL5 | AL4 | AL3 | AL2 | AL1 | AL0 |
| REGISTER 1 | res | res | res | res | res | A1 | A0 | LDR | AR7 | AR6 | AR5 | AR4 | AR3 | AR2 | AR1 | AR0 |
| REGISTER 2 | res | res | res | res | res | A1 | A0 | PDWN | BYPS | res | ATC | IZD | OUT | DEM1 | DEM0 | MUT |
| REGISTER 3 | res | res | res | res | res | A1 | A0 | res | res | res | LOP | FMT2 | FMT1 | FMT0 | LRP | res |

NOTE: res indicates a reserved bit, which should be set to 0.

PROGRAM REGISTER (PCM3000)

The software mode allows the user to control special functions. The PCM3000 special functions are controlled using four program registers which are each 16 bits long. There are four distinct registers, with bits 9 and 10 determining which register is in use. Table 3 describes the functions of the four registers.

Table 3. Functions of the Registers

| REGISTER NAME | REGISTER BIT(S) | BIT NAME | DESCRIPTION |
|---------------|-----------------|----------|---|
| Register 0 | 15–11 | res | Reserved, should be set to 0 |
| | 10–9 | A[1:0] | Register address 00 |
| | 8 | LDL | DAC attenuation data load control for Lch |
| | 7–0 | AL[7:0] | DAC attenuation data for Lch |
| Register 1 | 15–11 | res | Reserved, should be set to 0 |
| | 10–9 | A[1:0] | Register address 01 |
| | 8 | LDR | DAC attenuation data load control for Rch |
| | 7–0 | AR[7:0] | DAC attenuation data for Rch |
| Register 2 | 15–11 | res | Reserved, should be set to 0 |
| | 10–9 | A[1:0] | Register address 10 |
| | 8 | PDWN | ADC power-down control |
| | 7 | BYPS | ADC high-pass filter bypass control |
| | 6 | res | Reserved, should be set to 0 |
| | 5 | ATC | DAC attenuation data mode control |
| | 4 | IZD | DAC infinite zero detection circuit control |
| | 3 | OUT | DAC output enable control |
| | 2–1 | DEM[1:0] | DAC de-emphasis control |
| | 0 | MUT | DAC Lch and Rch soft mute control |
| Register 3 | 15–11 | res | Reserved, should be set to 0 |
| | 10–9 | A[1:0] | Register address 11 |
| | 8–6 | res | Reserved, should be set to 0 |
| | 5 | LOP | ADC/DAC analog loopback control |
| | 4–2 | FMT[2:0] | ADC/DAC audio data format selection |
| | 1 | LRP | ADC/DAC polarity of LR-clock selection |
| | 0 | res | Reserved, should be set to 0 |

PROGRAM REGISTER 0

res: Bits 15:11 – Reserved
These bits are reserved and should be set to 0.

A[1:0]: Bits 10:9 – Register Address
These bits define the address for REGISTER 0:

| A1 | A0 | |
|----|----|------------|
| 0 | 0 | Register 0 |

LDL: Bit 8 – DAC Attenuation Data Load Control for Left Channel
This bit is used to simultaneously set the analog outputs of the left and right channels. The output level is controlled by AL[7:0] attenuation data when this bit is set to 1. When set to 0, the new attenuation data is stored into a register, and the output level remains at the previous attenuation level. The LDR bit in REGISTER 1 has the equivalent function as LDL. When either LDL or LDR is set to 1, the output levels of the left and right channels are simultaneously controlled.

AL[7:0]: Bits 7:0 – DAC Attenuation Data for Left Channel

AL7 and AL0 are the MSB and LSB, respectively. The attenuation level (ATT) is given by

$$ATT = 20 \times \log_{10} (AL[7:0]/256) \text{ (dB), except } AL[7:0] = FFh$$

| AL[7:0] | ATTENUATION LEVEL |
|---------|-------------------|
| 00h | –∞ dB (mute) |
| 01h | –48.16 dB |
| : | : |
| FEh | –0.07 dB |
| FFh | 0 dB (default) |

PROGRAM REGISTER 1

res: Bits 15:11 – Reserved

These bits are reserved and should be set to 0.

A[1:0]: Bits 10:9 – Register Address

These bits define the address for REGISTER 1.

| A1 | A0 | |
|----|----|------------|
| 0 | 1 | Register 1 |

LDR: Bit 8 – DAC Attenuation Data Load Control for Right Channel

This bit is used to simultaneously set the analog outputs of the left and right channels. The output level is controlled by AR[7:0] attenuation data when this bit is set to 1. When set to 0, the new attenuation data is stored into a register, and the output level remains at the previous attenuation level. The LDL bit in REGISTER 0 has the equivalent function as LDR. When either LDL or LDR is set to 1, the output levels of the left and right channels are simultaneously controlled.

AR[7:0]: Bits 7:0 – DAC Attenuation Data for Right Channel

AR7 and AR0 are the MSB and LSB, respectively. The attenuation level (ATT) is given by

$$ATT = 20 \times \log_{10} (AR[7:0]/256) \text{ (dB), except } AR[7:0] = FFh$$

| AR[7:0] | ATTENUATION LEVEL |
|---------|-------------------|
| 00h | –∞ dB (mute) |
| 01h | –48.16 dB |
| : | : |
| FEh | –0.07 dB |
| FFh | 0 dB (default) |

PROGRAM REGISTER 2

res: Bits 15:11 – Reserved

These bits are reserved and should be set to 0.

A[1:0]: Bits 10:9 – Register Address

These bits define the address for REGISTER 2:

| A1 | A0 | |
|----|----|------------|
| 1 | 0 | Register 2 |

PDWN: Bit 8 – ADC Power-Down Control

This bit places the ADC section in a power-down mode, forcing the output data to all zeroes. This has no effect on the DAC section or the contents of the mode registers.

| PDWN | |
|------|------------------------------------|
| 0 | Power-down mode disabled (default) |
| 1 | Power-down mode enabled |

BYPS: Bit 7 – ADC High-Pass Filter Bypass Control

This bit enables or disables the high-pass filter for the ADC.

| BYPS | |
|------|--------------------------------------|
| 0 | High-pass filter enabled (default) |
| 1 | High-pass filter disabled (bypassed) |

res: Bit 6 – Reserved

This bit is reserved and should be set to 0.

ATC: Bit 5 – DAC Attenuation Data Mode Control

When set to 1, the REGISTER 0 attenuation data is used for both DAC channels. In this case, the REGISTER 1 attenuation data is ignored.

| ATC | |
|-----|---|
| 0 | Individual channel attenuation data control (default) |
| 1 | Common channel attenuation data control |

IZD: Bit 4 – DAC Infinite Zero Detection Circuit Control

This bit enables the infinite zero detection circuit in the PCM3000. When enabled, this circuit disconnects the analog output amplifier from the delta-sigma DAC when the input is continuously zero for 65,536 consecutive cycles of BCKIN.

| IZD | |
|-----|--|
| 0 | Infinite zero detection disabled (default) |
| 1 | Infinite zero detection enabled |

OUT: Bit 3 – DAC Output Enable Control

When set to 1, the outputs are forced to $V_{CC}/2$ (bipolar zero). In this case, all registers in the PCM3000 hold the present data. Therefore, when set to 0, the outputs return to the previous programmed state.

| OUT | |
|-----|--|
| 0 | DAC outputs enabled (default normal operation) |
| 1 | DAC outputs disabled (forced to BPZ) |

DEM[1:0]: Bits 2:1 – DAC De-Emphasis Control

These bits select the de-emphasis mode as shown.

| DEM1 | DEM0 | |
|------|------|---------------------------|
| 0 | 0 | De-emphasis OFF (default) |
| 0 | 1 | De-emphasis 48 kHz ON |
| 1 | 0 | De-emphasis 44.1 kHz ON |
| 1 | 1 | De-emphasis 32 kHz ON |

MUT: Bit 0 – DAC Soft Mute Control

When set to 1, both left- and right-channel DAC outputs are muted at the same time. This muting is done by attenuating the data in the digital filter, so that there is no audible click noise when soft mute is turned on.

| MUT | |
|-----|-------------------------|
| 0 | Mute disabled (default) |
| 1 | Mute enabled |

PROGRAM REGISTER 3

res: Bits 15:11 – Reserved
These bits are reserved and should be set to 0.

A[1:0]: Bits 10:9 – Register Address

These bits define the address for REGISTER 3.

| A1 | A0 | |
|----|----|------------|
| 1 | 1 | Register 3 |

res: Bits 8:6 – Reserved
These bits are reserved and should be set to 0.

LOP: Bit 5 – ADC to DAC Loopback Control

When this bit is set to 1, the ADC audio data is sent directly to the DAC. The data format defaults to I²S; DOUT is still available in loopback mode.

| LOP | |
|-----|-----------------------------|
| 0 | Loopback disabled (default) |
| 1 | Loopback enabled |

FMT[2:0]: Bits 4:2 – Audio Data Format Select

These bits determine the input and output audio data formats. (default: FMT[2:0] = 000_b)

| FM2 | FMT1 | FMT0 | DAC DATA FORMAT | ADC DATA FORMAT |
|-----|------|------|---|-------------------------------------|
| 0 | 0 | 0 | 16-bit, MSB-first, right-justified | 16-bit, MSB-first, left-justified |
| 0 | 0 | 1 | 18-bit, MSB-first, right-justified | 18-bit, MSB-first, left-justified |
| 0 | 1 | 0 | 16-bit, MSB-first, right-justified | 16-bit, MSB-first, right-justified |
| 0 | 1 | 1 | 18-bit, MSB-first, right-justified | 18-bit, MSB-first, right-justified |
| 1 | 0 | 0 | 16-/18-bit, MSB-first, left-justified | 18-bit, MSB-first, left-justified |
| 1 | 0 | 1 | 16-/18-bit, MSB-first, I ² S | 18-bit, MSB-first, I ² S |
| 1 | 1 | 0 | 16-bit, MSB-first, DSP-frame | 16-bit, MSB-first, DSP-frame |
| 1 | 1 | 1 | Reserved | Reserved |

LRP: Bit 1 – ADC-to-DAC LRCK Polarity Select

Polarity of LRCIN applies only to formats 0 through 4.

| LRP | |
|-----|--|
| 0 | Left channel is H, right channel is L (default). |
| 1 | Left channel is L, right channel is H. |

res: Bit 0 – Reserved
This bit is reserved and should be set to 0.

PCM3001 DATA FORMAT CONTROL

The input and output data formats are controlled by pins 27 (FMT0), 26 (FMT1), and 25 (FMT2). Set these pins to the same values shown for the bit-mapped PCM3000 controls in program register 3.

THEORY OF OPERATION

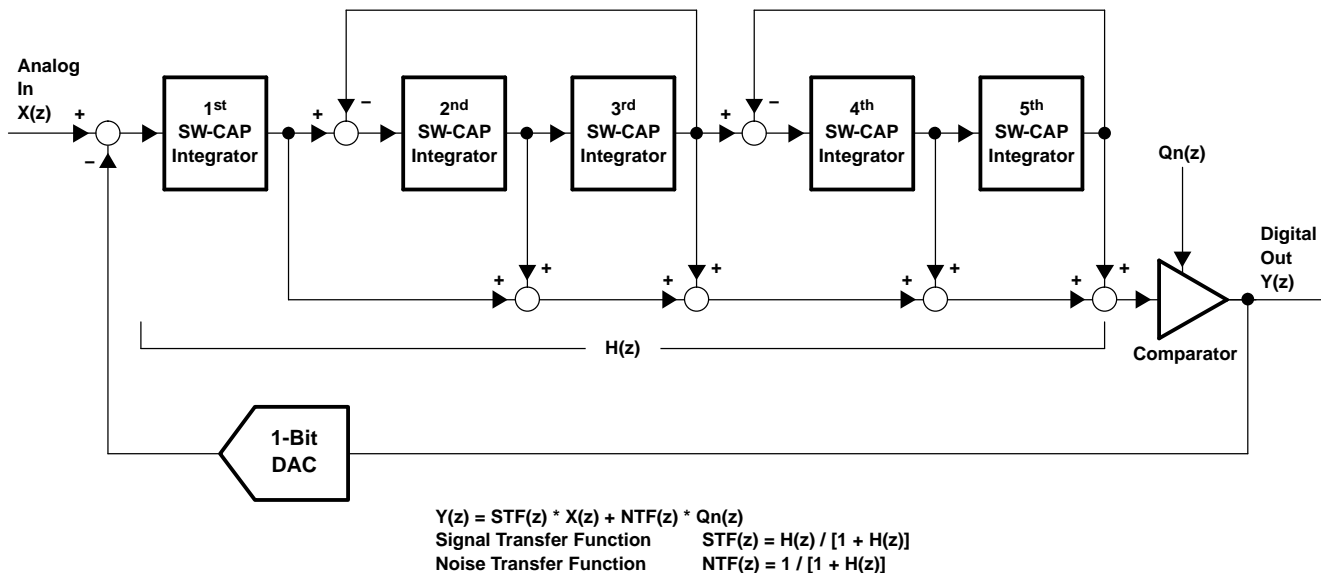
ADC SECTION

The PCM3000/3001 ADC consists of a band-gap reference, a stereo single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The block diagram in this data sheet illustrates the architecture of the ADC section. Figure 17 shows the single-to-differential converter, and Figure 31 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

An internal high-precision reference with two external capacitors provides all reference voltages required by the ADC, which defines the full scale range for the converter. The internal single-to-differential voltage converter saves the space and extra parts needed for external circuitry which is required by many delta-sigma converters. The internal full-differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at a $64\times$ oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying antialias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator, and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64\text{-}f_s$ 1-bit data stream from the modulator is converted to $1\text{-}f_s$, 18-bit data words by the decimation filter, which also acts as a low-pass filter to remove the shaped quantization noise. The dc components are removed by a high-pass filter function contained within the decimation filter.



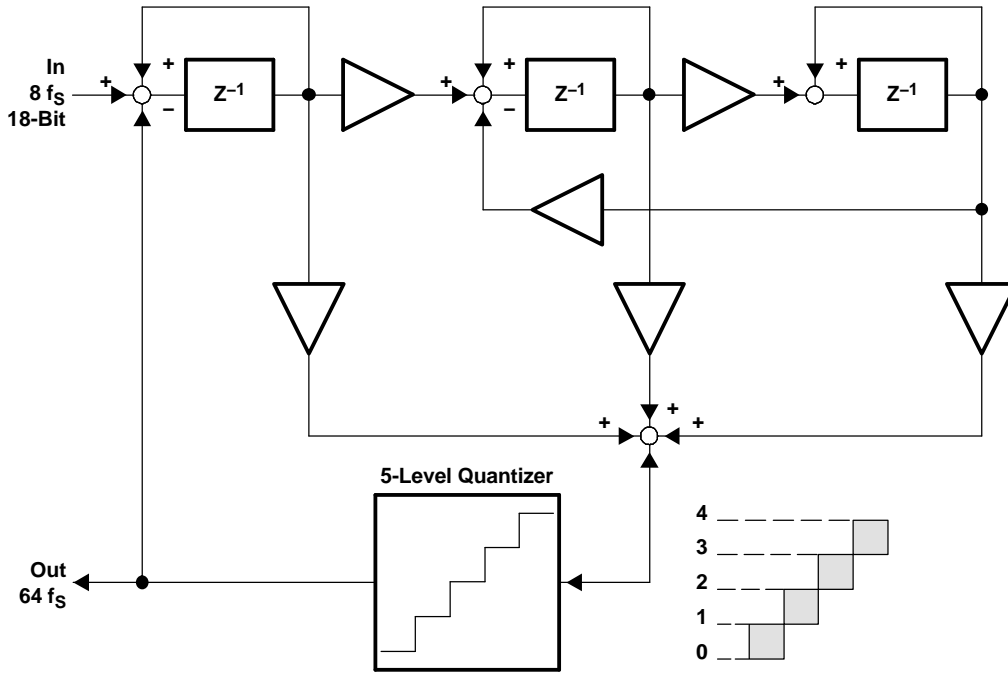
B0005-01

Figure 31. Simplified Fifth-Order Delta-Sigma Modulator

DAC SECTION

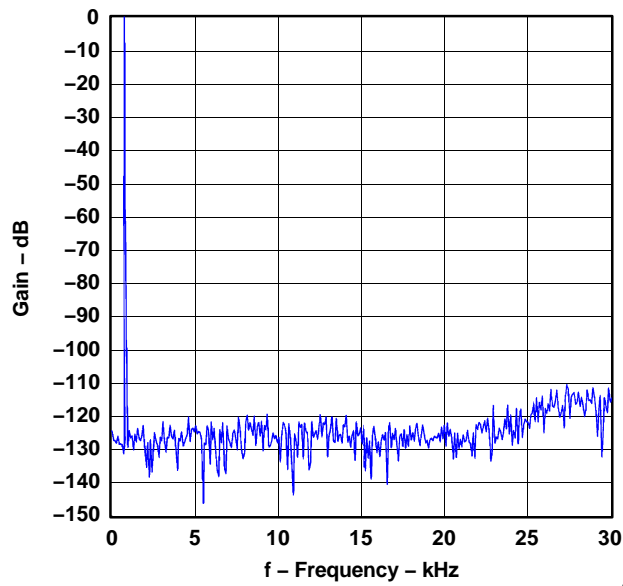
The delta-sigma DAC section of the PCM3000/3001 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to a 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 32. This 5-level delta-sigma modulator has the advantage of improved stability and reduced clock-jitter sensitivity over the typical one-bit (2-level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal $8\times$ interpolation filter is $64 f_s$ for a $256\text{-}f_s$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 33.



B0008-02

Figure 32. 5-Level $\Delta\Sigma$ Modulator Block Diagram



G027

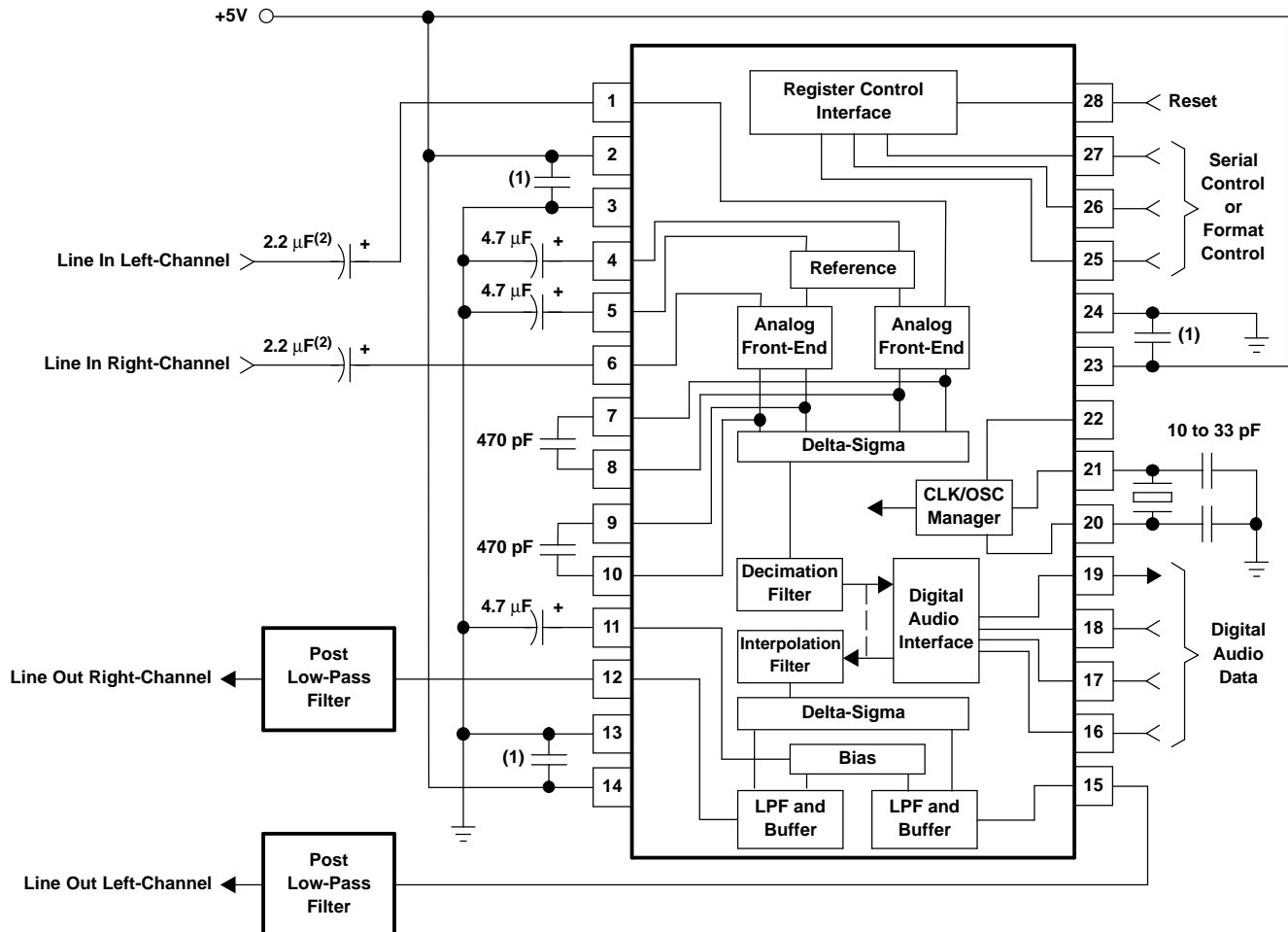
Figure 33. Quantization Noise Spectrum

APPLICATION INFORMATION

APPLICATION AND LAYOUT CONSIDERATIONS

TYPICAL CONNECTION

A typical connection diagram for the PCM3000/3001 is shown in Figure 34.



S0018-01

(1) Bypass capacitor = 0.1 μ F and 10 μ F.

(2) The input capacitor affects the pole of the HPF. Example: 2.2 μ F sets the cutoff frequency to 4.8 Hz, with a 66-ms time constant.

Figure 34. Typical Connection Diagram for PCM3000/3001

POWER SUPPLY BYPASSING

The digital and analog power-supply lines to the PCM3000/3001 should be bypassed to the corresponding ground pins with both 0.1- μ F ceramic and 10- μ F tantalum capacitors as close to the device pins as possible to maximize the performance of the ADC and DAC. Although the PCM3000/3001 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power-supply sequencing problems. If separate power supplies are used, back-to-back diodes between the two power sources near the device are recommended to avoid latch-up problems.

APPLICATION INFORMATION (continued)

GROUNDING

In order to optimize dynamic performance of the PCM3000/3001, the analog and digital grounds are not internally connected. PCM3000/3001 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3000/3001 ground pins to the analog ground plane using low-impedance connections. The PCM3000/3001 should reside entirely over this plane to avoid coupling high-frequency digital switching noise into the analog ground plane.

VOLTAGE INPUTS

A tantalum or aluminum electrolytic capacitor, between 2.2 μF and 10 μF , is recommended as an ac-coupling capacitor at the inputs. Combined with the 15-k Ω characteristic input impedance, a 2.2- μF coupling capacitor establishes a 4.8-Hz cutoff frequency for blocking dc. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 15-k Ω input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7- μF to 10- μF tantalum capacitor is recommended between V_{REFL}, V_{REFR}, and AGND1 to ensure low source impedance for the ADC references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

C_{INP} AND C_{INN} INPUTS

A 470-pF to 1000-pF film or NPO ceramic capacitor is recommended between C_{INPL} and C_{INNL}, and also between C_{INPR} and C_{INNR} to create an antialias filter that has a 170-kHz to 80-kHz cutoff frequency. These capacitors should be located as close as possible to the C_{INP} and C_{INN} pins to avoid introducing undesirable noise or dynamic errors into the delta-sigma modulator.

VCOM INPUT

A 4.7- μF to 10- μF tantalum capacitor is recommended between VCOM and AGND2 to ensure low source impedance of the DAC output common. This capacitor should be located as close as possible to the VCOM pin to reduce dynamic errors on the DAC common.

SYSTEM CLOCK

The quality of the system clock can influence the dynamic performance of both the ADC and DAC in the PCM3000/3001. The duty cycle, jitter, and threshold voltage at the system clock input pin should be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN), and word clock (LCRIN) must also be supplied simultaneously. Failure to supply the audio clocks results in a power dissipation increase of up to three times normal dissipation and may degrade long-term reliability if the maximum power dissipation limit is exceeded.

RSTB CONTROL

If capacitors greater than 4.7 μF are used on V_{REF} and VCOM, an external reset control with delay time corresponding to the V_{REF}, VCOM response is required.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| PCM3000E | ACTIVE | SSOP | DB | 28 | 47 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3000E/2K | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3000E/2KG4 | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3000EG4 | ACTIVE | SSOP | DB | 28 | 47 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3001E | ACTIVE | SSOP | DB | 28 | 47 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3001E/2K | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3001E/2KG4 | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| PCM3001EG/2K | ACTIVE | | | | | Pb-Free (RoHS) | CU SNBI | Level-1-260C-UNLIM |
| PCM3001EG4 | ACTIVE | SSOP | DB | 28 | 47 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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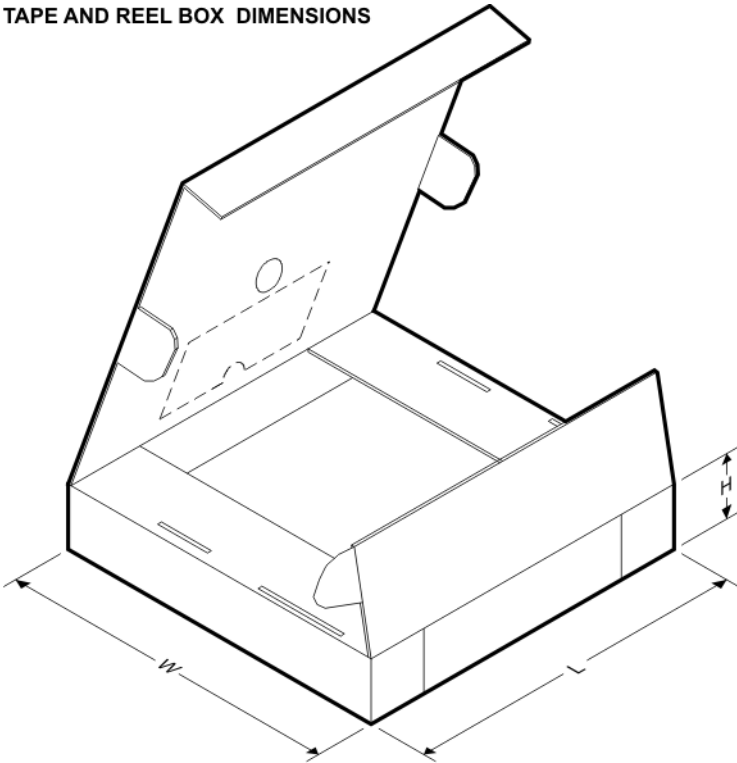
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM3000E/2K | SSOP | DB | 28 | 2000 | 330.0 | 17.4 | 8.5 | 10.8 | 2.4 | 12.0 | 16.0 | Q1 |
| PCM3001E/2K | SSOP | DB | 28 | 2000 | 330.0 | 17.4 | 8.5 | 10.8 | 2.4 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM3000E/2K | SSOP | DB | 28 | 2000 | 336.6 | 336.6 | 28.6 |
| PCM3001E/2K | SSOP | DB | 28 | 2000 | 336.6 | 336.6 | 28.6 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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