

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

PERFORMANCE FEATURES

Up to 19 ns instruction cycle time, 52 MIPS sustained performance
 Single-cycle instruction execution
 Single-cycle context switch
 3-bus architecture allows dual operand fetches in every instruction cycle
 Multifunction instructions
 Power-down mode featuring low CMOS standby power dissipation with 400 CLKIN cycle recovery from power-down condition
 Low power dissipation in idle mode

INTEGRATION FEATURES

ADSP-2100 family code compatible (easy to use algebraic syntax), with instruction set extensions
 Up to 160K bytes of on-chip RAM, configured
 Up to 32K words program memory RAM
 Up to 32K words data memory RAM
 Dual-purpose program memory for both instruction and data storage
 Independent ALU, multiplier/accumulator, and barrel shifter computational units
 2 independent data address generators
 Powerful program sequencer provides zero overhead looping conditional instruction execution
 Programmable 16-bit interval timer with prescaler
 100-lead LQFP and 144-ball BGA

SYSTEM INTERFACE FEATURES

16-bit internal DMA port for high-speed access to on-chip memory (mode selectable)
 4M-byte memory interface for storage of data tables and program overlays (mode selectable)
 8-bit DMA to byte memory for transparent program and data memory transfers (mode selectable)
 Programmable memory strobe and separate I/O memory space permits "glueless" system design
 Programmable wait state generation
 2 double-buffered serial ports with companding hardware and automatic data buffering
 Automatic booting of on-chip program memory from byte-wide external memory, for example, EPROM, or through internal DMA Port
 6 external interrupts
 13 programmable flag pins provide flexible system signaling
 UART emulation through software SPORT reconfiguration
 ICE-Port emulator interface supports debugging in final systems

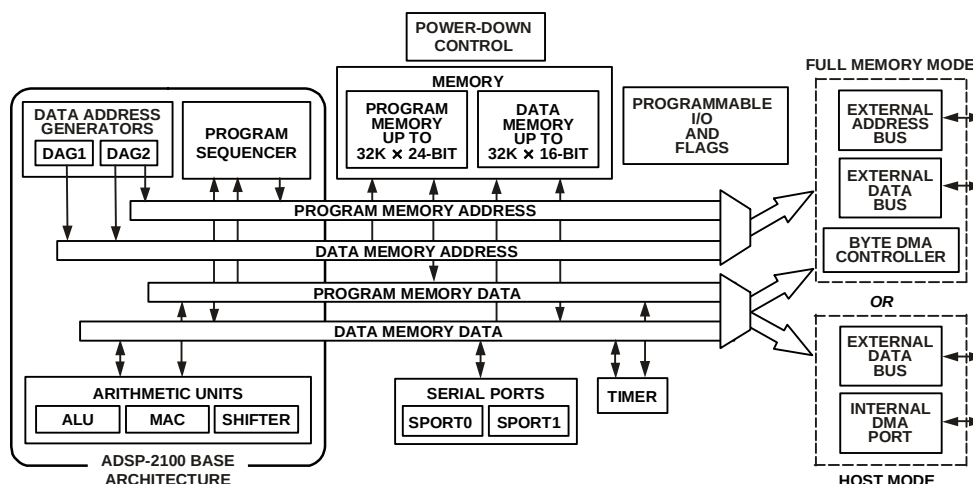


Figure 1. Functional Block Diagram

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Rev. C

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ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

TABLE OF CONTENTS

Performance Features	1	Specifications	21
Integration Features	1	Operating Conditions	21
System Interface Features	1	Electrical Characteristics	21
Table of Contents	2	Absolute Maximum Ratings	22
Revision History	2	Package Information	22
General Description	3	ESD Sensitivity	22
Architecture Overview	3	Timing Specifications	22
Modes Of Operation	4	Power Supply Current	36
Interrupts	5	Power Dissipation	37
Low Power Operation	6	Output Drive Currents	40
System Interface	7	Power-Down Current	41
Reset	8	Capacitive Loading – ADSP-2184L, ADSP-2186L	42
Memory Architecture	8	Capacitive Loading – ADSP-2185L, ADSP-2187L	42
Bus Request and Bus Grant	13	Test Conditions	43
Flag I/O Pins	13	Environmental Conditions	43
Instruction Set Description	14	LQFP Package Pinout	44
Development System	14	BGA Package Pinout	45
Additional Information	16	Outline Dimensions	46
Pin Descriptions	17	Surface Mount Design	47
Memory Interface Pins	18	Ordering Guide	47
Terminating Unused Pins	19		

REVISION HISTORY

1/08—Rev. C

This revision of the ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L processor data sheet combines the ADSP-2184L, ADSP-2185L, ADSP-2186L, and ADSP-2187L. This version also contains new RoHS compliant packages.

GENERAL DESCRIPTION

The ADSP-218xL series consists of four single chip microcomputers optimized for digital signal processing applications. The functional block diagram for the ADSP-218xL series members appears in [Figure 1 on Page 1](#). All series members are pin-compatible and are differentiated solely by the amount of on-chip SRAM. This feature, combined with ADSP-21xx code compatibility, provides a great deal of flexibility in the design decision. Specific family members are shown in [Table 1](#).

Table 1. ADSP-218xL DSP Microcomputer Family

Device	Program Memory (K words)	Data Memory (K words)
ADSP-2184L	4	4
ADSP-2185L	16	16
ADSP-2186L	8	8
ADSP-2187L	32	32

ADSP-218xL series members combine the ADSP-2100 family base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

ADSP-218xL series members integrate up to 160K bytes of on-chip memory configured as up to 32K words (24-bit) of program RAM, and up to 32K words (16-bit) of data RAM. Power-down circuitry is also provided to meet the low power needs of battery-operated portable equipment. The ADSP-218xL is available in 100-lead LQFP and 144-ball BGA packages.

Fabricated using high-speed, low-power, CMOS processes, ADSP-218xL series members operate with a 19 ns instruction cycle time (ADSP-2185L and ADSP-2187L) or a 25 ns instruction cycle time (ADSP-2184L and ADSP-2186L). Every instruction can execute in a single processor cycle.

The ADSP-218xL's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, ADSP-218xL series members can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

ARCHITECTURE OVERVIEW

The ADSP-218xL series instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-218xL assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The functional block diagram is an overall block diagram of the ADSP-218xL series. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, ADSP-218xL series members execute looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Five internal buses provide efficient data transfer:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting ADSP-218xL series members to fetch two operands in a single cycle, one from program memory and one from data memory. ADSP-218xL series members can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, ADSP-218xL series members can be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSP's on-chip program and data RAM.

An interface to low cost, byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BGG}$). One execution mode (Go Mode) allows the ADSP-218xL to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

ADSP-218xL series members can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORT), the BDMA port, and the power-down circuitry. There is also a master RESET signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each serial port can generate an internal programmable serial clock or accept an external serial clock.

ADSP-218xL series members provide up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

ADSP-218xL series members incorporate two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Following is a brief list of the capabilities of the ADSP-218xL SPORTs. For additional information on Serial Ports, refer to the *ADSP-218x DSP Hardware Reference*.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 bits to 16 bits and provide optional A-law and μ -law companding, according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24-word or 32-word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

MODES OF OPERATION

The ADSP-218xL series modes of operation appear in [Table 2](#). Only the ADSP-2187L provides Mode D operation

Setting Memory Mode

Memory Mode selection for the ADSP-218xL series is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration

Passive Configuration involves the use of a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down resistance, on the order of 10 k Ω , can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption

Table 2. Modes of Operation

Mode D ¹	Mode C	Mode B	Mode A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode. ²
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used, but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (Requires additional hardware.)
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. ²
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (Requires additional hardware.)
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until the host writes to internal program memory location 0. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down. ²

¹ Mode D applies to the ADSP-2187L processor only.

² Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down resistance will hold the pin in a known state, and will not switch.

Active Configuration

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should be three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level, and will not oscillate should the three-state driver's level hover around the logic switching point.

IDMA ACK Configuration (ADSP-2187L Only)

Mode D = 0 and in Host Mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be "wire-OR'ed." Mode D = 1 and in Host Mode: $\overline{\text{IACK}}$ is an open drain and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be "wire-OR'ed" together.

INTERRUPTS

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. ADSP-218xL series members provide four dedicated external interrupt input pins: $\overline{\text{IRQ2}}$, $\overline{\text{IRQL0}}$, $\overline{\text{IRQL1}}$, and $\overline{\text{IRQE}}$ (shared with the PF7–4 pins). In addition, SPORT1 may be reconfigured for $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, FI, and FO, for a total of six external interrupts. The ADSP-218xL also supports internal interrupts

from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power-down and reset). The $\overline{\text{IRQ2}}$, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{\text{IRQL0}}$ and $\overline{\text{IRQL1}}$ are level-sensitive and $\overline{\text{IRQE}}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table 3.

Table 3. Interrupt Priority and Interrupt Vector Addresses

Source Of Interrupt	Interrupt Vector Address (Hex)
$\overline{\text{RESET}}$ (or Power-Up with PUCR = 1)	0x0000 (highest priority)
Power-Down (Nonmaskable)	0x002C
$\overline{\text{IRQ2}}$	0x0004
$\overline{\text{IRQL1}}$	0x0008
$\overline{\text{IRQL0}}$	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
$\overline{\text{IRQE}}$	0x0018
BDMA Interrupt	0x001C
SPORT1 Transmit or $\overline{\text{IRQ1}}$	0x0020
SPORT1 Receive or $\overline{\text{IRQ0}}$	0x0024
Timer	0x0028 (lowest priority)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Individual interrupt requests are logically AND'ed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

ADSP-218xL series members mask all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ external interrupts to be either edge- or level-sensitive. The $\overline{\text{IRQE}}$ pin is an external edge-sensitive interrupt and can be forced and cleared. The $\overline{\text{IRQLO}}$ and $\overline{\text{IRQLI}}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are 12 levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power-down), regardless of the state of IMASK:

```
ENA INTS;  
DIS INTS;
```

Disabling the interrupts does not affect serial port autobuffering or DMA. When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

ADSP-218xL series members have three low-power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power-Down

ADSP-218xL series members have a low-power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-218x DSP Hardware Reference*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 400 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 400 CLKIN cycle recovery.

- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 400 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{\text{PWD}}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin (PWDACK) indicates when the processor has entered power-down.

Idle

When the ADSP-218xL is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle Mode IDMA, BDMA, and autobuffer cycle steals still occur.

Slow Idle

The IDLE instruction is enhanced on ADSP-218xL series members to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

```
IDLE (n);
```

where $n = 16, 32, 64$, or 128 . This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n , the clock divisor. When an enabled interrupt is received, ADSP-218xL series members remain in the idle state for up to a maximum of n processor cycles ($n = 16, 32, 64$, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a

faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows typical basic system configurations with the ADSP-218xL series, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. ADSP-218xL series members also provide four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

Clock Signals

ADSP-218xL series members can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the

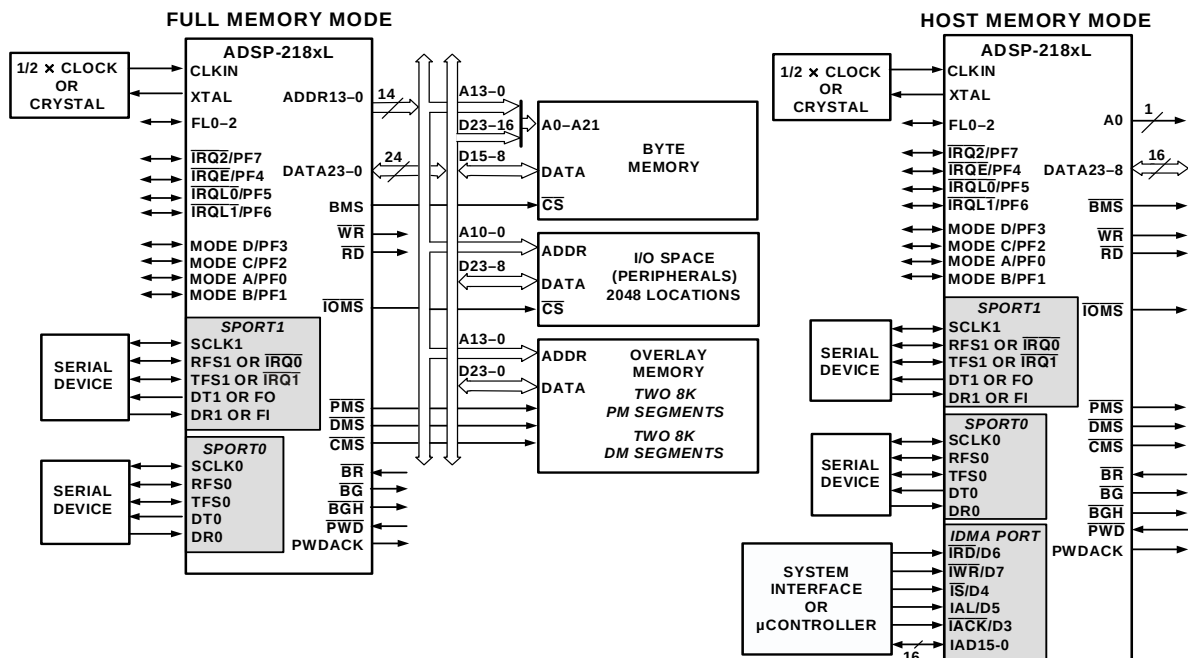
power-down state. For additional information, refer to the *ADSP-218x DSP Hardware Reference*, for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL pin must be left unconnected.

ADSP-218xL series members use an input clock with a frequency equal to half the instruction rate; a 40 MHz input clock yields a 12.5 ns processor cycle (which is equivalent to 80 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because ADSP-218xL series members include an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used. To provide an adequate feedback path around the internal amplifier circuit, place a resistor in parallel with the circuit, as shown in Figure 3.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.



NOTE: MODE D APPLIES TO THE ADSP-2187L PROCESSOR ONLY

Figure 2. Basic System Interface

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

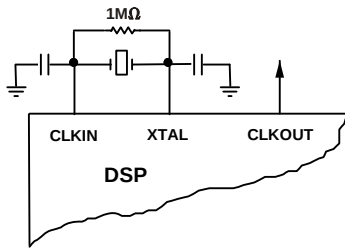


Figure 3. External Crystal Connections

RESET

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-218xL. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked, but does not include the crystal oscillator start-up time. During this power-up sequence, the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification (t_{RSP}).

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the use of an external Schmitt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading

sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

MEMORY ARCHITECTURE

The ADSP-218xL series provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O. Refer to Figure 4 through Figure 7 for PM and DM memory allocations in the ADSP-218xL series.

Program Memory

Program Memory (Full Memory Mode) is a 24-bit-wide space for storing both instruction opcodes and data. The member DSPs of this series have up to 32K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces, using the external data bus.

Program Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in Host Mode due to a restricted data bus that is only 16 bits wide.

Data Memory

Data Memory (Full Memory Mode) is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-218xL series has up to 32K words of Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

Data Memory (Host Mode) allows access to all internal memory. External overlay access is limited by a single external address line (A0).

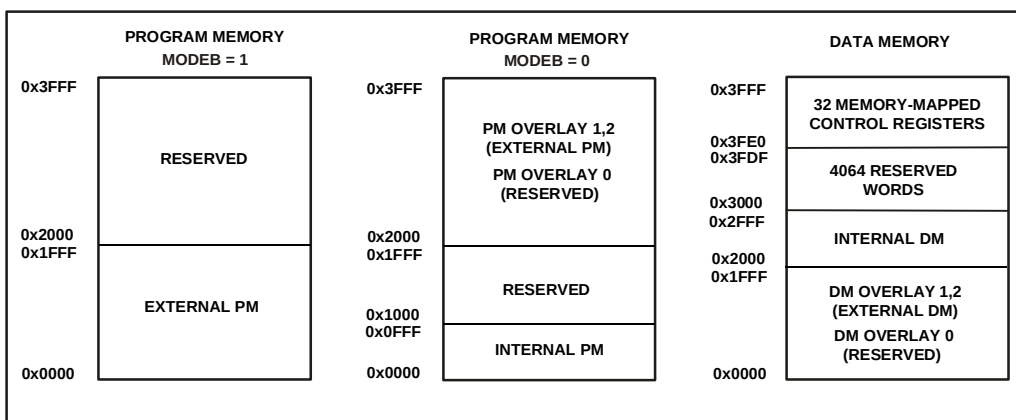


Figure 4. ADSP-2184 Memory Architecture

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

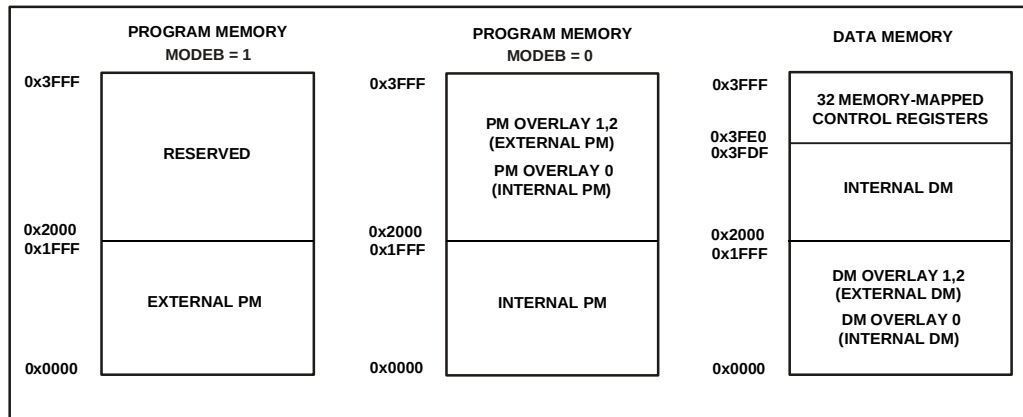


Figure 5. ADSP-2185 Memory Architecture

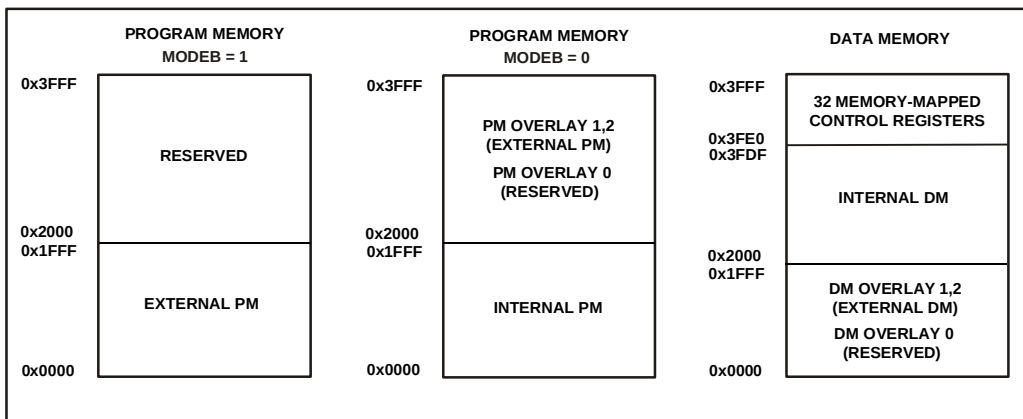


Figure 6. ADSP-2186 Memory Architecture

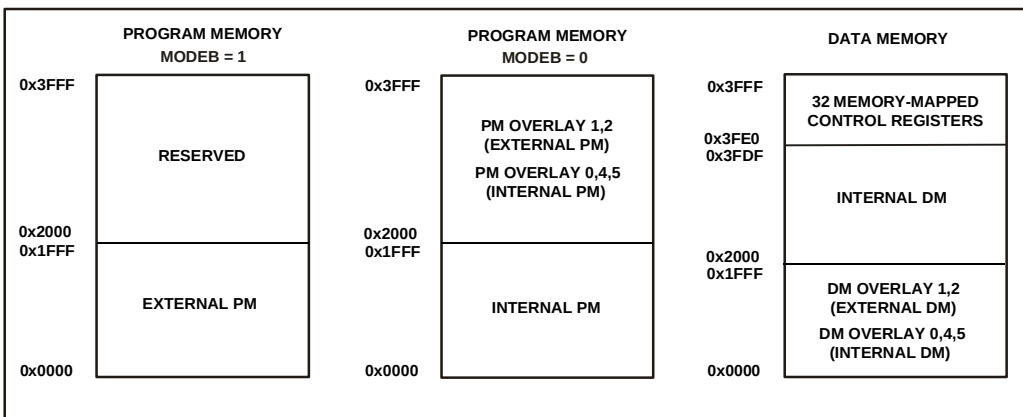


Figure 7. ADSP-2187 Memory Architecture

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Table 4. PMOVLAY Bits

Processor	PMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not Applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x2000 and 0x3FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x2000 and 0x3FFF

Table 5. DMOVLAY Bits

Processor	DMOVLAY	Memory	A13	A12–0
ADSP-2184L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2185L	0	Internal overlay	Not applicable	Not applicable
ADSP-2186L	No internal overlay region	Not applicable	Not applicable	Not applicable
ADSP-2187L	0, 4, 5	Internal overlay	Not applicable	Not applicable
All Processors	1	External overlay 1	0	13 LSBs of address between 0x0000 and 0x1FFF
All Processors	2	External overlay 2	1	13 LSBs of address between 0x0000 and 0x1FFF

I/O Space (Full Memory Mode)

ADSP-218xL series members support an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined.

Two instructions were added to the core ADSP-2100 family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated 3-bit wait state registers, IOWAIT0–3 as shown in Figure 8, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges, as shown in Table 6.

Note: In Full Memory Mode, all 2048 locations of I/O space are directly addressable. In Host Memory Mode, only address pin A0 is available; therefore, additional logic is required externally to achieve complete addressability of the 2048 I/O space locations.

Table 6. Wait States

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

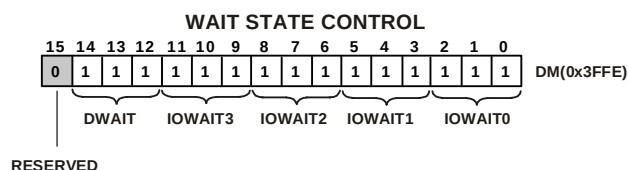


Figure 8. Wait State Control Register

Composite Memory Select

ADSP-218xL series members have a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality. Each bit in the CMSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the BMS bit.

See Figure 9 and Figure 10 for illustration of the programmable flag and composite control register and the system control register.

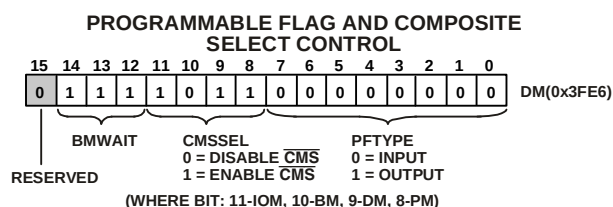
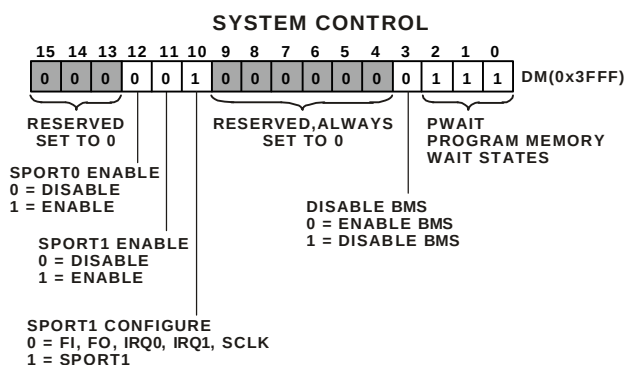


Figure 9. Programmable Flag and Composite Control Register



NOTE: RESERVED BITS ARE SHOWN ON A GRAY FIELD. THESE BITS SHOULD ALWAYS BE WRITTEN WITH ZEROS.

Figure 10. System Control Register

Byte Memory Select

The ADSP-218xL's $\overline{\text{BMS}}$ disable feature combined with the CMS pin allows use of multiple memories in the byte memory space. For example, an EPROM could be attached to the BMS select, and a flash memory could be connected to $\overline{\text{CMS}}$. Because at reset $\overline{\text{BMS}}$ is enabled, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the flash memory.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is $16\text{K} \times 8$ bits.

The byte memory space on the ADSP-218xL series supports read and write operations as well as four different data formats. The byte memory uses data bits 15–8 for data. The byte memory uses data bits 23–16 and address bits 13–0 to create a 22-bit address. This allows up to a 4 megabit $\times$ 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA, Full Memory Mode)

The byte memory DMA controller (Figure 11) allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16-, or 24-bit word transferred.

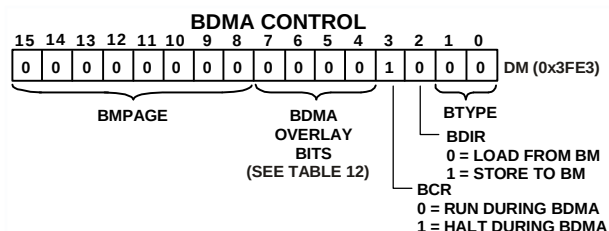


Figure 11. BDMA Control Register

The BDMA circuit supports four different data formats that are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table 7 shows the data formats supported by the BDMA circuit.

Table 7. Data Formats

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program memory	24	Full word
01	Data memory	16	Full word
10	Data memory	8	MSBs
11	Data memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally, the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register.

The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations. The source or destination of a BDMA transfer is always on-chip program or data memory.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

The BDMA overlay bits specify the OVLAY memory blocks to be accessed for internal memory. Set these bits as indicated in [Figure 11](#).

Note: BDMA cannot access external overlay memory regions 1 and 2.

The BMWAIT field, which has 3 bits on ADSP-218xL series members, allows selection of up to 7 wait states for BDMA transfers.

Internal Memory DMA Port (IDMA Port; Host Memory Mode)

The IDMA Port provides an efficient means of communication between a host system and ADSP-218xL series members. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead. The IDMA port cannot, however, be used to write to the DSP's memory-mapped control registers. A typical IDMA transfer process is shown as follows:

1. Host starts IDMA transfer.
2. Host checks $\overline{\text{IACK}}$ control line to see if the DSP is busy.
3. Host uses $\overline{\text{IS}}$ and IAL control lines to latch either the DMA starting address (IDMAA) or the PM/DM OVLAY selection into the DSP's IDMA control registers. If Bit 15 = 1, the values of Bits 7–0 represent the IDMA overlay; Bits 14–8 must be set to 0. If Bit 15 = 0, the value of Bits 13–0 represent the starting address of internal memory to be accessed and Bit 14 reflects PM or DM for access. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicated in [Table 8](#).
4. Host uses $\overline{\text{IS}}$ and $\overline{\text{IRD}}$ (or $\overline{\text{IWR}}$) to read (or write) DSP internal memory (PM or DM).
5. Host checks $\overline{\text{IACK}}$ line to see if the DSP has completed the previous IDMA operation.
6. Host ends IDMA transfer.

Table 8. IDMA/BDMA Overlay Bits

Processor	IDMA/BDMA PMOVLAY	IDMA/BDMA DMOVLAY
ADSP-2184L	0	0
ADSP-2185L	0	0
ADSP-2186L	0	0
ADSP-2187L	0, 4, 5	0, 4, 5

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written while the ADSP-218xL is operating at full speed.

The DSP memory address is latched and then automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the IDMA address latch signal (IAL) or the missing edge of the IDMA select signal ($\overline{\text{IS}}$) latches this value into the IDMAA register.

Once the address is stored, data can be read from, or written to, the ADSP-218xL's on-chip memory. Asserting the select line ($\overline{\text{IS}}$) and the appropriate read or write line ($\overline{\text{IRD}}$ and $\overline{\text{IWR}}$ respectively) signals the ADSP-218xL that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation. Asserting the IDMA port select ($\overline{\text{IS}}$) and address latch enable (IAL) directs the ADSP-218xL to write the address onto the IAD14–0 bus into the IDMA Control Register ([Figure 12](#)). If Bit 15 is set to 0, IDMA latches the address. If Bit 15 is set to 1, IDMA latches into the OVLAY register. This register, also shown in [Figure 12](#), is memory-mapped at address DM (0x3FE0). Note that the latched address (IDMAA) cannot be read back by the host. The IDMA Overlay register applies to The ADSP-2187L processor only.

When Bit 14 in 0x3FE7 is set to zero, short reads use the timing shown in [Figure 26 on Page 34](#). When Bit 14 in 0x3FE7 is set to 1, timing in [Figure 27 on Page 35](#) applies for short reads in Short Read Only Mode. Set IDDMOVLAY and IDPMOVLAY bits in the IDMA overlay register as indicated in [Table 8](#). Refer to the *ADSP-218x DSP Hardware Reference* for additional details.

Note: In Full Memory Mode, all locations of 4M-byte memory space are directly addressable. In Host Memory Mode, only address pin A0 is available, requiring additional external logic to provide address information for the byte.

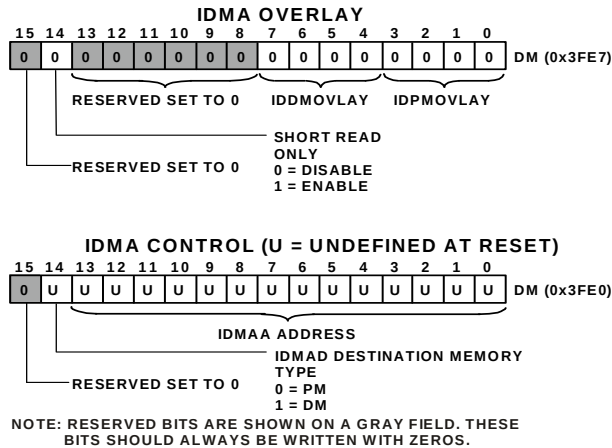


Figure 12. IDMA OVLAY/Control Registers

Bootstrap Loading (Booting)

ADSP-218xL series members have two mechanisms to allow automatic loading of the internal program memory after reset. The method for booting is controlled by the Mode A, Mode B, and Mode C configuration bits.

When the mode pins specify BDMA booting, the ADSP-218xL initiates a BDMA boot sequence when reset is released.

The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24-bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space-compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface. For BDMA accesses while in Host Mode, the addresses to boot memory must be constructed externally to the ADSP-218xL. The only memory address bit provided by the processor is A0.

IDMA Port Booting

ADSP-218xL series members can also boot programs through its internal DMA port. If Mode C = 1, Mode B = 0, and Mode A = 1, the ADSP-218xL boots from the IDMA port. IDMA feature

can load as much on-chip memory as desired. Program execution is held off until the host writes to on-chip program memory location 0.

BUS REQUEST AND BUS GRANT

ADSP-218xL series members can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the Bus Request ($\overline{BR}$) signal. If the ADSP-218xL is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-218xL will not halt program execution until it encounters an instruction that requires an external memory access.

If an ADSP-218xL series member is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces nor assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers, and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when an ADSP-218xL series member requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-218xL deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

FLAG I/O PINS

ADSP-218xL series members have eight general-purpose programmable input/output flag pins. They are controlled by two memory-mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-218xL's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, ADSP-218xL series members have five fixed-mode flags, FI, FO, FL0, FL1, and FL2. FL0 to FL2 are dedicated output flags. FI and FO are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2, and PF3 are also used for device configuration during reset.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

INSTRUCTION SET DESCRIPTION

The ADSP-218xL series assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as $AR = AX0 + AY0$, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-218xL's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction, with up to two fetches or one write to processor memory space, during a single instruction cycle.

DEVELOPMENT SYSTEM

Analog Devices' wide range of software and hardware development tools supports the ADSP-218xL series. The DSP tools include an integrated development environment, an evaluation kit, and a serial port emulator.

VisualDSP++[†] is an integrated development environment, allowing for fast and easy development, debugging, and deployment. The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy-to-use assembler that is based on an algebraic syntax; an archiver (librarian/library builder); a linker; a PROM-splitter utility; a cycle-accurate, instruction-level simulator; a C compiler; and a C run-time library that includes DSP and mathematical functions.

Debugging both C and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C and assembly code (interleaved source and object information)
- Insert break points
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution

- Fill and dump memory
- Source level debugging

The VisualDSP++ IDE lets programmers define and manage DSP software development. The dialog boxes and property pages let programmers configure and manage all of the ADSP-218xL development tools, including the syntax highlighting in the VisualDSP++ editor. This capability controls how the development tools process inputs and generate outputs.

The ADSP-2189M EZ-KIT Lite[‡] provides developers with a cost-effective method for initial evaluation of the powerful ADSP-218xL DSP family architecture. The ADSP-2189M EZ-KIT Lite includes a standalone ADSP-2189M DSP board supported by an evaluation suite of VisualDSP++. With this EZ-KIT Lite, users can learn about DSP hardware and software development and evaluate potential applications of the ADSP-218xL series. The ADSP-2189M EZ-KIT Lite provides an evaluation suite of the VisualDSP++ development environment with the C compiler, assembler, and linker. The size of the DSP executable that can be built using the EZ-KIT Lite tools is limited to 8K words.

The EZ-KIT Lite includes the following features:

- 75 MHz ADSP-2189M
- Full 16-Bit Stereo Audio I/O with AD73322 Codec
- RS-232 Interface
- EZ-ICE[§] Connector for Emulator Control
- DSP Demonstration Programs
- Evaluation Suite of VisualDSP++

The ADSP-218x EZ-ICE[§] Emulator provides an easier and more cost-effective method for engineers to develop and optimize DSP systems, shortening product development cycles for faster time-to-market. ADSP-218xL series members integrate on-chip emulation support with a 14-pin ICE-Port[™] interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. ADSP-218xL series members need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs. The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution

[†] VisualDSP++ is a registered trademark of Analog Devices, Inc.

[‡] EZ-KIT Lite is a registered trademark of Analog Devices, Inc.

[§] EZ-ICE is a registered trademark of Analog Devices, Inc.

- Complete assembly and disassembly of instructions
- C source-level debugging

Designing an EZ-ICE-Compatible System

ADSP-218xL series members have on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If a passive method of maintaining mode information is being used (as discussed in [Setting Memory Mode on Page 4](#)), it does not matter that the mode information is latched by an emulator reset. However, if the $\overline{\text{RESET}}$ pin is being used as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in [Figure 13](#). This circuit forces the value located on the Mode A pin to logic high, regardless of whether it is latched via the $\overline{\text{RESET}}$ or $\overline{\text{ERESET}}$ pin.

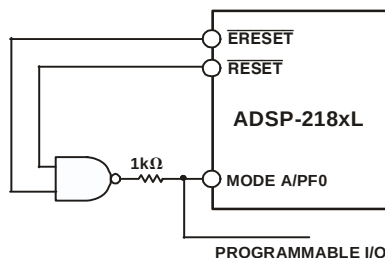


Figure 13. Mode A Pin/EZ-ICE Circuit

The ICE-Port interface consists of the following ADSP-218xL pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, $\overline{\text{EE}}$, $\overline{\text{EBG}}$, $\overline{\text{ECLK}}$, $\overline{\text{ERESET}}$, $\overline{\text{ELIN}}$, $\overline{\text{EMS}}$, and $\overline{\text{EOUT}}$.

These ADSP-218xL pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-218xL and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the $\overline{\text{EE}}$ (emulator enable) signal to take control of the ADSP-218xL in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in the system.

The EZ-ICE connects to the target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe

The EZ-ICE connector (a standard pin strip header) is shown in [Figure 14](#). This connector must be added to the target board design to use the EZ-ICE. Be sure to allow enough room in the system to fit the EZ-ICE probe onto the 14-pin connector.

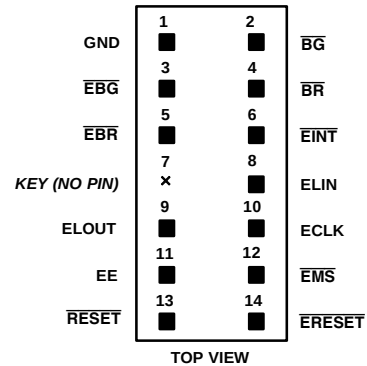


Figure 14. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inch. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface

For the target system to be compatible with the EZ-ICE emulator, it must comply with the following memory interface guidelines:

Design the Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst-case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If the target does not meet the worst-case chip specification for memory access parameters, the circuitry may not be able to be emulated at the desired CLKIN frequency. Depending on the severity of the specification violation, the system may be difficult to manufacture, as DSP components statistically vary in switching characteristic and timing requirements, within published limits.

Restriction: All memory strobe signals on the ADSP-218xL ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in the target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed when the EZ-ICE is not being used.

Target System Interface Signals

When the EZ-ICE board is installed, the performance on some system signals changes. Design the system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between the target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$, when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ-ICE board's DSP.

ADDITIONAL INFORMATION

This data sheet provides a general overview of ADSP-218xL series functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-218x DSP Hardware Reference* and the *ADSP-218x DSP Instruction Set Reference*.

PIN DESCRIPTIONS

ADSP-218xL series members are available in a 100-lead LQFP package and a 144-ball BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{\text{RESET}}$ only, while serial port pins are

software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text in [Table 9](#), while alternate functionality is shown in *italics*.

Table 9. Common-Mode Pins

Pin Name	No. of Pins	I/O	Function
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{BR}}$	1	I	Bus Request Input
$\overline{\text{BG}}$	1	O	Bus Grant Output
$\overline{\text{BGH}}$	1	O	Bus Grant Hung Output
$\overline{\text{DMS}}$	1	O	Data Memory Select Output
$\overline{\text{PMS}}$	1	O	Program Memory Select Output
$\overline{\text{IOMS}}$	1	O	Memory Select Output
$\overline{\text{BMS}}$	1	O	Byte Memory Select Output
$\overline{\text{CMS}}$	1	O	Combined Memory Select Output
$\overline{\text{RD}}$	1	O	Memory Read Enable Output
$\overline{\text{WR}}$	1	O	Memory Write Enable Output
$\overline{\text{IRQ2/}}$	1	I	Edge- or Level-Sensitive Interrupt Request ¹
PF7		I/O	Programmable I/O Pin
$\overline{\text{IRQ1/}}$	1	I	Level-Sensitive Interrupt Requests ¹
PF6		I/O	Programmable I/O Pin
$\overline{\text{IRQ0/}}$	1	I	Level-Sensitive Interrupt Requests ¹
PF5		I/O	Programmable I/O Pin
$\overline{\text{IRQE/}}$	1	I	Edge-Sensitive Interrupt Requests ¹
PF4		I/O	Programmable I/O Pin
Mode D ² /	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF3		I/O	Programmable I/O Pin During Normal Operation
Mode C/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF2		I/O	Programmable I/O Pin During Normal Operation
Mode B/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF1		I/O	Programmable I/O Pin During Normal Operation
Mode A/	1	I	Mode Select Input—Checked Only During $\overline{\text{RESET}}$
PF0		I/O	Programmable I/O Pin During Normal Operation
CLKIN	1	I	Clock Input
XTAL	1	O	Quartz Crystal Output
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1/	5	I/O	Serial Port I/O Pins
$\overline{\text{IRQ1}}-\text{O, FI, FO}$			Edge- or Level-Sensitive Interrupts, FI, FO ³
$\overline{\text{PWD}}$	1	I	Power-Down Control Input
PWDACK	1	O	Power-Down Acknowledge Control Output
FL0, FL1, FL2	3	O	Output Flags
V_{DDINT}	2	I	Internal V_{DD} (1.8 V) Power (LQFP)
V_{DDEXT}	4	I	External V_{DD} (1.8 V, 2.5 V, or 3.3 V) Power (LQFP)
GND	10	I	Ground (LQFP)

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Table 9. Common-Mode Pins (Continued)

Pin Name	No. of Pins	I/O	Function
V _{DDINT}	4	I	Internal V _{DD} (3.3 V) Power (BGA)
V _{DDEXT}	7	I	External V _{DD} (3.3 V) Power (BGA)
GND	20	I	Ground (BGA)
EZ-Port	9	I/O	For Emulation Use

¹ Interrupt/Flag pins retain both functions concurrently. If IMASK is set to enable the corresponding interrupts, the DSP will vector to the appropriate interrupt vector address when the pin is asserted, either by external devices or set as a programmable flag.

² This mode applies to the ADSP-2187L only.

³ SPORT configuration determined by the DSP System Control Register. Software configurable.

MEMORY INTERFACE PINS

ADSP-218xL series members can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities.

The operating mode is determined by the state of the Mode C pin during RESET and cannot be changed while the processor is running. [Table 10](#) and [Table 11](#) list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode that is set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinouts in [Table 29 on Page 44](#) and [Table 30 on Page 45](#).

Table 10. Full Memory Mode Pins (Mode C = 0)

Pin Name	No. of Pins	I/O	Function
A13–0	14	O	Address Output Pins for Program, Data, Byte, and I/O Spaces
D23–0	24	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.)

Table 11. Host Mode Pins (Mode C = 1)

Pin Name	No. of Pins	I/O	Function
IAD15–0	16	I/O	IDMA Port Address/Data Bus
A0	1	O	Address Pin for External I/O, Program, Data, or Byte Access ¹
D23–8	16	I/O	Data I/O Pins for Program, Data, Byte, and I/O Spaces
$\overline{\text{IWR}}$	1	I	IDMA Write Enable
$\overline{\text{IRD}}$	1	I	IDMA Read Enable
IAL	1	I	IDMA Address Latch Pin
$\overline{\text{IS}}$	1	I	IDMA Select
$\overline{\text{IACK}}$	1	O	IDMA Port Acknowledge Configurable in Mode D ² ; Open Drain

¹ In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

² Mode D function available on ADSP-2187L only.

TERMINATING UNUSED PINS

Table 12 shows the recommendations for terminating unused pins.

Table 12. Unused Pin Terminations

Pin Name ¹	I/O 3-State (Z) ²	Reset State	High-Z ³ Caused By	Unused Configuration
XTAL	O	O		Float
CLKOUT	O	O		Float ⁴
A13–1 or IAD12–0	O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
A0	I/O (Z)	High-Z	$\overline{IS}$	Float
	O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
D23–8	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
D7 or $\overline{IWR}$	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
	I	I		High (Inactive)
D6 or $\overline{IRD}$	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
	I	I	$\overline{BR}$, $\overline{EBR}$	High (Inactive)
D5 or IAL	I/O (Z)	High-Z		Float
	I	I		Low (Inactive)
D4 or $\overline{IS}$	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
	I	I		High (Inactive)
D3 or $\overline{IACK}$	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
				Float
D2–0 or IAD15–13	I/O (Z)	High-Z	$\overline{BR}$, $\overline{EBR}$	Float
	I/O (Z)	High-Z	$\overline{IS}$	Float
$\overline{PMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{DMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{IOMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{CMS}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{RD}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{WR}$	O (Z)	O	$\overline{BR}$, $\overline{EBR}$	Float
$\overline{BR}$	I	I		High (Inactive)
$\overline{BG}$	O (Z)	O	EE	Float
$\overline{BGH}$	O	O		Float
$\overline{IRQ2}/PF7$	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float ⁵
$\overline{IRQ1}/PF6$	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float ⁵
$\overline{IRQ0}/PF5$	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float ⁵
$\overline{IRQE}/PF4$	I/O (Z)	I		Input = High (Inactive) or Program as Output, Set to 1, Let Float ⁵
$\overline{PWD}$	I	I		High
SCLK0	I/O	I		Input = High or Low, Output = Float
RFS0	I/O	I		High or Low
DR0	I	I		High or Low
TFS0	I/O	I		High or Low
DT0	O	O		Float

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Table 12. Unused Pin Terminations (Continued)

Pin Name ¹	I/O 3-State (Z) ²	Reset State	High-Z ³ Caused By	Unused Configuration
SCLK1	I/O	I		Input = High or Low, Output = Float
RFS1/ $\overline{\text{IRQ0}}$	I/O	I		High or Low
DR1/FI	I	I		High or Low
TFS1/ $\overline{\text{IRQ1}}$	I/O	I		High or Low
DT1/FO	O	O		Float
EE	I	I		Float
$\overline{\text{EBR}}$	I	I		Float
$\overline{\text{EBG}}$	O	O		Float
$\overline{\text{ERESET}}$	I	I		Float
$\overline{\text{EMS}}$	O	O		Float
$\overline{\text{EINT}}$	I	I		Float
ECLK	I	I		Float
ELIN	I	I		Float
ELOUT	O	O		Float

¹ CLKIN, $\overline{\text{RESET}}$, and PF3–0/Mode D–A are not included in this table because these pins must be used.

² All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is High-Z (high impedance) when inactive.

³ High-Z = high impedance.

⁴ If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.

⁵ If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1 prior to enabling interrupts, and let pins float.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

SPECIFICATIONS

OPERATING CONDITIONS

Parameter ¹	K Grade (Commercial)		B Grade (Industrial)		Unit
	Min	Max	Min	Max	
V _{DD}	3.0	3.6	3.0	3.6	V
T _{AMB}	0	+70	-40	+85	°C

¹ Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS

Parameter ¹	Description	Test Conditions	K and B Grades			Unit
			Min	Typ	Max	
V _{IH}	Hi-Level Input Voltage ^{2, 3}	@ V _{DD} = Max	2.0			V
		@ V _{DD} = Max	2.2			V
V _{IL}	Lo-Level Input Voltage ^{2, 3}	@ V _{DD} = Min			0.8	V
V _{OH}	Hi-Level Output Voltage ^{2, 4, 5}	@ V _{DD} = Min, I _{OH} = -0.5 mA	1.35			V
		@ V _{DD} = Min, I _{OH} = -100 μA ⁶	V _{DD} - 0.3			V
V _{OL}	Lo-Level Output Voltage ^{2, 4, 5}	@ V _{DD} = Min, I _{OL} = 2.0 mA			0.4	V
I _{IH}	Hi-Level Input Current ³	@ V _{DD} = Max, V _{IN} = V _{DD} Max			10	μA
I _{IL}	Lo-Level Input Current ³	@ V _{DD} = Max, V _{IN} = 0 V			10	μA
I _{OZH}	Three-State Leakage Current ⁷	@ V _{DD} = Max, V _{IN} = V _{DD} Max ⁸			10	μA
I _{OZL}	Three-State Leakage Current ⁷	@ V _{DD} = Max, V _{IN} = 0 V ⁸			10	μA
C _I	Input Pin Capacitance ^{3, 6}	@ V _{IN} = 3.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C			8	pF
C _O	Output Pin Capacitance ^{6, 7, 9}	@ V _{IN} = 2.5 V, f _{IN} = 1.0 MHz, T _{AMB} = 25°C			8	pF

¹ Specifications subject to change without notice.

² Bidirectional pins: D23-0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13-1, PF7-0.

³ Input only pins: CLKIN, RESET, BR, DR0, DR1, PWD.

⁴ Output pins: BG, PMS, DMS, BMS, IOMS, CMS, RD, WR, PWDACK, A0, DT0, DT1, CLKOUT, FL2-FL0, BGH.

⁵ Although specified for TTL outputs, all ADSP-218xL outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

⁶ Guaranteed but not tested.

⁷ Three-statable pins: A13-A1, D23-D0, PMS, DMS, BMS, IOMS, CMS, RD, WR, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF7-PF0.

⁸ 0 V on BR.

⁹ Output pin capacitance is the capacitive load for any three-stated output pin.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage (V_{DD})	–0.3 V to +4.6 V
Input Voltage ¹	–0.5 V to $V_{DD} + 0.5$ V
Output Voltage Swing ²	–0.5 V to $V_{DD} + 0.5$ V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

¹ Applies to bidirectional pins (D23–0, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A13–1, PF7–0) and input only pins (CLKIN, RESET, $\overline{BR}$, DR0, DR1, PWD).

² Applies to output pins (BG, PMS, DMS, BMS, IOMS, CMS, RD, WR, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, BGH).

PACKAGE INFORMATION

The information presented in [Figure 15](#) provides details about the package branding for the ADSP-218xL processors. For a complete listing of product availability, see [Ordering Guide on Page 47](#).



Figure 15. Typical Package Brand

Table 13. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	RoHs Compliant Option (optional)
cc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

ESD SENSITIVITY



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

General Notes

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added up meaningfully to derive longer times.

Timing Notes

Switching characteristics specify how the processor changes its signals. Designers have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Frequency Dependency For Timing Specifications

t_{CK} is defined as $0.5 t_{CKI}$. The ADSP-218xL uses an input clock with a frequency equal to half the instruction rate. For example, a 26 MHz input clock (which is equivalent to 38 ns) yields a 19 ns processor cycle (equivalent to 52 MHz). t_{CK} values within the range of $0.5 t_{CKI}$ period should be substituted for all relevant timing parameters to obtain the specification value.

Example: $t_{CKH} = 0.5 t_{CK} - 7 \text{ ns} = 0.5 (19) - 7 \text{ ns} = 2.5 \text{ ns}$

Clock Signals and Reset

Table 14. Clock Signals and Reset

Parameter		ADSP-2184L, ADSP-2186L		ADSP-2185L, ADSP-2187L		Unit
		Min	Max	Min	Max	
Timing Requirements:						
t _{CKI}	CLKIN Period	50	150	38	100	ns
t _{CKIL}	CLKIN Width Low	20		15		ns
t _{CKIH}	CLKIN Width High	20		15		ns
Switching Characteristics:						
t _{CKL}	CLKOUT Width Low	0.5t _{CK} – 7		0.5t _{CK} – 7		ns
t _{CKH}	CLKOUT Width High	0.5t _{CK} – 7		0.5t _{CK} – 7		ns
t _{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	ns
Control Signals Timing Requirements:						
t _{RSP}	$\overline{\text{RESET}}$ Width Low ¹	5t _{CK}		5t _{CK}		ns
t _{MS}	Mode Setup Before $\overline{\text{RESET}}$ High	2		2		ns
t _{MH}	Mode Hold After $\overline{\text{RESET}}$ High	5		5		ns

¹ Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator start-up time).

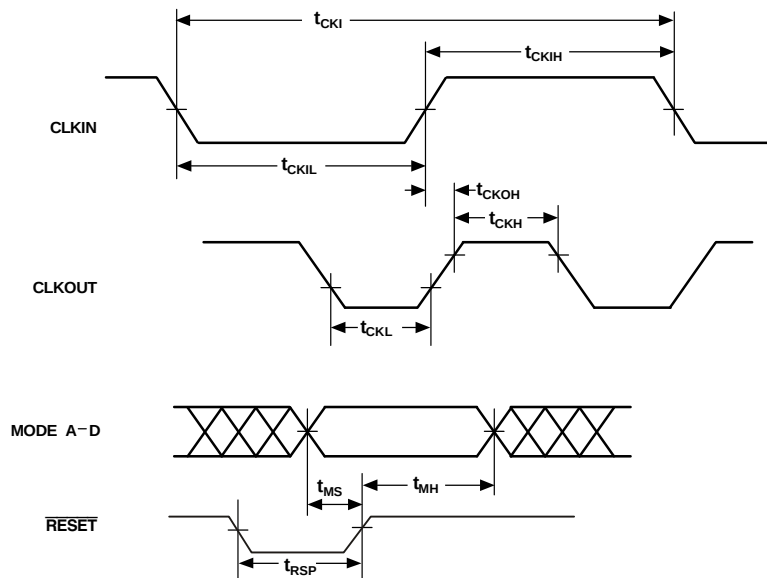


Figure 16. Clock Signals and Reset

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Interrupts and Flags

Table 15. Interrupts and Flags

Parameter	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{IFS} $\overline{IRQx}$, FI, or PFx Setup Before CLKOUT Low ^{1, 2, 3, 4}	$0.25t_{CK} + 15$		ns
t_{IFH} $\overline{IRQx}$, FI, or PFx Hold After CLKOUT High ^{1, 2, 3, 4}	$0.25t_{CK}$		ns
<i>Switching Characteristics:</i>			
t_{FOH} Flag Output Hold After CLKOUT Low ⁵	$0.5t_{CK} - 5$		ns
t_{FOD} Flag Output Delay From CLKOUT Low ⁵		$0.5t_{CK} + 4$	ns

¹ If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the *Program Control* chapter of the *ADSP-218x DSP Hardware Reference* for further information on interrupt servicing.)

² Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

³ $\overline{IRQx} = \overline{IRQ0}, \overline{IRQ1}, \overline{IRQ2}, \overline{IRQL0}, \overline{IRQL1}, \overline{IRQLE}$.

⁴ PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.

⁵ Flag Outputs = PFx, FL0, FL1, FL2, FO.

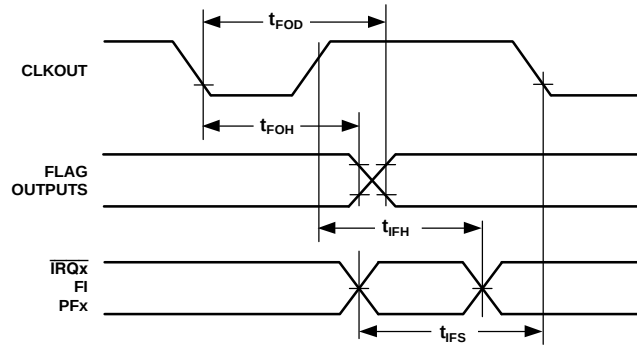


Figure 17. Interrupts and Flags

Bus Request—Bus Grant

Table 16. Bus Request—Bus Grant

Parameter	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{BH} $\overline{BR}$ Hold After CLKOUT High ¹	$0.25t_{CK} + 2$		ns
t_{BS} $\overline{BR}$ Setup Before CLKOUT Low ¹	$0.25t_{CK} + 17$		ns
<i>Switching Characteristics:</i>			
t_{SD} CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable ²		$0.25t_{CK} + 10$	ns
t_{SDB} $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE} $\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC} $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High ³	$0.25t_{CK} - 7$		ns
t_{SDBH} $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low ⁴	0		ns
t_{SEH} $\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable ⁴	0		ns

¹ $\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$ / $\overline{BG}$ cycle relationships.

² $\overline{xMS} = \overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

³ For the ADSP-2187L, this specification is $0.25t_{CK} - 4$ ns min.

⁴ $\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

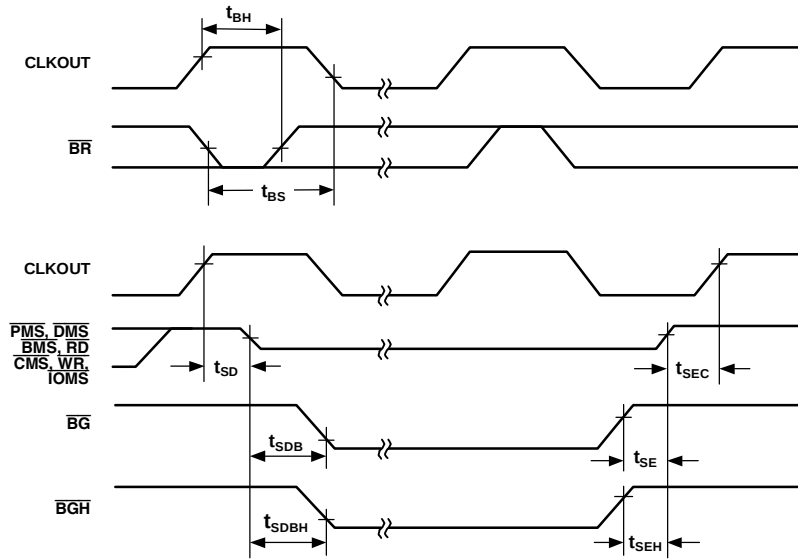


Figure 18. Bus Request—Bus Grant

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Memory Read

Table 17. Memory Read

Parameter		Min	Max	Unit
<i>Timing Requirements:</i>				
t_{RDD}	$\overline{RD}$ Low to Data Valid ¹		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A13-0, $\overline{xMS}$ to Data Valid ²		$0.75t_{CK} - 12.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High ³	1		ns
<i>Switching Characteristics:</i>				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A13-0, $\overline{xMS}$ Setup Before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A13-0, $\overline{xMS}$ Hold After $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

¹ $w = \text{wait states} \times t_{CK}$.

² $\overline{xMS} = \overline{PMS}, \overline{DMS}, \overline{CMS}, \overline{IOMS}, \overline{BMS}$.

³ For the ADSP-2187L, this specification is 0 ns min.

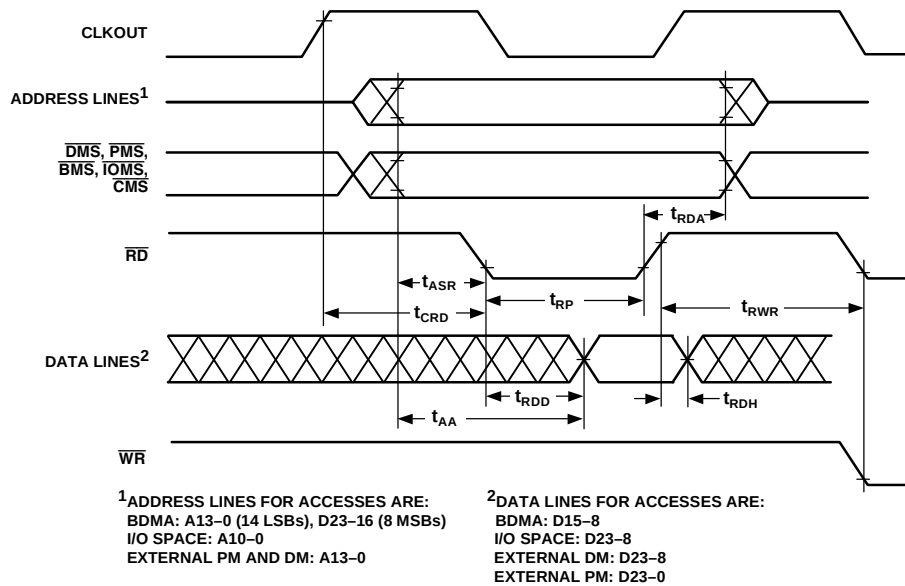


Figure 19. Memory Read

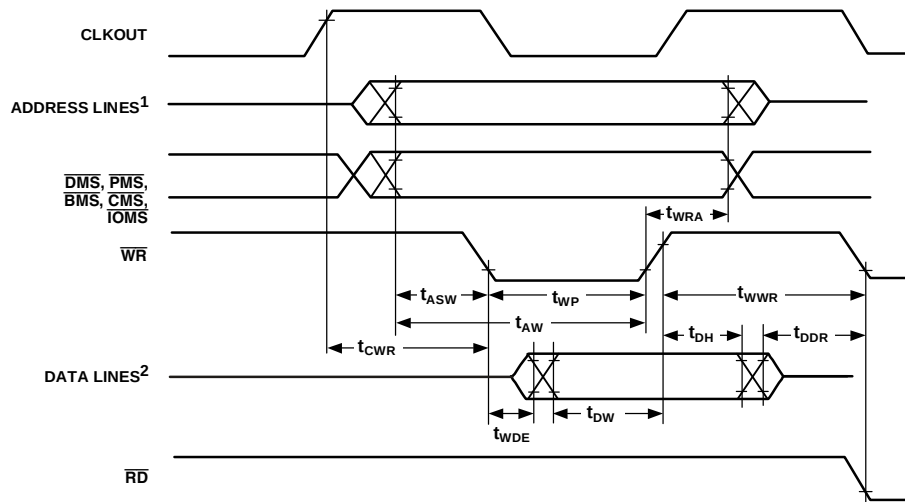
Memory Write

Table 18. Memory Write

Parameter		Min	Max	Unit
<i>Switching Characteristics:</i>				
t_{DW}	Data Setup Before $\overline{WR}$ High ¹	$0.5t_{CK} - 7 + w$		ns
t_{DH}	Data Hold After $\overline{WR}$ High	$0.25t_{CK} - 2$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A13-0, $\overline{xMS}$ Setup Before $\overline{WR}$ Low ²	$0.25t_{CK} - 6$		ns
t_{DDR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 7$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{AW}	A13-0, $\overline{xMS}$ Setup Before $\overline{WR}$ Deasserted	$0.75t_{CK} - 9 + w$		ns
t_{WRA}	A13-0, $\overline{xMS}$ Hold After $\overline{WR}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

¹ $w = \text{wait states} \times t_{CK}$.

² $\overline{xMS} = \overline{PMS}, \overline{DMS}, \overline{CMS}, \overline{IOMS}, \overline{BMS}$.



¹ ADDRESS LINES FOR ACCESSES ARE:
BDMA: A13-0 (14 LSBs), D23-16 (8 MSBs)
I/O SPACE: A10-0
EXTERNAL PM AND DM: A13-0

² DATA LINES FOR ACCESSES ARE:
BDMA: D15-8
I/O SPACE: D23-8
EXTERNAL DM: D23-8
EXTERNAL PM: D23-0

Figure 20. Memory Write

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

Serial Ports

Table 19. Serial Ports

Parameter	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{SCK} SCLK Period ¹	50		ns
t_{SCS} DR/TFS/RFS Setup Before SCLK Low	4		ns
t_{SCH} DR/TFS/RFS Hold After SCLK Low ²	8		ns
t_{SCP} SCLKIN Width ³	20		ns
<i>Switching Characteristics:</i>			
t_{CC} CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE} SCLK High to DT Enable	0		ns
t_{SCDV} SCLK High to DT Valid		15	ns
t_{RH} TFS/RFS _{OUT} Hold After SCLK High	0		ns
t_{RD} TFS/RFS _{OUT} Delay from SCLK High		15	ns
t_{SCDH} DT Hold after SCLK High	0		ns
t_{TDE} TFS (Alt) to DT Enable	0		ns
t_{TDV} TFS (Alt) to DT Valid		14	ns
t_{SCDD} SCLK High to DT Disable		15	ns
t_{RDV} RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

¹ For the ADSP-2187L, this specification is 38 ns min.

² For the ADSP-2187L, this specification is 7 ns min.

³ For the ADSP-2185L, and the ADSP-2187L, this specification is 15 ns min.

The timing diagram illustrates the relationship between several signals and their timing parameters:

- CLKOUT**: Shows two clock periods with period t_{CC} .
- SCLK**: Shows a clock signal with period t_{SCK} , setup time t_{SCP} , and hold time t_{SCH} .
- DR**: Data Register output signal.
- TFS_{IN}** and **RFS_{IN}**: Input signals for frame and range synchronization.
- RFS_{OUT}** and **TFS_{OUT}**: Output signals for range and frame synchronization.
- DT**: Data Transfer signal.
- TFS_{OUT} ALTERNATE FRAME MODE**: Output signal for alternate frame mode.
- RFS_{OUT} MULTICHANNEL MODE, FRAME DELAY 0 (MFD = 0)**: Output signal for multichannel mode with zero frame delay.
- TFS_{IN} ALTERNATE FRAME MODE**: Input signal for alternate frame mode.
- RFS_{IN} MULTICHANNEL MODE, FRAME DELAY 0 (MFD = 0)**: Input signal for multichannel mode with zero frame delay.

Timing parameters shown include:

- t_{RD} : Read delay from **DR** to **RFS_{IN}**.
- t_{RH} : Read hold time from **RFS_{IN}** to **DR**.
- t_{SCDV} : Setup time from **SCLK** to **DR**.
- t_{SCDH} : Setup time from **SCLK** to **DT**.
- t_{SCDD} : Setup time from **SCLK** to **TFS_{OUT}**.
- t_{TDE} : Transfer delay from **DT** to **TFS_{OUT}**.
- t_{TDV} : Transfer delay from **DT** to **TFS_{IN}**.
- t_{RDV} : Read delay from **DR** to **RFS_{IN}**.

Rev. C | Page 29 of 48 | January 2008

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

IDMA Address Latch

Table 20. IDMA Address Latch

Parameter		Min	Max	Unit
<i>Timing Requirements:</i>				
t_{IALP}	Duration of Address Latch ^{1, 2}	10		ns
t_{IASU}	IAD15–0 Address Setup Before Address Latch End ²	5		ns
t_{IAH}	IAD15–0 Address Hold After Address Latch End ^{2, 3}	3		ns
t_{IKA}	$\overline{IACK}$ Low Before Start of Address Latch ^{2, 4}	0		ns
t_{IALS}	Start of Write or Read After Address Latch End ^{2, 4}	3		ns
t_{IALD}	Address Latch Start After Address Latch End ^{1, 2}	2		ns

¹ Start of Address Latch = $\overline{IS}$ Low and IAL High.

² End of Address Latch = $\overline{IS}$ High or IAL Low.

³ For the ADSP-2187L, this specification is 2 ns min.

⁴ Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

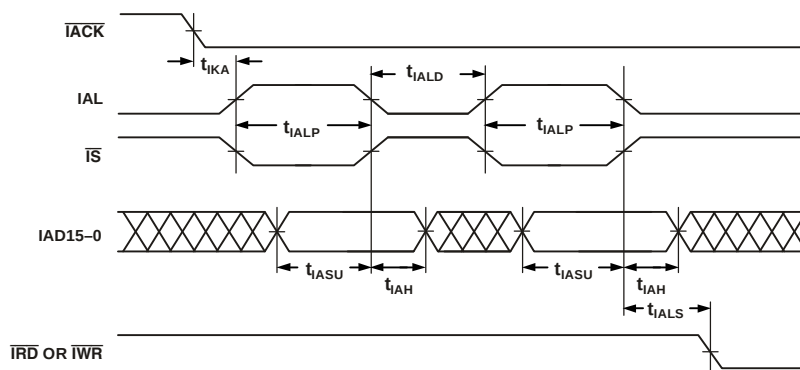


Figure 22. IDMA Address Latch

IDMA Write, Short Write Cycle

Table 21. IDMA Write, Short Write Cycle

Parameter	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{IKW} $\overline{IACK}$ Low Before Start of Write ¹	0		ns
t_{IWP} Duration of Write ^{1, 2}	15		ns
t_{IDSU} IAD15–0 Data Setup Before End of Write ^{2, 3, 4}	5		ns
t_{IDH} IAD15–0 Data Hold After End of Write ^{2, 3, 4}	2		ns
<i>Switching Characteristic:</i>			
t_{IKHW} Start of Write to $\overline{IACK}$ High ⁵		17	ns

¹ Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.

² End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.

³ If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU} , t_{IDH} .

⁴ If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU} , t_{IKH} .

⁵ For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

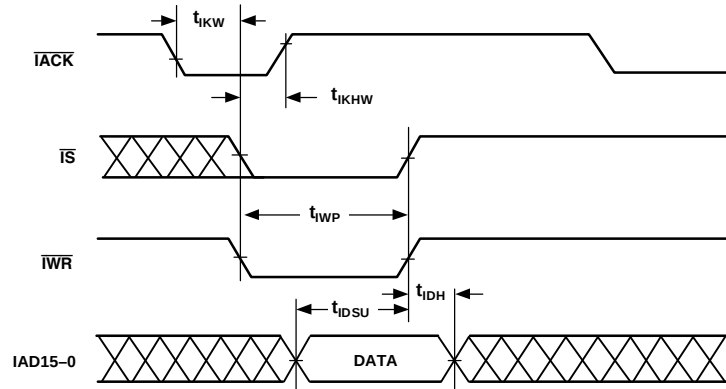


Figure 23. IDMA Write, Short Write Cycle

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

IDMA Write, Long Write Cycle

Table 22. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
<i>Timing Requirements:</i>				
t_{IKW}	$\overline{IACK}$ Low Before Start of Write ¹	0		ns
t_{IKSU}	IAD15–0 Data Setup Before End of Write ^{2, 3, 4}	$0.5t_{CK} + 10$		ns
t_{IKH}	IAD15–0 Data Hold After End of Write ^{2, 3, 4}	2		ns
<i>Switching Characteristics:</i>				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low ⁴	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High ⁵		17	ns

¹ Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.

² If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IKSU} , t_{IKH} .

³ If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU} , t_{IKH} .

⁴ This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

⁵ For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

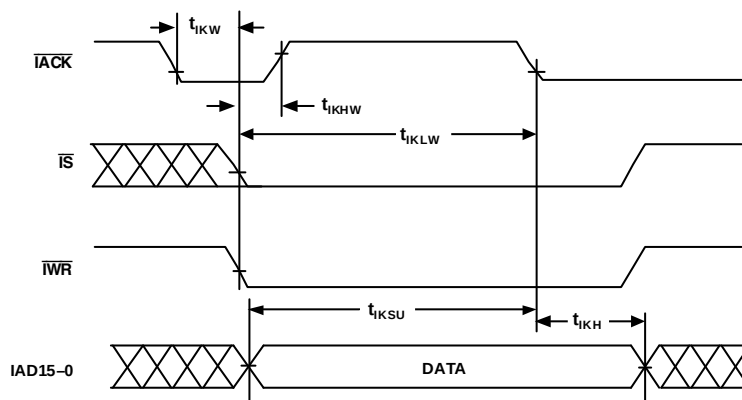


Figure 24. IDMA Write, Long Write Cycle

IDMA Read, Long Read Cycle

Table 23. IDMA Read, Long Read Cycle

Parameter	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{IKR} $\overline{IACK}$ Low Before Start of Read ¹	0		ns
t_{IRK} End of Read After $\overline{IACK}$ Low ²	2		ns
<i>Switching Characteristics:</i>			
t_{IKHR} $\overline{IACK}$ High After Start of Read ^{1, 3}		17	ns
t_{IKDS} IAD15-0 Data Setup Before $\overline{IACK}$ Low	$0.5t_{CK} - 10$		ns
t_{IKDH} IAD15-0 Data Hold After End of Read ²	0		ns
t_{IKDD} IAD15-0 Data Disabled After End of Read ²		10	ns
t_{IRDE} IAD15-0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV} IAD15-0 Previous Data Valid After Start of Read ⁴		15	ns
t_{IRDH1} IAD15-0 Previous Data Hold After Start of Read (DM/PM1) ⁵	$2t_{CK} - 5$		ns
t_{IRDH2} IAD15-0 Previous Data Hold After Start of Read (PM2) ⁶	$t_{CK} - 5$		ns

¹ Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.

² End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

³ For the ADSP-2185L, and the ADSP-2187L, this specification is 4 ns min., and 15 ns max.

⁴ For the ADSP-2187L, this specification is 10 ns max.

⁵ DM read or first half of PM read.

⁶ Second half of PM read.

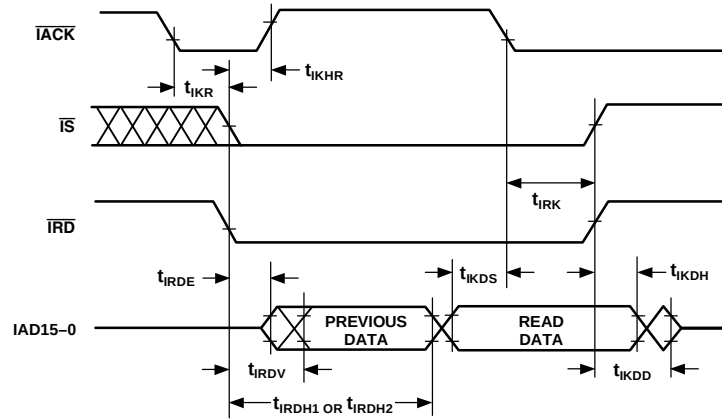


Figure 25. IDMA Read, Long Read Cycle

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

IDMA Read, Short Read Cycle

Table 24. IDMA Read, Short Read Cycle

Parameter ^{1,2}		Min	Max	Unit
<i>Timing Requirements:</i>				
t_{IKR}	$\overline{IACK}$ Low Before Start of Read ³	0		ns
t_{IRP1}	Duration of Read (DM/PM1) ^{4,5}	15		ns
t_{IRP2}	Duration of Read (PM2) ^{6,7}	15		ns
<i>Switching Characteristics:</i>				
t_{IKHR}	$\overline{IACK}$ High After Start of Read ³		15	ns
t_{IKDH}	IAD15–0 Data Hold After End of Read ⁸	0		ns
t_{IKDD}	IAD15–0 Data Disabled After End of Read ⁸		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid After Start of Read		15	ns

¹ Short Read Only must be disabled in the IDMA overlay memory mapped register. This mode is disabled by clearing (=0) Bit 14 of the IDMA overlay register, and is disabled by default upon reset.

² Consider using the Short Read Only mode, instead, because Short Read mode is not applicable at high clock frequencies.

³ Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.

⁴ DM Read or first half of PM Read.

⁵ For the ADSP-2186L, this specification also has a max value of $2t_{CK} - 5$.

⁶ Second half of PM Read.

⁷ For the ADSP-2186L, this specification also has a max value of $t_{CK} - 5$ max.

⁸ End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

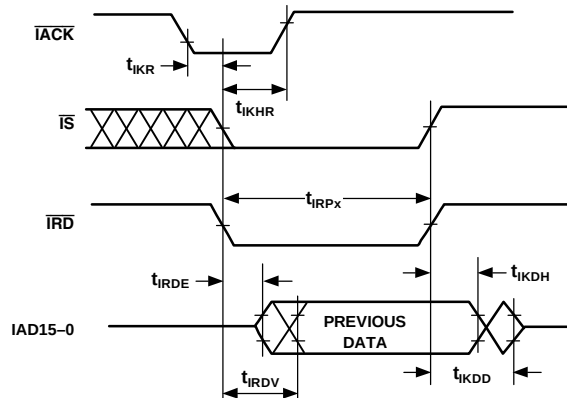


Figure 26. IDMA Read, Short Read Cycle

IDMA Read, Short Read Cycle in Short Read Only Mode

Table 25. IDMA Read, Short Read Cycle in Short Read Only Mode¹

Parameter ²	Min	Max	Unit
<i>Timing Requirements:</i>			
t_{IKR} $\overline{IACK}$ Low Before Start of Read ³	0		ns
t_{IRP} Duration of Read ⁴	10		ns
<i>Switching Characteristics:</i>			
t_{IKHR} $\overline{IACK}$ High After Start of Read ³		10	ns
t_{IKDH} IAD15–0 Previous Data Hold After End of Read ⁴	0		ns
t_{IKDD} IAD15–0 Previous Data Disabled After End of Read ⁴		10	ns
t_{IRDE} IAD15–0 Previous Data Enabled After Start of Read	0		ns
t_{IRDV} IAD15–0 Previous Data Valid After Start of Read		10	ns

¹ Applies to the ADSP-2187L only.

² Short Read Only is enabled by setting Bit 14 of the IDMA overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.

³ Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.

⁴ End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

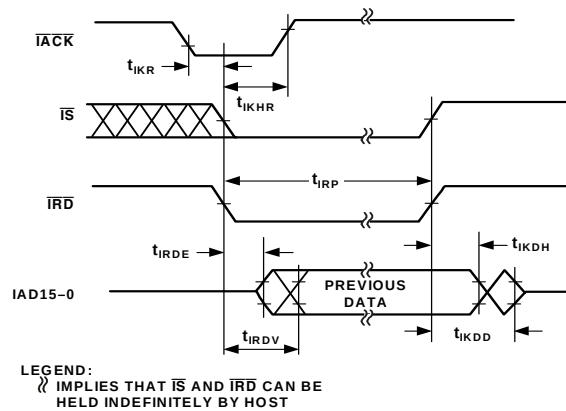


Figure 27. IDMA Read, Short Read Cycle in Short Read Only Mode

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

POWER SUPPLY CURRENT

Table 26. Power Supply Current¹

Parameter	Test Conditions	Min	Typ	Max	Unit
<i>ADSP-2184L</i>					
I_{DD} Supply Current (Idle) ²	@ $V_{DD} = 3.3\text{ V}^4$		8.6		mA
I_{DD} Supply Current (Dynamic) ³	@ $V_{DD} = 3.3$, $T_{AMB} = 25^\circ\text{C}$, $t_{CK} = 25\text{ ns}^4$		42		mA
<i>ADSP-2185L</i>					
I_{DD} Supply Current (Idle) ²	@ $V_{DD} = 3.3\text{ V}^4$				
	$t_{CK} = 19\text{ ns}$		8.6		mA
	$t_{CK} = 25\text{ ns}$		7.0		mA
	$t_{CK} = 30\text{ ns}$		6.0		mA
I_{DD} Supply Current (Dynamic) ³	@ $V_{DD} = 3.3\text{ V}$, $T_{AMB} = 25^\circ\text{C}^4$				
	$t_{CK} = 19\text{ ns}$		49		mA
	$t_{CK} = 25\text{ ns}$		38		mA
	$t_{CK} = 30\text{ ns}$		31.5		mA
<i>ADSP-2186L</i>					
I_{DD} Supply Current (Idle) ²	@ $V_{DD} = 3.3\text{ V}^4$		8.6		mA
I_{DD} Supply Current (Dynamic) ³	@ $V_{DD} = 3.3\text{ V}$, $T_{AMB} = 25^\circ\text{C}$, $t_{CK} = 25\text{ ns}^4$		42		mA
<i>ADSP-2187L</i>					
I_{DD} Supply Current (Idle) ²	@ $V_{DD} = 3.3\text{ V}^4$				
	$t_{CK} = 19\text{ ns}$		10		mA
	$t_{CK} = 25\text{ ns}$		8		mA
	$t_{CK} = 30\text{ ns}$		7		mA
I_{DD} Supply Current (Dynamic) ³	@ $V_{DD} = 3.3\text{ V}$, $T_{AMB} = 25^\circ\text{C}^4$				
	$t_{CK} = 19\text{ ns}$		51		mA
	$t_{CK} = 25\text{ ns}$		41		mA
	$t_{CK} = 30\text{ ns}$		34		mA

¹ Specifications subject to change without notice.

² Idle refers to ADSP-218xL state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

³ I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

⁴ $V_{IN} = 0\text{ V}$ and 3 V .

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

where:

C is load capacitance.

f is the output switching frequency.

Example: In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- Application operates at $V_{DD} = 3.3$ V and $t_{CK} = 30$ ns.

$$\text{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

where:

P_{INT} is the internal power dissipation from [Figure 28](#) through [Figure 31 on Page 39](#).

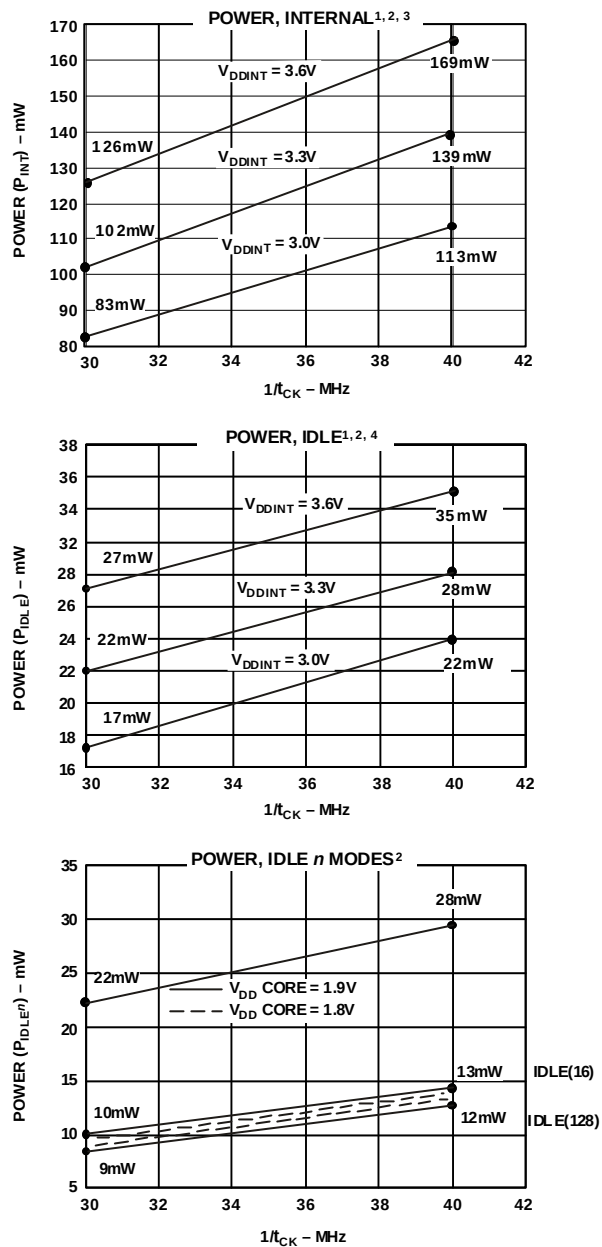
$(C \times V_{DD}^2 \times f)$ is calculated for each output, as in the example in [Table 27](#).

Table 27. Example Power Dissipation Calculation¹

Parameters	No. of Pins	$\times C$ (pF)	$\times V_{DD}^2$ (V)	$\times f$ (MHz)	PD (mW)
Address, $\overline{DMS}$	8	10	3.3^2	33.3	29.0
Data Output, $\overline{WR}$	9	10	3.3^2	16.67	16.3
$\overline{RD}$	1	10	3.3^2	16.67	1.8
CLKOUT	1	10	3.3^2	33.3	3.6
					= 50.7

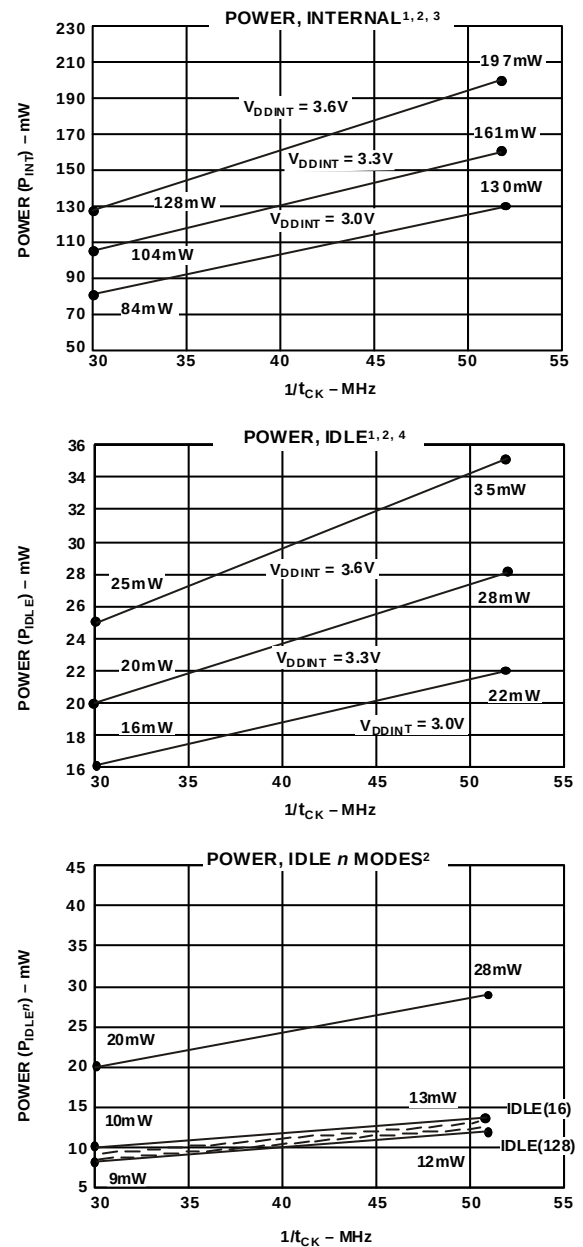
¹ Total power dissipation for this example is $P_{INT} + 50.7$ mW.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L



- NOTES**
 VALID FOR ALL TEMPERATURE GRADES.
 1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
 2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
 3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
 4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

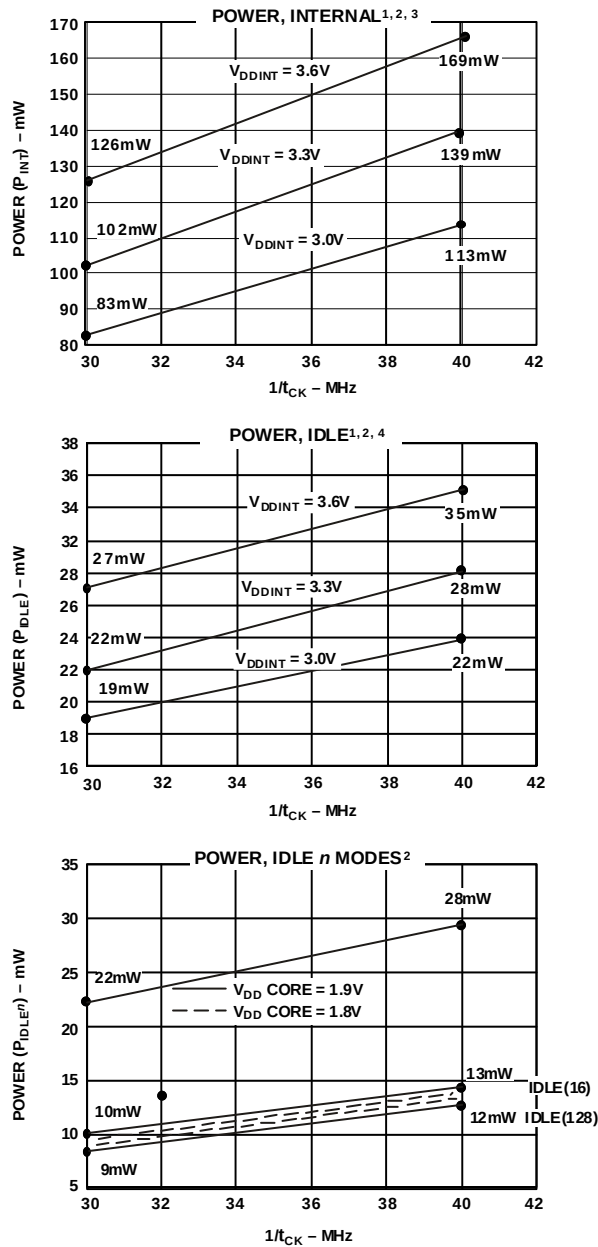
Figure 28. Power vs. Frequency (ADSP-2184L)



- NOTES**
 VALID FOR ALL TEMPERATURE GRADES.
 1. POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
 2. TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
 3. IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
 4. IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 29. Power vs. Frequency (ADSP-2185L)

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

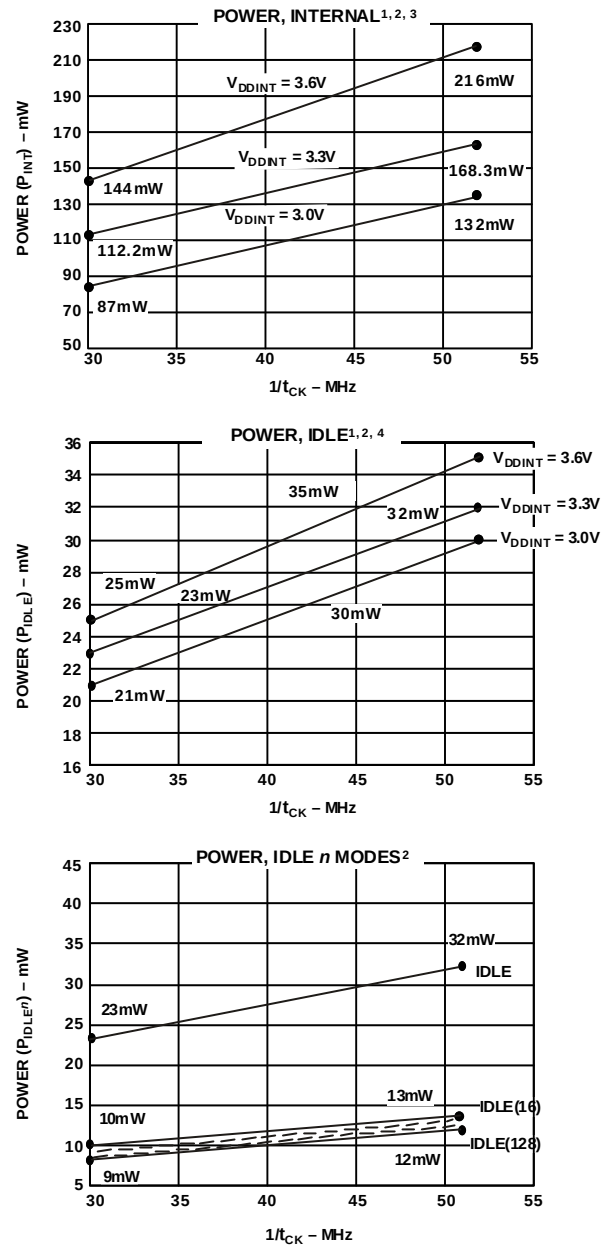


NOTES

VALID FOR ALL TEMPERATURE GRADES.

- POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
- TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
- IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
- IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 30. Power vs. Frequency (ADSP-2186L)



NOTES

VALID FOR ALL TEMPERATURE GRADES.

- POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
- TYPICAL POWER DISSIPATION AT 3.3V V_{DD} AND 25°C, EXCEPT WHERE SPECIFIED.
- IDD MEASUREMENT TAKEN WITH ALL INSTRUCTIONS EXECUTING FROM INTERNAL MEMORY. 50% OF THE INSTRUCTIONS ARE MULTIFUNCTION (TYPES 1, 4, 5, 12, 13, 14), 30% ARE TYPE 2 AND TYPE 6, AND 20% ARE IDLE INSTRUCTIONS.
- IDLE REFERS TO STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.

Figure 31. Power vs. Frequency (ADSP-2187L)

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

OUTPUT DRIVE CURRENTS

Figure 32 through Figure 35 show typical I-V characteristics for the output drivers on the ADSP-218xL processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

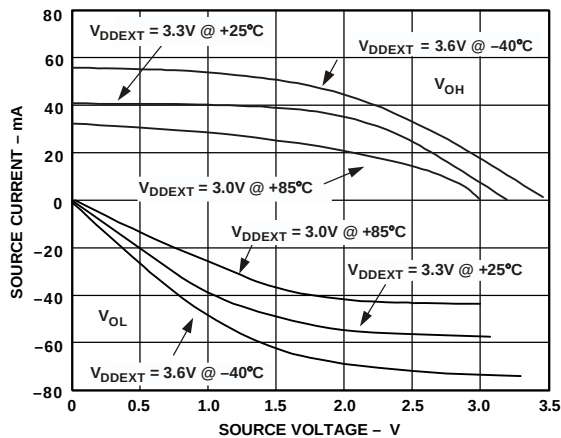


Figure 32. Typical Output Driver Characteristics (ADSP-2184L)

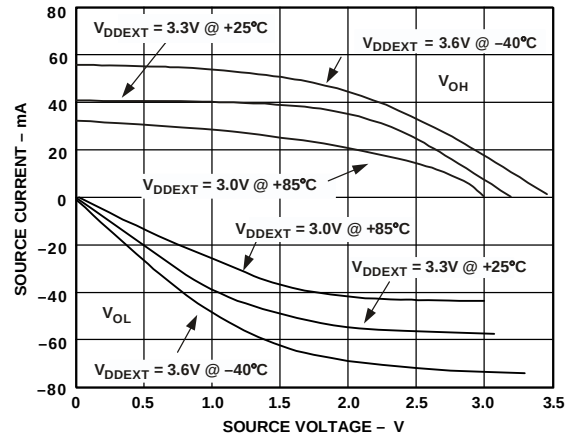


Figure 34. Typical Output Driver Characteristics (ADSP-2186L)

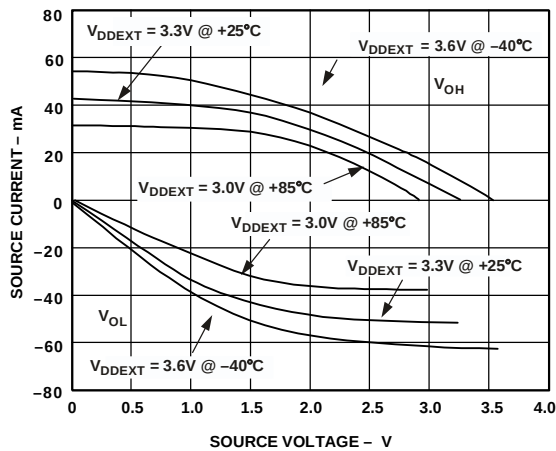


Figure 33. Typical Output Driver Characteristics (ADSP-2185L)

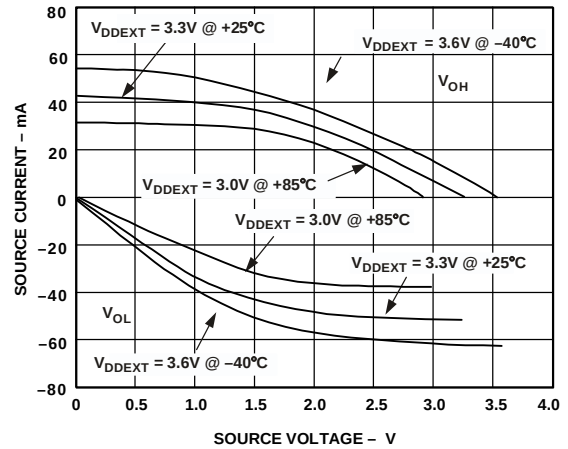


Figure 35. Typical Output Driver Characteristics (ADSP-2187L)

POWER-DOWN CURRENT

Figure 36 through Figure 39 show the typical power-down supply current. Note that these graphs reflect ADSP-218xL operation in lowest power mode. (See the “System Interface” chapter of the *ADSP-218x DSP Hardware Reference* for details). Current reflects device operating with no input loads.

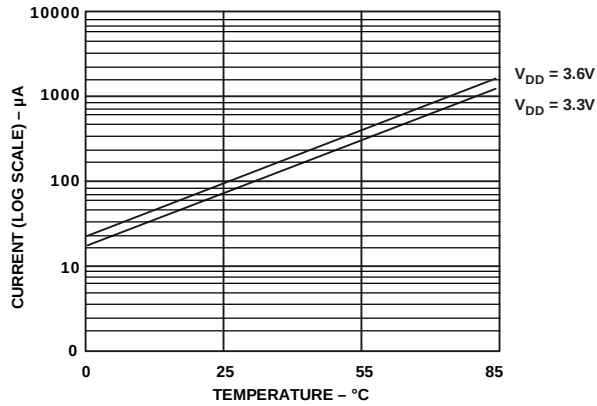


Figure 36. Typical Power-Down Current (ADSP-2184L)

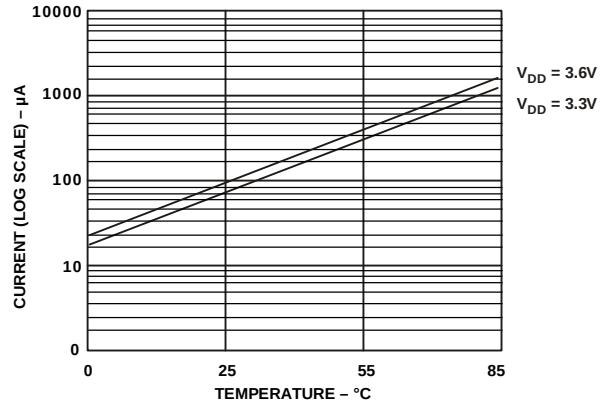


Figure 38. Typical Power-Down Current (ADSP-2186L)

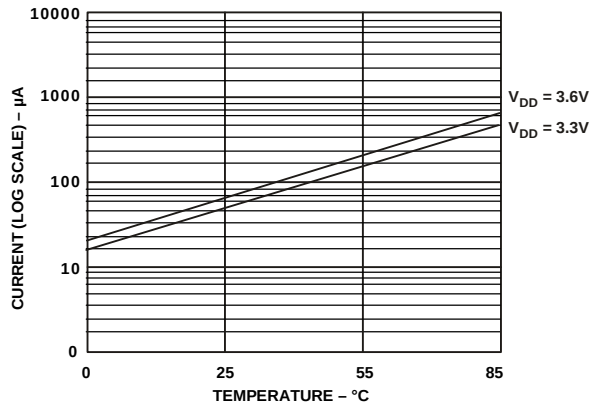


Figure 37. Typical Power-Down Current (ADSP-2185L)

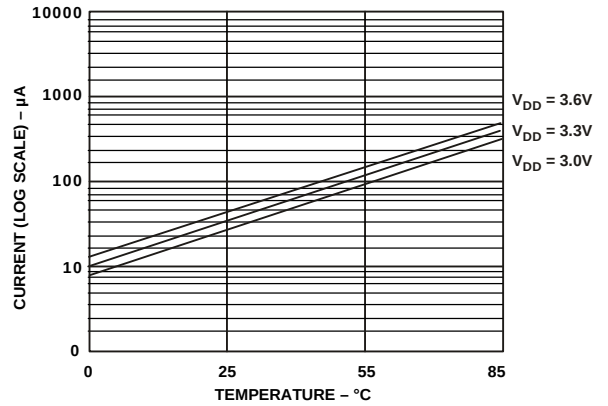


Figure 39. Typical Power-Down Current (ADSP-2187L)

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

CAPACITIVE LOADING – ADSP-2184L, ADSP-2186L

Figure 40 and Figure 41 show the capacitive loading characteristics of the ADSP-2184L and ADSP-2186L.

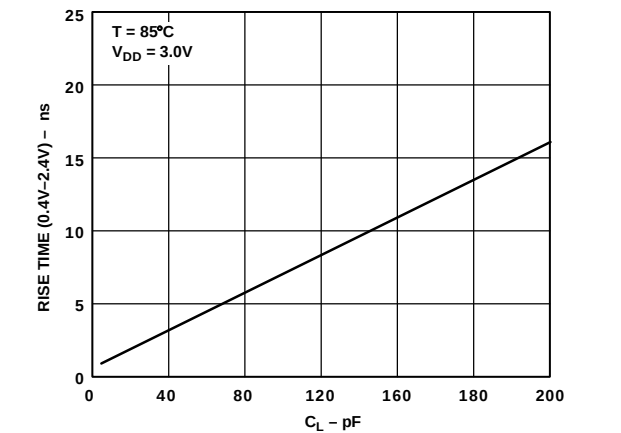


Figure 40. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

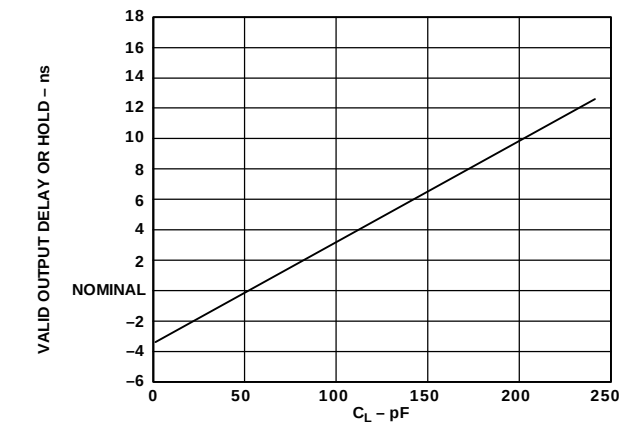


Figure 41. Typical Output Valid Delay or Hold vs. Load Capacitance, CL (at Maximum Ambient Operating Temperature)

CAPACITIVE LOADING – ADSP-2185L, ADSP-2187L

Figure 42 and Figure 43 show the capacitive loading characteristics of the ADSP-2185L and ADSP-2187L.

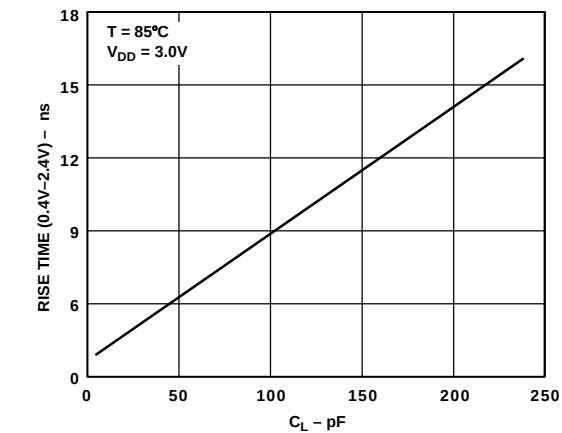


Figure 42. Typical Output Rise Time vs. Load Capacitance (at Maximum Ambient Operating Temperature)

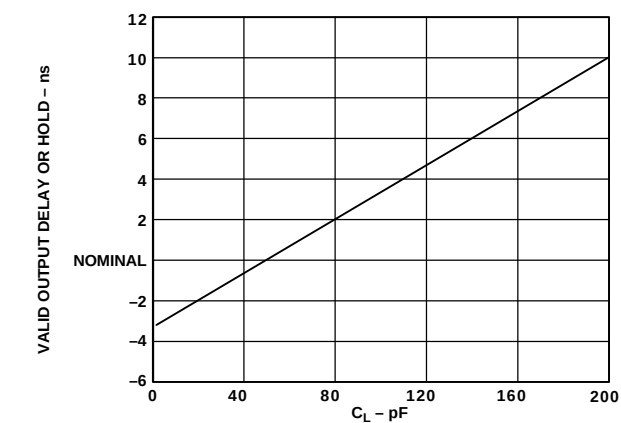


Figure 43. Typical Output Valid Delay or Hold vs. Load Capacitance, CL (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Figure 44 shows voltage reference levels for all ac measurements (except output disable/enable).

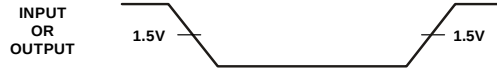


Figure 44. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY} , as shown in Figure 45. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY} , is dependent on the capacitive load, C_L , and the current load, i_L , on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 45. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

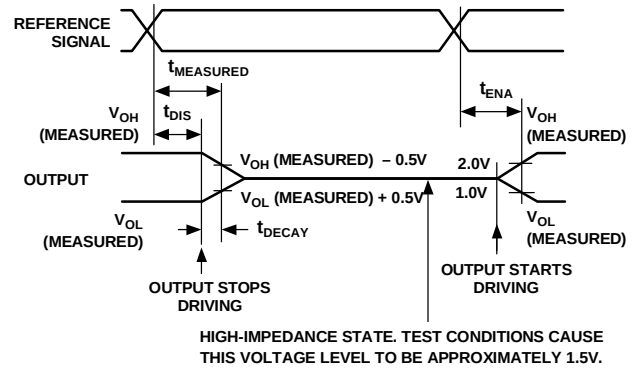


Figure 45. Output Enable/Disable

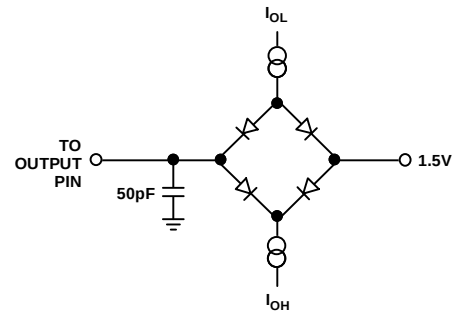


Figure 46. Equivalent Loading for AC Measurements (Including All Fixtures)

ENVIRONMENTAL CONDITIONS

Table 28. Thermal Resistance

Rating Description ¹	Symbol	LQFP (°C/W)	BGA (°C/W)
Thermal Resistance (Case-to-Ambient)	θ_{CA}	48	63.3
Thermal Resistance (Junction-to-Ambient)	θ_{JA}	50	70.7
Thermal Resistance (Junction-to-Case)	θ_{JC}	2	7.4

¹ Where the ambient temperature rating (T_{AMB}) is:

$$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$$

T_{CASE} = case temperature in °C

PD = power dissipation in W

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

LQFP PACKAGE PINOUT

The LQFP package pinout is shown in [Table 29](#). Pin names in bold text in the table replace the plain-text-named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value

of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/ $\overline{\text{IRQ1}}$, RFS1/ $\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default, upon reset.

Table 29. LQFP Pin Assignments

Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name	Lead No.	Lead Name
1	A4/ IAD3	26	$\overline{\text{IRQE}}$ + PF4	51	$\overline{\text{EBR}}$	76	D16
2	A5/ IAD4	27	$\overline{\text{IRQLO}}$ + PF5	52	$\overline{\text{BR}}$	77	D17
3	GND	28	GND	53	$\overline{\text{EBG}}$	78	D18
4	A6/ IAD5	29	$\overline{\text{IRQLT}}$ + PF6	54	$\overline{\text{BG}}$	79	D19
5	A7/ IAD6	30	$\overline{\text{IRQ2}}$ + PF7	55	D0/IAD13	80	GND
6	A8/ IAD7	31	DT0	56	D1/IAD14	81	D20
7	A9/ IAD8	32	TFS0	57	D2/IAD15	82	D21
8	A10/ IAD9	33	RFS0	58	D3/IACK	83	D22
9	A11/ IAD10	34	DR0	59	V _{DDINT}	84	D23
10	A12/ IAD11	35	SCLK0	60	GND	85	FL2
11	A13/ IAD12	36	V _{DDEXT}	61	D4/ $\overline{\text{IS}}$	86	FL1
12	GND	37	DT1/FO	62	D5/IAL	87	FL0
13	CLKIN	38	TFS1/ $\overline{\text{IRQ1}}$	63	D6/IRD	88	PF3 [Mode D ¹]
14	XTAL	39	RFS1/ $\overline{\text{IRQ0}}$	64	D7/IWR	89	PF2 [Mode C]
15	V _{DDEXT}	40	DR1/FI	65	D8	90	V _{DDEXT}
16	CLKOUT	41	GND	66	GND	91	$\overline{\text{PWD}}$
17	GND	42	SCLK1	67	V _{DDEXT}	92	GND
18	V _{DDINT}	43	$\overline{\text{ERESET}}$	68	D9	93	PF1 [Mode B]
19	$\overline{\text{WR}}$	44	$\overline{\text{RESET}}$	69	D10	94	PF0 [Mode A]
20	$\overline{\text{RD}}$	45	$\overline{\text{EMS}}$	70	D11	95	$\overline{\text{BGH}}$
21	$\overline{\text{BMS}}$	46	EE	71	GND	96	PWDACK
22	$\overline{\text{DMS}}$	47	ECLK	72	D12	97	A0
23	$\overline{\text{PMS}}$	48	ELOUT	73	D13	98	A1/IAD0
24	$\overline{\text{IOMS}}$	49	ELIN	74	D14	99	A2/IAD1
25	$\overline{\text{CMS}}$	50	$\overline{\text{EINT}}$	75	D15	100	A3/IAD2

¹ Mode D function available on ADSP-2187L only.

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

BGA PACKAGE PINOUT

The BGA package pinout is shown in Table 30. Pin names in bold text in the table replace the plain text named functions when Mode C equals 1. A plus sign (+) separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets are state bits latched from the value

of the pin at the deassertion of $\overline{\text{RESET}}$. The multiplexed pins DT1/FO, TFS1/ $\overline{\text{IRQ1}}$, RFS1/ $\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

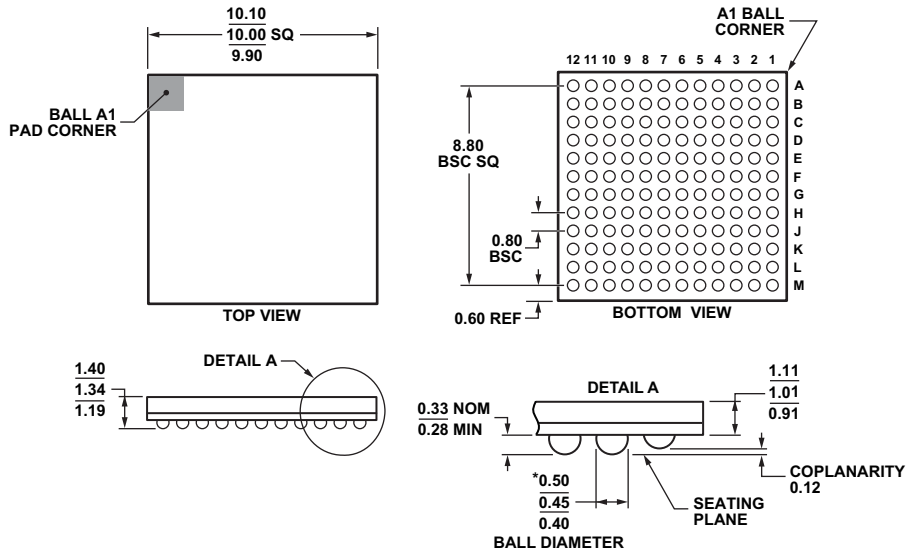
Table 30. BGA Pin Assignments

Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name	Ball No.	Ball Name
A01	A2/ IAD1	D01	NC	G01	XTAL	K01	NC
A02	A1/ IAD0	D02	$\overline{\text{WR}}$	G02	NC	K02	NC
A03	GND	D03	NC	G03	GND	K03	NC
A04	A0	D04	$\overline{\text{BGH}}$	G04	A10/ IAD9	K04	$\overline{\text{BMS}}$
A05	NC	D05	A9/ IAD8	G05	NC	K05	$\overline{\text{DMS}}$
A06	GND	D06	PF1 [MODE B]	G06	NC	K06	RFS0
A07	NC	D07	PF2 [MODE C]	G07	NC	K07	TFS1/ $\overline{\text{IRQ1}}$
A08	NC	D08	NC	G08	D6/ $\overline{\text{IRD}}$	K08	SCLK1
A09	NC	D09	D13	G09	D5/ IAL	K09	$\overline{\text{ERESET}}$
A10	D22	D10	D12	G10	NC	K10	$\overline{\text{EBR}}$
A11	GND	D11	NC	G11	NC	K11	$\overline{\text{BR}}$
A12	GND	D12	GND	G12	D4/ $\overline{\text{IS}}$	K12	$\overline{\text{EBG}}$
B01	A4/ IAD3	E01	V _{DDEXT}	H01	CLKIN	L01	$\overline{\text{IRQE}}$ + PF4
B02	A3/ IAD2	E02	V _{DDEXT}	H02	GND	L02	NC
B03	GND	E03	A8/ IAD7	H03	GND	L03	$\overline{\text{IRQL1}}$ + PF6
B04	NC	E04	FL0	H04	GND	L04	$\overline{\text{IOMS}}$
B05	NC	E05	PF0 [MODE A]	H05	V _{DDINT}	L05	GND
B06	GND	E06	FL2	H06	DT0	L06	$\overline{\text{PMS}}$
B07	V _{DDEXT}	E07	PF3 [MODE D ¹]	H07	TFS0	L07	DR0
B08	D23	E08	GND	H08	D2/ IAD15	L08	GND
B09	D20	E09	GND	H09	D3/ $\overline{\text{IACK}}$	L09	$\overline{\text{RESET}}$
B10	D18	E10	V _{DDEXT}	H10	GND	L10	ELIN
B11	D17	E11	GND	H11	NC	L11	ELOUT
B12	D16	E12	D10	H12	GND	L12	$\overline{\text{EINT}}$
C01	PWDACK	F01	A13/ IAD12	J01	CLKOUT	M01	$\overline{\text{IRQL0}}$ + PF5
C02	A6/ IAD5	F02	NC	J02	V _{DDINT}	M02	$\overline{\text{IRQL2}}$ + PF7
C03	$\overline{\text{RD}}$	F03	A12/ IAD11	J03	NC	M03	NC
C04	A5/ IAD4	F04	A11/ IAD10	J04	V _{DDEXT}	M04	$\overline{\text{CMS}}$
C05	A7/ IAD6	F05	FL1	J05	V _{DDEXT}	M05	GND
C06	$\overline{\text{PWD}}$	F06	NC	J06	SCLK0	M06	DT1/FO
C07	V _{DDEXT}	F07	NC	J07	D0/ IAD13	M07	DR1/FI
C08	D21	F08	D7/ $\overline{\text{IWR}}$	J08	RFS1/ $\overline{\text{IRQ0}}$	M08	GND
C09	D19	F09	D11	J09	$\overline{\text{BG}}$	M09	NC
C10	D15	F10	D8	J10	D1/ IAD14	M10	$\overline{\text{EMS}}$
C11	NC	F11	NC	J11	V _{DDINT}	M11	EE
C12	D14	F12	D9	J12	V _{DDINT}	M12	ECLK

¹ Mode D function available on ADSP-2187L only.

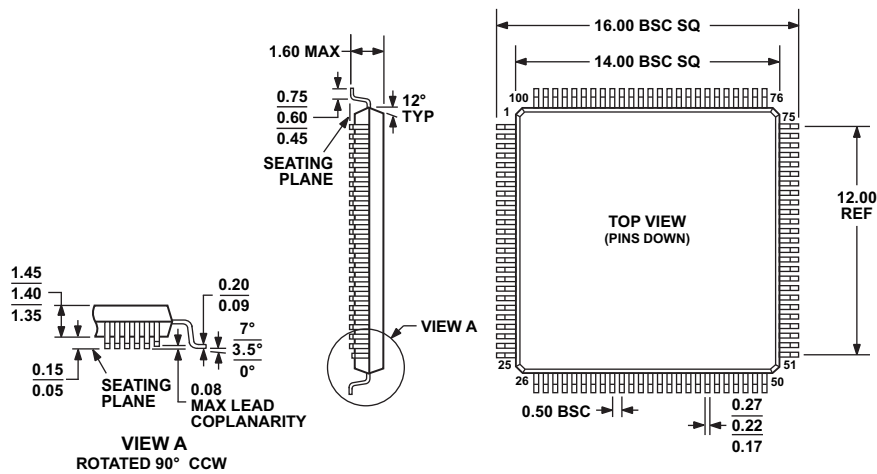
ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-205-AC
WITH THE EXCEPTION TO BALL DIAMETER.

Figure 47. 144-Ball BGA [CSP_BGA] (BC-144-6)



COMPLIANT TO JEDEC STANDARDS MS-026-BED
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 OF ITS IDEAL
POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

Figure 48. 100-Lead Low Profile Quad Flat Package [LQFP] (ST-100-1)

ADSP-2184L/ADSP-2185L/ADSP-2186L/ADSP-2187L

SURFACE MOUNT DESIGN

Table 31 is provided as an aid to PCB design to accommodate BGA style surface mount packages. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 31. BGA Data for Use with Surface Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
144-Ball BGA (BC-144-6)	Solder Mask Defined	0.40 mm diameter	0.50 mm diameter

ORDERING GUIDE

Model	Temperature Range ¹	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2184LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2184LBSTZ-160 ²	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LKST-115	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2185LKST-133	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LKST-160	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LKST-210	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LKSTZ-210 ²	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LBST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2185LBST-133	–40°C to +85°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-133 ²	–40°C to +85°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2185LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-160 ²	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2185LBST-210	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2185LBSTZ-210 ²	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2186LKST-115	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LKST-115R ³	0°C to 70°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LKST-133	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2186LKSTZ-133 ²	0°C to 70°C	32.2	100-Lead LQFP	ST-100-1
ADSP-2186LBST-115	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LBSTZ-115 ²	–40°C to +85°C	28.8	100-Lead LQFP	ST-100-1
ADSP-2186LBST-160 ²	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2186LBCA-160R ³	–40°C to +85°C	40	144-Ball BGA	BC-144-6
ADSP-2187LKST-160	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LKSTZ-160 ²	0°C to 70°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LKST-210	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LKSTZ-210 ²	0°C to 70°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LBST-160	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LBSTZ-160 ²	–40°C to +85°C	40	100-Lead LQFP	ST-100-1
ADSP-2187LBST-210	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1
ADSP-2187LBSTZ-210 ²	–40°C to +85°C	52.5	100-Lead LQFP	ST-100-1

¹ Ranges shown represent ambient temperature.

² Z = RoHS Compliant Part.

³ R = Tape and Reel.

