

74CBTLVD3244

8-bit level-shifting bus switch with 4-bit output enables

Rev. 2 — 16 December 2011

Product data sheet

1. General description

The 74CBTLVD3244 is a dual 4-pole, single-throw bus switch. The device features two output enable inputs ($\overline{nOE}$) that each control four switch channels. The switches are disabled when the associated $\overline{nOE}$ input is HIGH. Schmitt trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 3.0 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3244DS	–40 °C to +125 °C	SSOP20 [1]	plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT724-1
74CBTLVD3244PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74CBTLVD3244BQ	–40 °C to +125 °C	DHVQFN20	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

[1] Also known as QSOP20 package

4. Functional diagram

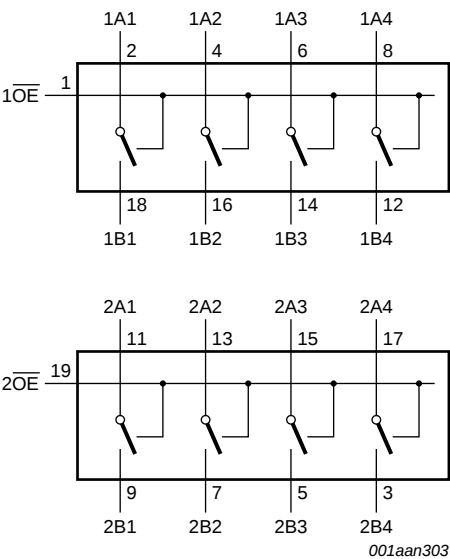


Fig 1. Logic symbol

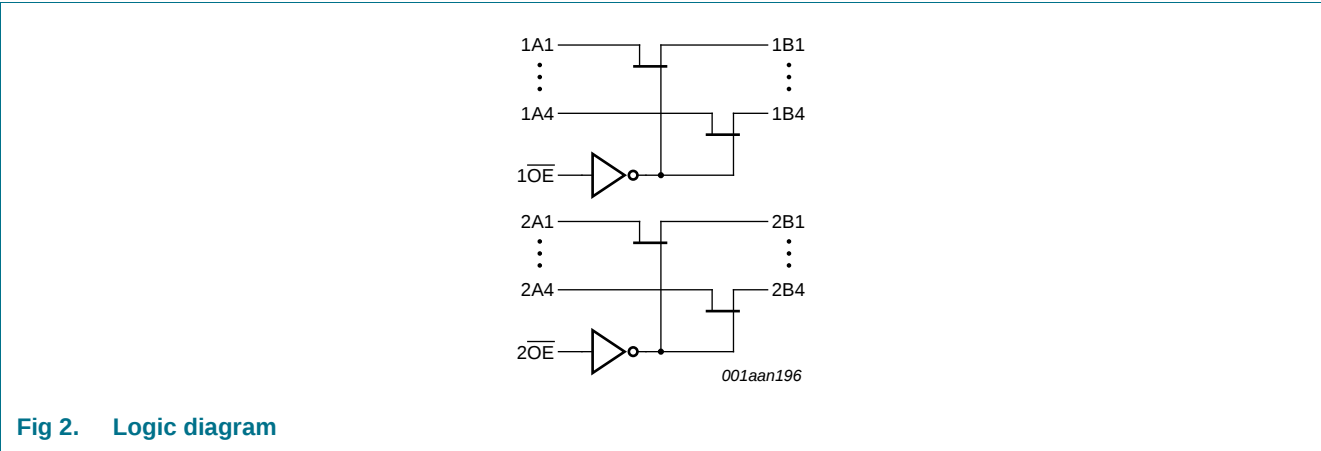


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning

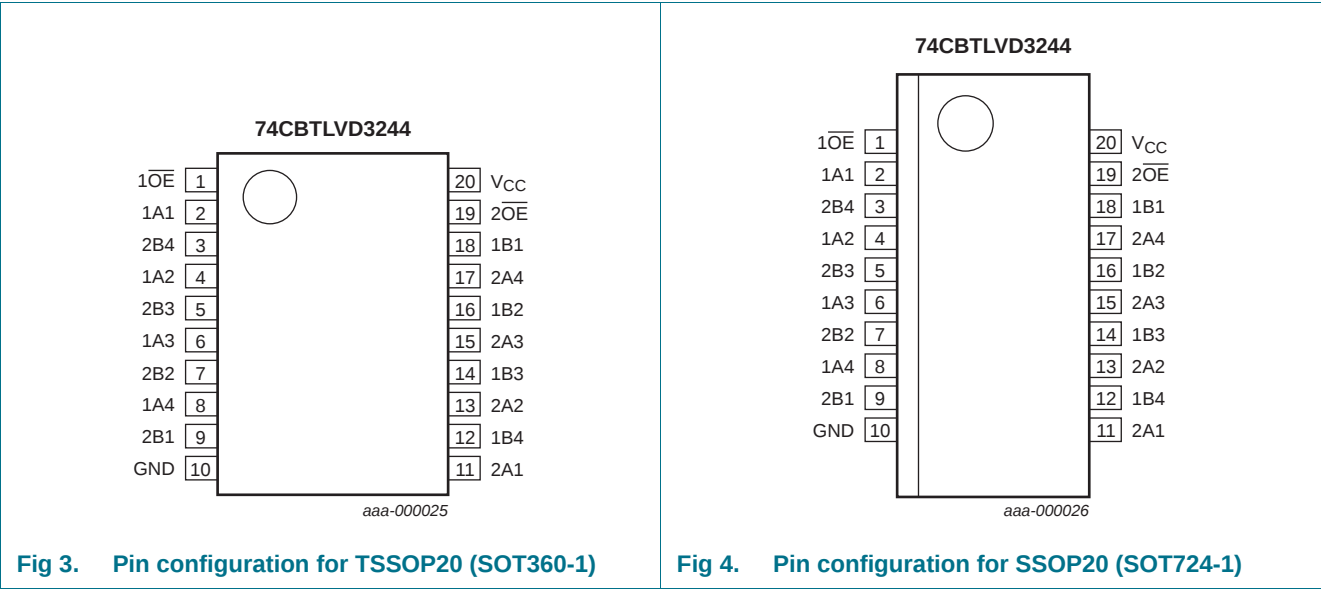
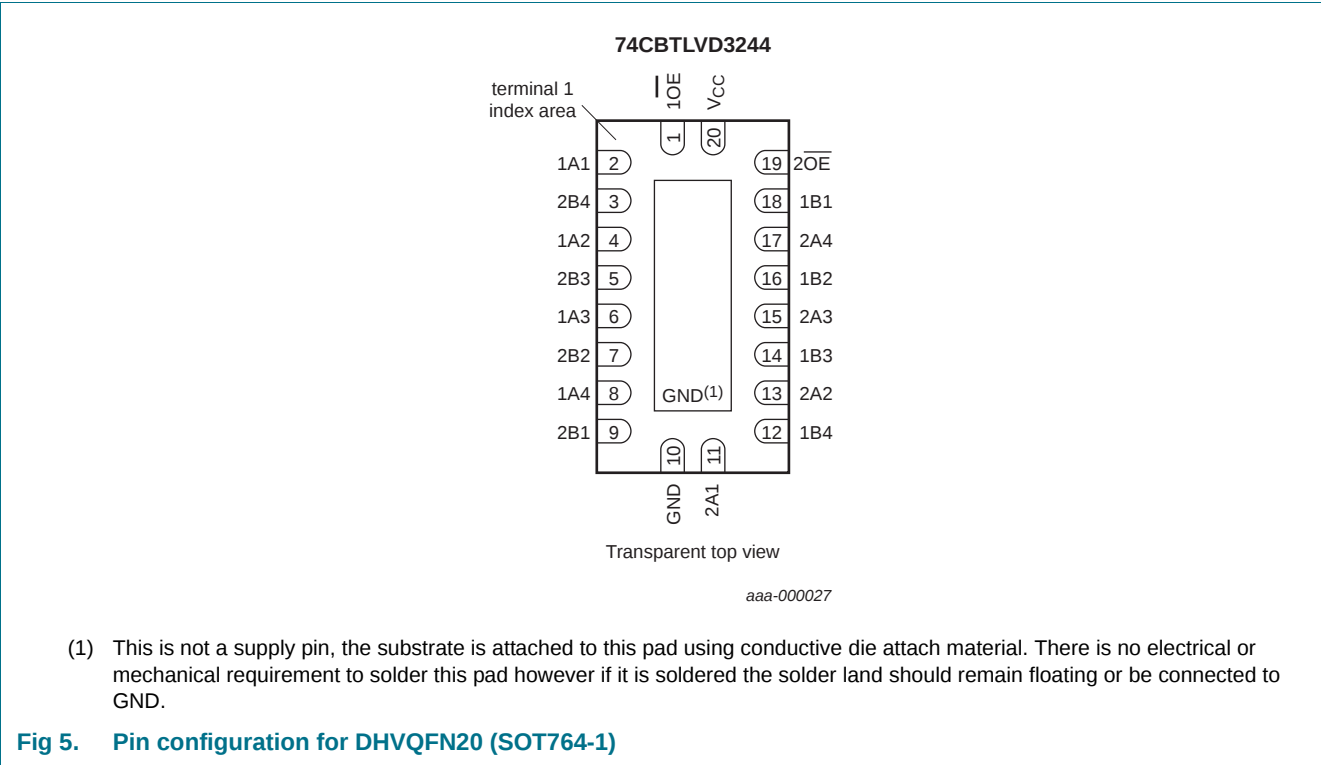


Fig 3. Pin configuration for TSSOP20 (SOT360-1)

Fig 4. Pin configuration for SSOP20 (SOT724-1)



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{1OE}$, $\overline{2OE}$	1, 19	output enable input (active LOW)
1A1 to 1A4	2, 4, 6, 8	data input/output (A port)
2B1 to 2B4	9, 7, 5, 3	data input/output (A port)
GND	10	ground (0 V)
2A1 to 2A4	11, 13, 15, 17	data input/output (B port)
1B1 to 1B4	18, 16, 14, 12	data input/output (B port)
V _{CC}	20	positive supply voltage

6. Functional description

Table 3. Function selection^[1]

Input	Input/output
$\overline{nOE}$	nAn, nBn
L	nAn = nBn
H	Z

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage		^[1] -0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode	^[1] -0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_{IO} < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current	$V_{SW} = 0$ V to V_{CC}	-	±128	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[2] -	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN20 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		3.0	3.6	V
V_I	input voltage		0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0$ V to 3.6 V	^[1] 0	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	$T_{amb} = -40$ °C to +85 °C			$T_{amb} = -40$ °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 3.0$ V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 3.0$ V to 3.6 V	-	-	0.9	-	0.9	V
I_I	input leakage current	pin $\overline{nOE}$; $V_I = GND$ to V_{CC} ; $V_{CC} = 3.6$ V	-	-	±1	-	±20	μA
V_{pass}	pass voltage	$V_I = V_{CC}$; see Figure 8 to Figure 12	-	-	-	-	-	V

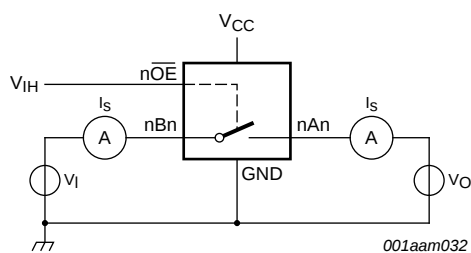
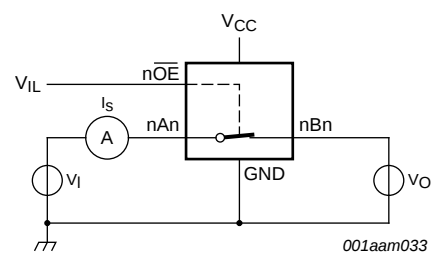
Table 6. Static characteristics ...continued

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Figure 6	-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Figure 7	-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	μA
I _{CC}	supply current	V _I = V _{CC} ; I _O = 0 A; V _{CC} = 3.6 V; V _{SW} = GND or V _{CC}	-	-	20	-	50	μA
		V _I = GND; I _O = 0 A; V _{CC} = 3.6 V; V _{SW} = GND or V _{CC}	-	-	100	-	150	μA
ΔI _{CC}	additional supply current	pin n $\overline{\text{OE}}$; V _I = V _{CC} – 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	[2]	-	300	-	2000	μA
C _I	input capacitance	pin n $\overline{\text{OE}}$; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	2.5	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	9.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1 Test circuits

V_I = V_{CC} or GND and V_O = GND or V_{CC}.**Fig 6.** Test circuit for measuring OFF-state leakage current (one switch)V_I = V_{CC} or GND and V_O = open circuit.**Fig 7.** Test circuit for measuring ON-state leakage current (one switch)

9.2 Typical pass voltage graphs

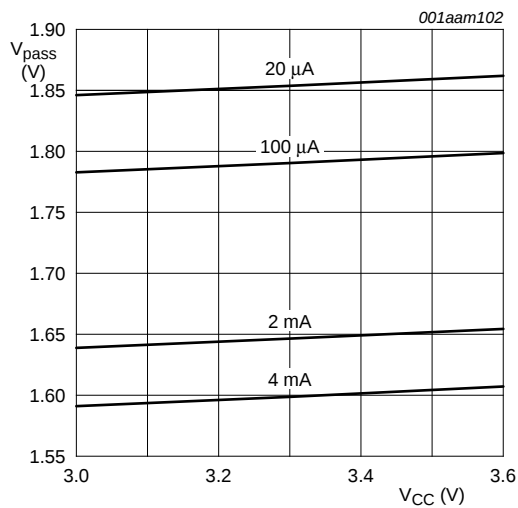


Fig 8. Pass voltage versus supply voltage;
T_{amb} = 125 °C (typical)

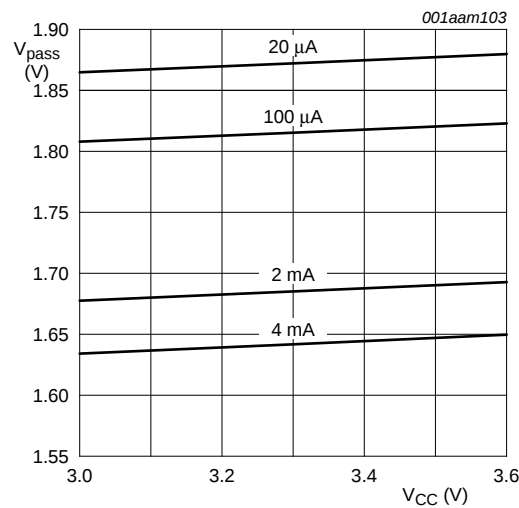


Fig 9. Pass voltage versus supply voltage;
T_{amb} = 85 °C (typical)

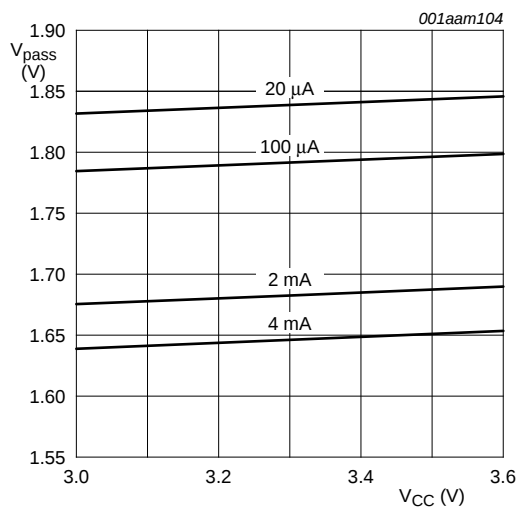


Fig 10. Pass voltage versus supply voltage;
T_{amb} = 25 °C (typical)

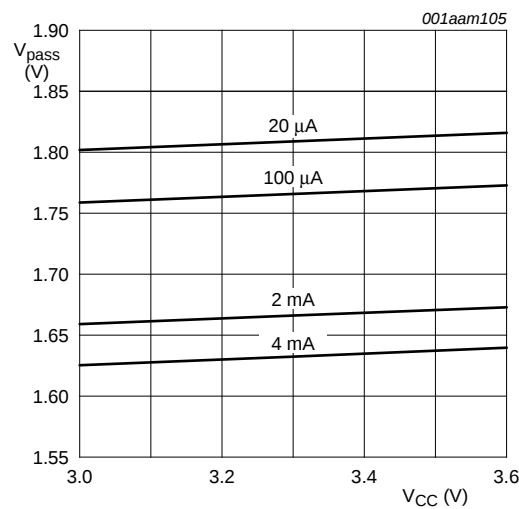


Fig 11. Pass voltage versus supply voltage;
T_{amb} = 0 °C (typical)

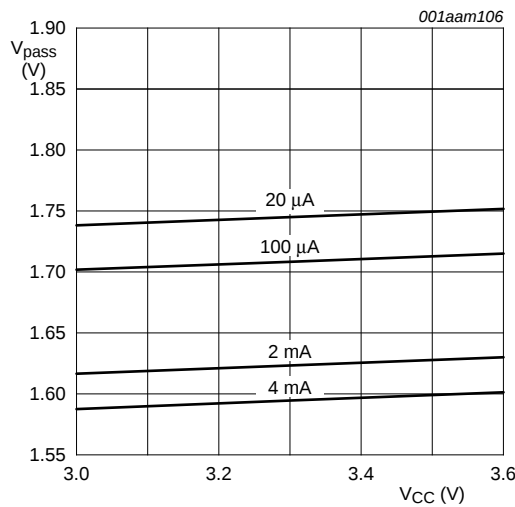


Fig 12. Pass voltage versus supply voltage; T_{amb} = -40 °C (typical)

9.3 ON resistance

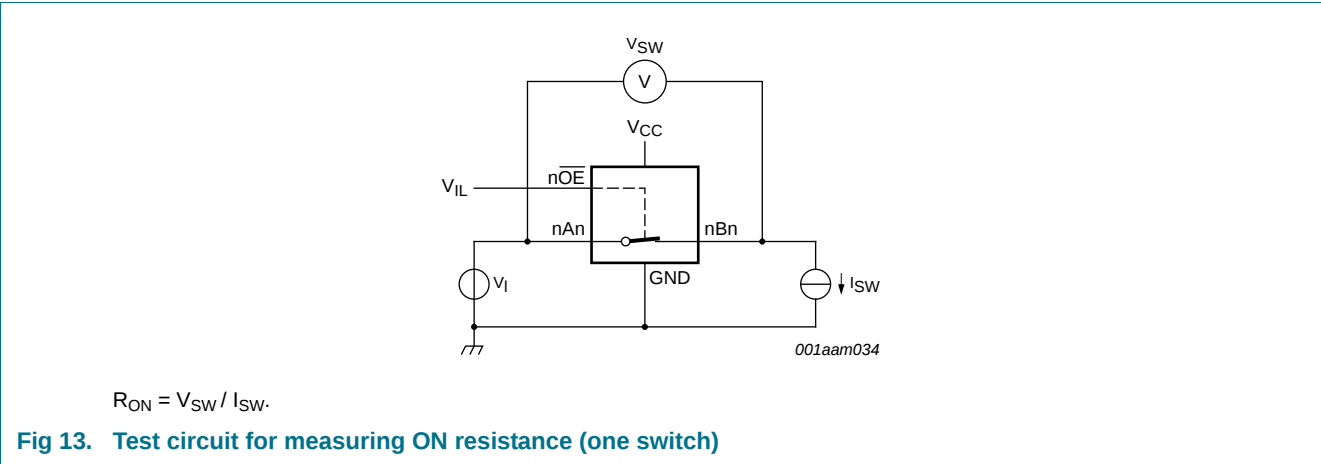
Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 13](#).

Symbol	Parameter	Conditions	T _{amb} = −40 °C to +85 °C			T _{amb} = −40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
R _{ON}	ON resistance	V _{CC} = 3.0 V to 3.6 V						
		I _{SW} = 64 mA; V _I = 0 V	-	3.7	7.0	-	10.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	3.7	7.0	-	10.0	Ω
		I _{SW} = 15 mA; V _I = 1.2 V	-	4.7	10.0	-	12.0	Ω

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.4 ON resistance test circuit



10. Dynamic characteristics

Table 8. Dynamic characteristics
GND = 0 V; for test circuit see [Figure 16](#)

Symbol	Parameter	Conditions	T _{amb} = –40 °C to +85 °C			T _{amb} = –40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nBn or nBn to nAn; see Figure 14 V _{CC} = 3.0 V to 3.6 V	-	-	0.11	-	0.22	ns
t _{en}	enable time	nOE to nAn or nBn; see Figure 15 V _{CC} = 3.0 V to 3.6 V	1.5	2.8	5.0	1.5	6.0	ns
t _{dis}	disable time	nOE to nAn or nBn; see Figure 15 V _{CC} = 3.0 V to 3.6 V	0.8	3.1	7.0	0.8	8.0	ns

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
- [2] The propagation delay is the calculated RC time constant of the on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

11. Waveforms

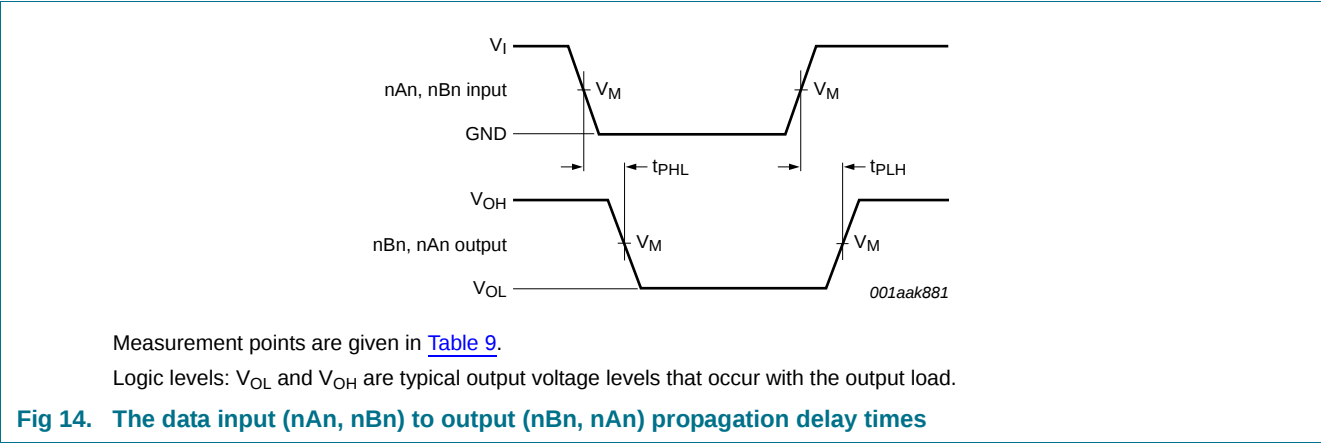
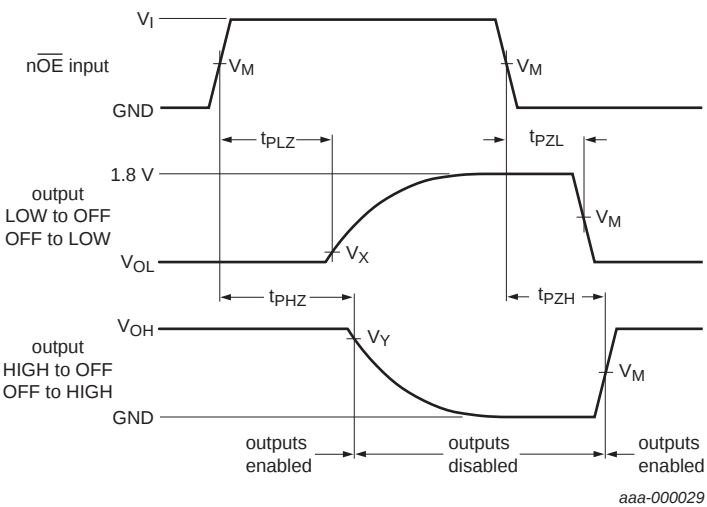


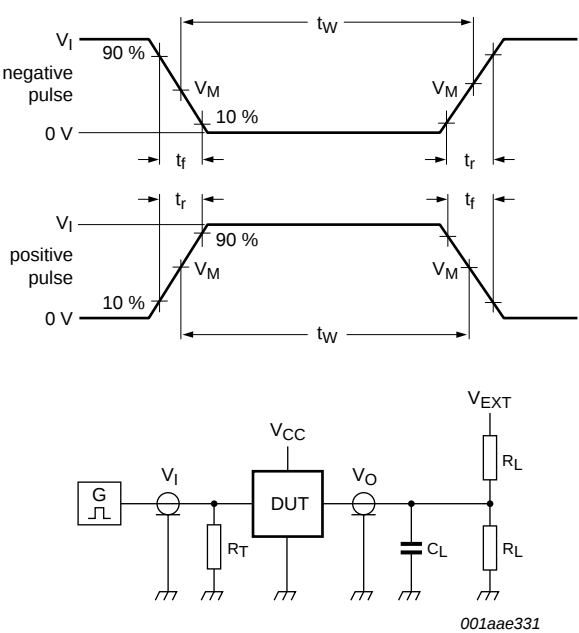
Table 9. Measurement points

Supply voltage	Input			Output		
V _{CC}	V _M	V _I	t _r = t _f	V _M	V _X	V _Y
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.9 V	V _{OL} + 0.15 V	V _{OH} – 0.15 V



Measurement points are given in [Table 9](#).
Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 15. Enable and disable times



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V to 3.6 V	30 pF	1 kΩ	open	GND	3.6 V

11.1 Additional dynamic characteristics

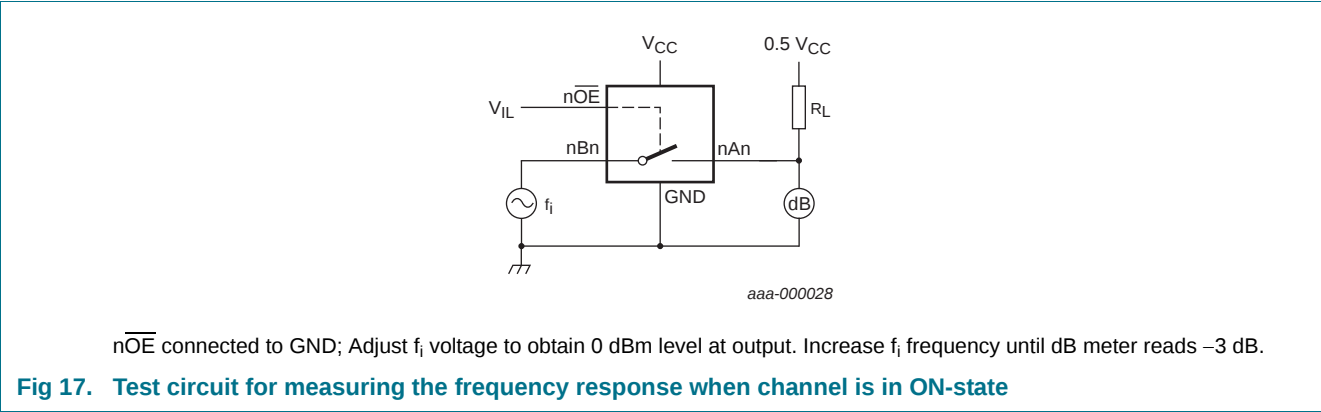
Table 11. Additional dynamic characteristics
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
f _(-3dB)	-3 dB frequency response	V _{CC} = 3.3 V; R _L = 50 Ω; see Figure 17 ^[2]	-	575	-	MHz

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.

[2] f_i is biased at 0.5V_{CC}.

11.2 Test circuits



12. Package outline

SSOP20: plastic shrink small outline package; 20 leads; body width 3.9 mm; lead pitch 0.635 mm SOT724-1

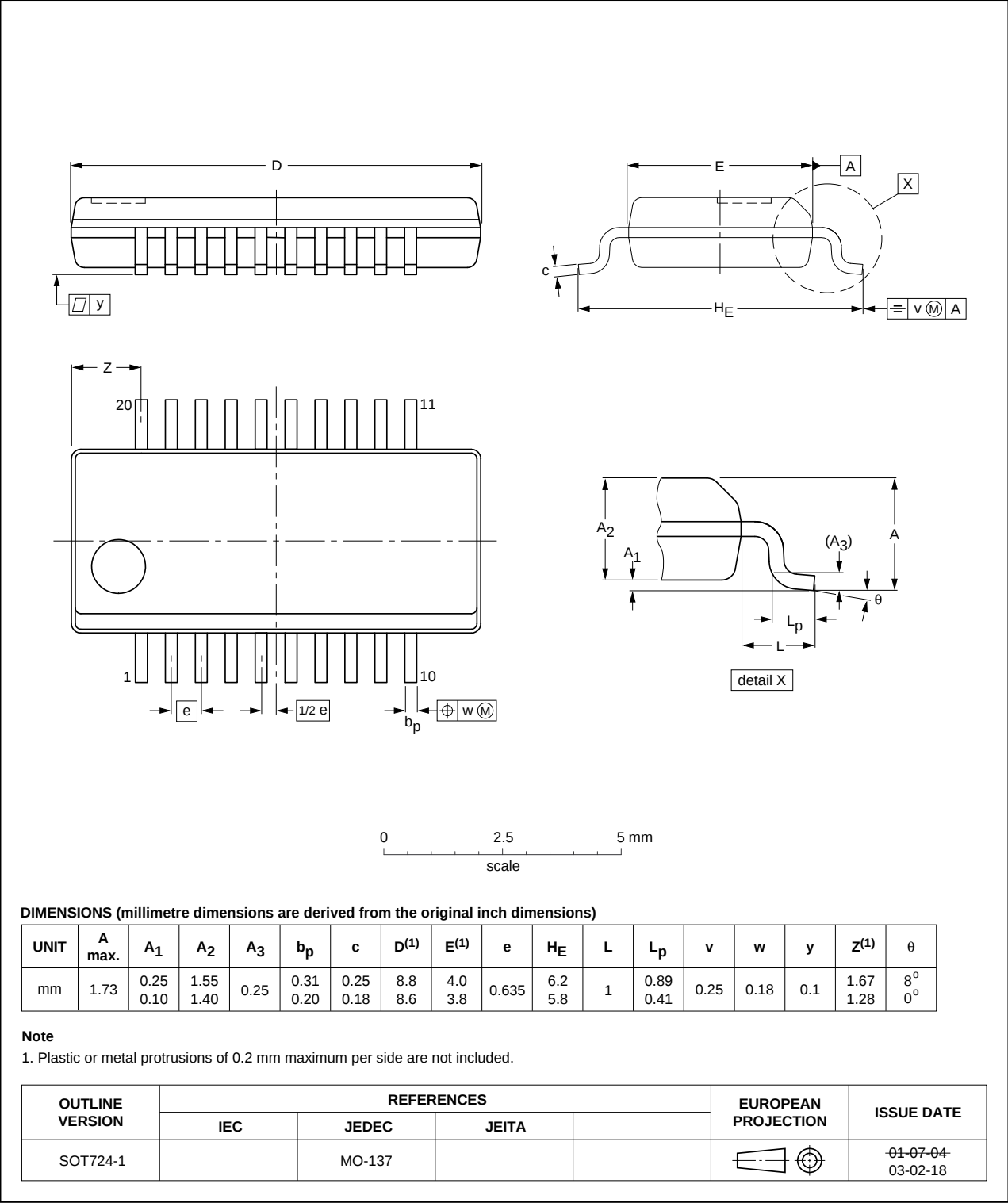


Fig 18. Package outline SOT724-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

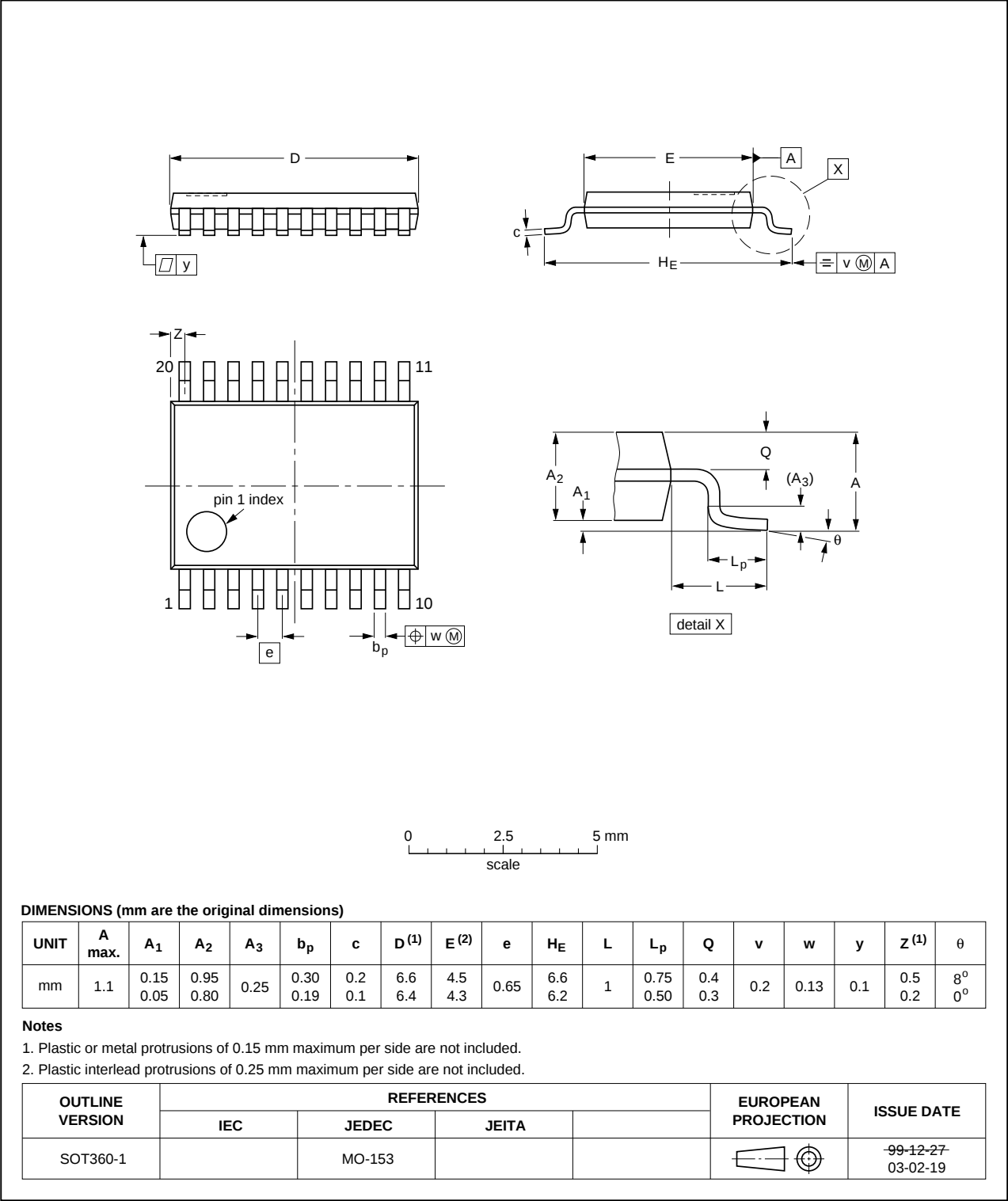


Fig 19. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm SOT764-1

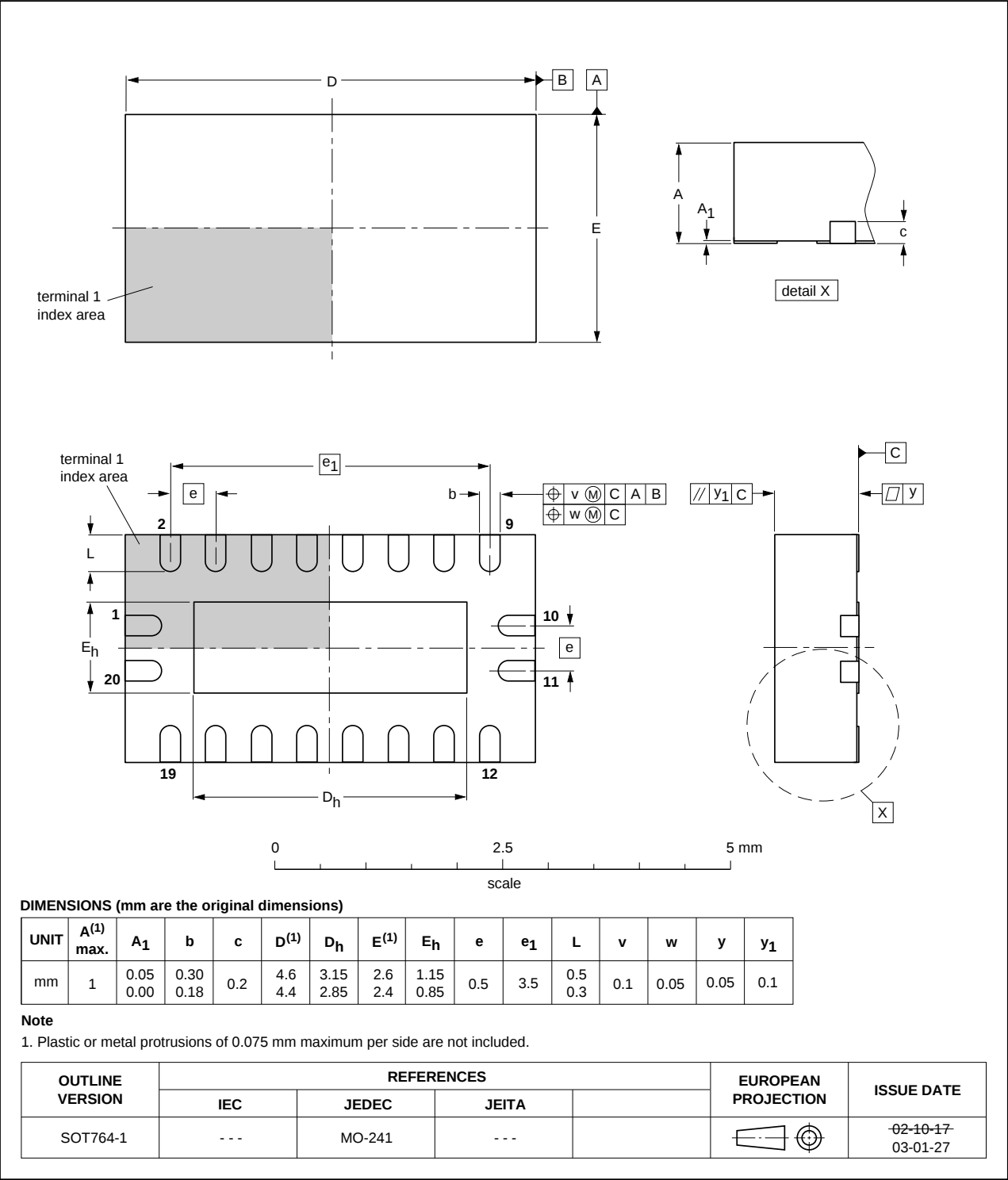


Fig 20. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3244 v.2	20111216	Product data sheet	-	74CBTLVD3244 v.1
Modifications:	• Legal pages updated.			
74CBTLVD3244 v.1	20110715	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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