

# TFA9842AJ

## 7.5 W stereo power amplifier with volume control

Rev. 01 — 28 April 2006

Preliminary specification

### 1. General description

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The TFA9842AJ contains two identical audio power amplifiers. The TFA9842AJ can be used as two Single-Ended (SE) channels with a volume control. The maximum gain is 26 dB.

The TFA9842AJ comes in a 9-pin DIL-bent-SIL (DBS9P) power package. The TFA9842AJ is pin compatible with the TFA9843AJ, TFA9843(B)J, TFA9842(B)J and TFA9841J. The difference between the TFA9843AJ and the TFA9843(B)J, TFA9842(B)J, TFA9841J is the functionality of pin 7. The TFA9843AJ has a Volume Control (VC) on pin 7. The TFA9843(B)J, TFA9842(B)J and TFA9841J have a mode select (MODE) on pin 7.

The TFA9842AJ contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heatsink and ambient temperature) allow it.

### 2. Features

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- 2 channel SE: 1 W to 7.5 W operation possibility
- Soft clipping
- Input clamps
- Volume control
- Standby and Mute mode
- No on or off switching plops
- Low standby current
- High supply voltage ripple rejection
- Outputs short-circuit protected to ground, supply and across the load
- Thermally protected
- Pin compatible with the TFA9843AJ, TFA9843(B)J, TFA9842(B)J and TFA9841J

### 3. Applications

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- CRT TV and LCD TV
- Monitors
- PC speakers
- Boom box
- Mini and micro audio receivers

# PHILIPS

## 4. Quick reference data

Table 1. Quick reference data

| Symbol        | Parameter                       | Conditions                                                  | Min   | Typ | Max | Unit          |
|---------------|---------------------------------|-------------------------------------------------------------|-------|-----|-----|---------------|
| $V_{CC}$      | supply voltage                  | operating                                                   | [1] 9 | 17  | 28  | V             |
| $I_q$         | quiescent current               | $V_{CC} = 17\text{ V};$<br>$R_L = \infty\ \Omega$           | -     | 60  | 100 | mA            |
| $I_{CC(stb)}$ | standby supply current          | $V_{CC} = 17\text{ V};$<br>$V_{I(VC)} < 0.8\text{ V}$       | -     | -   | 150 | $\mu\text{A}$ |
| $P_o$         | output power                    | THD = 10 %;<br>$R_L = 4\ \Omega;$<br>$V_{CC} = 17\text{ V}$ | 7     | 7.5 | -   | W             |
| THD           | total harmonic distortion       | $P_o = 1\text{ W}$                                          | -     | 0.1 | 0.5 | %             |
| $G_{V(max)}$  | maximum voltage gain            | $V_{I(VC)} > 5.0\text{ V}$                                  | 25    | 26  | 27  | dB            |
| $\Delta G_V$  | voltage gain range              | $1.5\text{ V} < V_{I(VC)} < 5.0\text{ V}$                   | -     | 80  | -   | dB            |
| SVRR          | supply voltage ripple rejection | $f_{ripple} = 1\text{ kHz}$                                 | [2] - | 60  | -   | dB            |

[1] A minimum load of 3  $\Omega$  is allowed at supply voltages > 22 V.

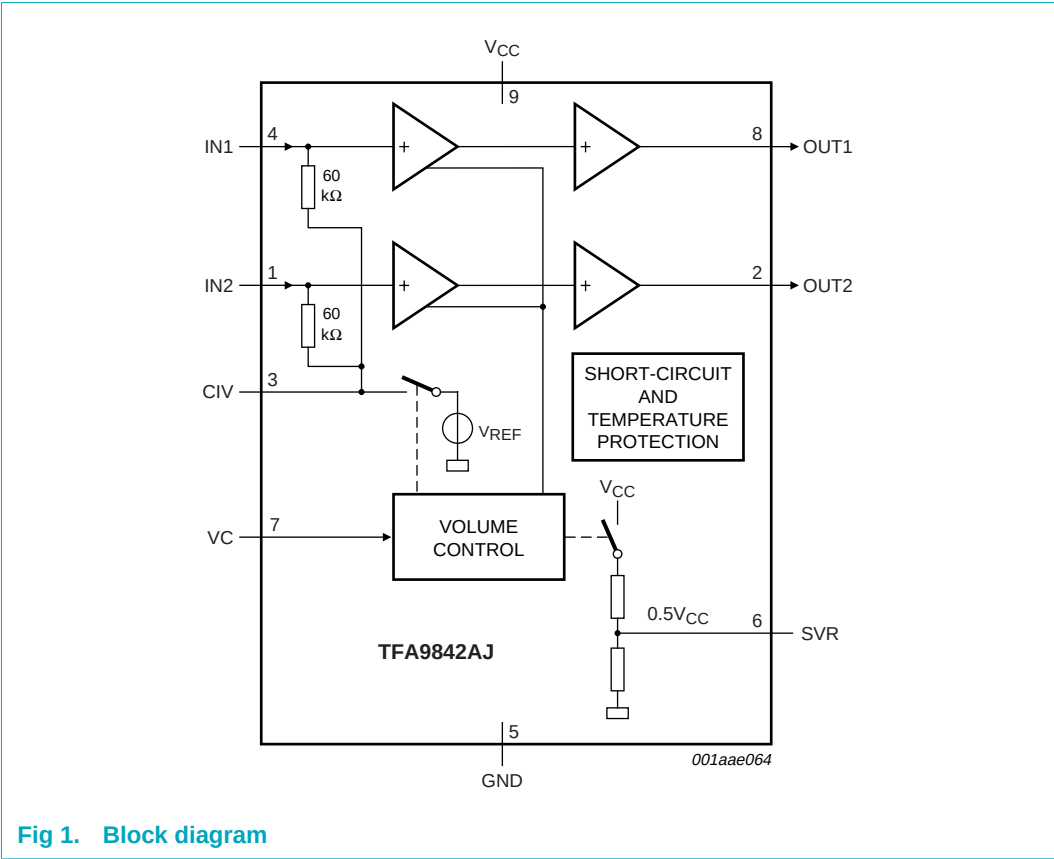
[2] Supply voltage ripple rejection is measured at the output, with a source impedance  $Z_S = 0\ \Omega$  at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency  $f_{ripple}$  and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

## 5. Ordering information

Table 2. Ordering information

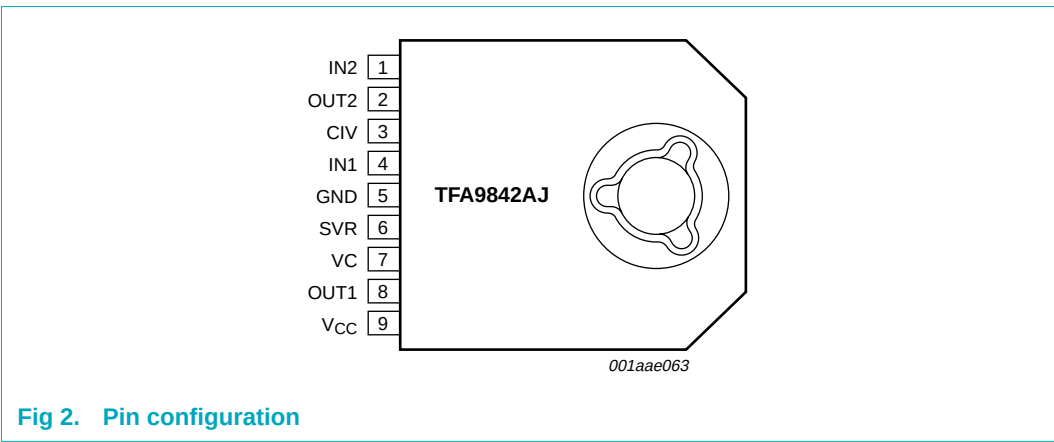
| Type number | Package |                                                                                     |           |
|-------------|---------|-------------------------------------------------------------------------------------|-----------|
|             | Name    | Description                                                                         | Version   |
| TFA9842AJ   | DBS9P   | plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad | SOT523 -1 |

6. Block diagram



7. Pinning information

7.1 Pinning



## 7.2 Pin description

Table 3. Pin description

| Symbol          | Pin | Description                                             |
|-----------------|-----|---------------------------------------------------------|
| IN2             | 1   | input 2                                                 |
| OUT2            | 2   | loudspeaker terminal 2                                  |
| CIV             | 3   | common input voltage decoupling                         |
| IN1             | 4   | input 1                                                 |
| GND             | 5   | ground                                                  |
| SVR             | 6   | half supply voltage decoupling (ripple rejection)       |
| VC              | 7   | volume control input (standby, mute and volume control) |
| OUT1            | 8   | loudspeaker terminal 1                                  |
| V <sub>CC</sub> | 9   | supply voltage                                          |

## 8. Functional description

### 8.1 Input configuration

The input cut-off frequency is:

$$f_{i(-3dB)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

Single-ended application:  $R_i = 60 \text{ k}\Omega$  and  $C_i = 220 \text{ nF}$ :

$$f_{i(-3dB)} = \frac{1}{2\pi(60 \times 10^3 \times 220 \times 10^{-9})} = 12 \text{ Hz} \quad (2)$$

As shown in [Equation 2](#), large capacitor values for the inputs are not necessary; therefore switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

The TFA9842AJ has clamps on the inputs. In Standby mode the voltage on the input pins is clamped for voltages lower than  $-0.1 \text{ V}$ . When the TFA9842AJ is in Mute, Volume control or Operating mode (maximum gain) the input clamp voltage is  $1 \text{ V (RMS)}$ .

### 8.2 Power amplifier

The power amplifier is a single-ended amplifier with an all NPN output stage, capable of delivering a peak output current of  $3 \text{ A}$ .

#### 8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10 %; see [Figure 7](#). The maximum output power is limited by the supply voltage of  $26 \text{ V}$  and the maximum available output current is  $3 \text{ A}$  repetitive peak current. A minimum load of  $3 \text{ }\Omega$  is required for supply voltages  $> 22 \text{ V}$ ; see [Figure 4](#). The output power is measured with one channel driven.

### 8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom, compared to the average power output, for transferring the loudest parts without distortion. At  $V_{CC} = 17\text{ V}$  and  $P_o = 5\text{ W}$  (SE with  $R_L = 4\ \Omega$ ) at  $\text{THD} < 0.5\%$  (see [Figure 5](#)), the Average Listening Level (ALL) music power without any distortion yields:

$$P_{o(ALL)} = \frac{5}{15.85} = 315\text{ mW} \quad (3)$$

The power dissipation can be derived from [Figure 8](#) (SE) for 0 dB respectively 12 dB headroom (see [Table 4](#)).

For the average listening level a power dissipation of 4.2 W can be used for a heatsink calculation.

**Table 4. Power rating as function of headroom**

| Headroom | Power output SE<br>(THD < 0.5 %) | Power dissipation (P);<br>both channels driven |
|----------|----------------------------------|------------------------------------------------|
| 0 dB     | $P_o = 5\text{ W}$               | 8.4 W                                          |
| 12 dB    | $P_{o(ALL)} = 315\text{ mW}$     | 4.2 W                                          |

### 8.3 Mode selection

The TFA9842AJ has four functional modes, which can be selected by applying the proper DC voltage to pin VC (see [Table 5](#)).

**Table 5. Mode selection**

| $V_{I(VC)}$       | Status            | Definition                                                                                                                                                                                                                             |
|-------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 V to 0.8 V      | Standby           | in this mode the current consumption is very low and the outputs are floating; the device is in Standby mode when $V_{I(VC)} < 0.8\text{ V}$ .                                                                                         |
| 1.2 V to 1.5 V    | Mute              | in this mode the amplifier is DC-biased but not operational (no audio output); this allows the input coupling capacitors to be charged to avoid pop-noise; the device is in Mute mode when $1.2\text{ V} < V_{I(VC)} < 1.5\text{ V}$ . |
| 1.5 V to 5.0 V    | Volume control    | in this mode the volume of the amplifier can be controlled; the gain can be adjusted between the range of $1.5\text{ V} < V_{I(VC)} < 5.0\text{ V}$ .                                                                                  |
| 5.0 V to $V_{CC}$ | On (maximum gain) | in this mode the amplifier has its maximum gain; the Operating mode is activated at $V_{I(VC)} > 5.0\text{ V}$ .                                                                                                                       |

### 8.4 Supply voltage ripple rejection

The supply voltage ripple rejection (SVRR) is measured with an electrolytic capacitor of 150  $\mu\text{F}$  connected to pin SVR with a bandwidth of 20 Hz to 22 kHz. The SVRR as a function of the frequency is illustrated in [Figure 10](#). A larger capacitor value on pin SVR improves the ripple rejection behavior at the lower frequencies.

### 8.5 Built-in protection circuits

The TFA9842AJ contains two types of temperature sensors; one measures the local temperatures of the power stages and one measures the global chip temperature. At a local temperature of the power stage of approximately 185 °C or a global temperature of approximately 150 °C this detection circuit switches off the power stages for 2 ms. When the outputs are switched off the voltage is measured on the outputs. In the event of a short-circuit to ground or to  $V_{CC}$  the device will remain in Protection mode. In all other cases the power stages switch-on automatically and the detection will take place again; however a too high temperature will switch-off the power stages immediately. This can result in repetitive switching during too high junction temperature. This protects the TFA9842AJ against short-circuits to ground, to the supply voltage, across the load and too high chip temperatures.

The protection will only be activated when necessary, so even during a short-circuit condition, a certain amount of (pulsed) current will still flow through the short-circuit (as much as the power stage can handle without exceeding the critical temperature level).

## 9. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol        | Parameter                               | Conditions    | Min  | Max            | Unit |
|---------------|-----------------------------------------|---------------|------|----------------|------|
| $V_{CC}$      | supply voltage                          | operating     | −0.3 | +28            | V    |
| $V_I$         | input voltage                           |               | −0.3 | $V_{CC} + 0.3$ | V    |
| $I_{ORM}$     | repetitive peak output current          |               | -    | 3              | A    |
| $T_{stg}$     | storage temperature                     | non-operating | −55  | +150           | °C   |
| $T_{amb}$     | ambient temperature                     | operating     | −40  | +85            | °C   |
| $P_{tot}$     | total power dissipation                 |               | -    | 35             | W    |
| $V_{CC(scp)}$ | short-circuit protection supply voltage |               | -    | 26             | V    |

## 10. Thermal characteristics

**Table 7. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions           | Typ | Unit |
|---------------|---------------------------------------------|----------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air          | 40  | K/W  |
| $R_{th(j-c)}$ | thermal resistance from junction to case    | both channels driven | 2.0 | K/W  |

## 11. Static characteristics

**Table 8. Static characteristics**

$V_{CC} = 17\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $R_L = 4\text{ }\Omega$ ;  $V_{I(VC)} = V_{CC}$ ;  $V_i = 0\text{ V}$ ; measured in test circuit of [Figure 11](#); unless otherwise specified.

| Symbol      | Parameter               | Conditions                        | Min   | Typ | Max      | Unit          |
|-------------|-------------------------|-----------------------------------|-------|-----|----------|---------------|
| $V_{CC}$    | supply voltage          | operating                         | [1] 9 | 17  | 28       | V             |
| $I_q$       | quiescent current       | $R_L = \infty\text{ }\Omega$      | -     | 60  | 100      | mA            |
| $I_{stb}$   | standby current         | $V_{I(VC)} = 0\text{ V}$          | -     | -   | 150      | $\mu\text{A}$ |
| $V_O$       | output voltage          |                                   | [2] - | 9   | -        | V             |
| $V_{I(VC)}$ | input voltage on pin VC | On mode (maximum gain)            | 5.0   | -   | $V_{CC}$ | V             |
|             |                         | Volume control mode               | 1.5   | -   | 5.0      | V             |
|             |                         | Mute mode                         | 1.2   | -   | 1.5      | V             |
|             |                         | Standby mode                      | 0     | -   | 0.8      | V             |
| $I_{I(VC)}$ | input current on pin VC | $0\text{ V} < V_{I(VC)} < V_{CC}$ | -     | -   | 20       | $\mu\text{A}$ |

[1] A minimum load of  $3\text{ }\Omega$  is allowed at supply voltages  $> 22\text{ V}$ .

[2] The DC output voltage with respect to ground is approximately  $0.5V_{CC}$ .

## 12. Dynamic characteristics

**Table 9. Dynamic characteristics**

$V_{CC} = 17\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $R_L = 4\text{ }\Omega$ ;  $f = 1\text{ kHz}$ ;  $V_{I(VC)} = V_{CC}$ ; measured in test circuit [Figure 11](#); unless otherwise specified.

| Symbol                | Parameter                       | Conditions                                     | Min   | Typ | Max | Unit          |
|-----------------------|---------------------------------|------------------------------------------------|-------|-----|-----|---------------|
| $P_o$                 | output power                    | THD = 10 %; $R_L = 4\text{ }\Omega$            | 7     | 7.5 | -   | W             |
|                       |                                 | THD = 0.5 %; $R_L = 4\text{ }\Omega$           | -     | 6.1 | -   | W             |
| THD                   | total harmonic distortion       | $P_o = 1\text{ W}$                             | -     | 0.1 | 0.5 | %             |
| $G_{V(max)}$          | maximum voltage gain            | $V_{I(VC)} > 5.0\text{ V}$                     | 25    | 26  | 27  | dB            |
| $\Delta G_V$          | voltage gain range              | $1.5\text{ V} < V_{I(VC)} < 5.0\text{ V}$      | -     | 80  | -   | dB            |
| $V_i$                 | input voltage                   | Gain = 0 dB;<br>THD < 1 %                      | 1.0   | -   | -   | V             |
| $Z_i$                 | input impedance                 |                                                | 40    | 60  | -   | k $\Omega$    |
| $V_{n(o)}$            | noise output voltage            |                                                | [1] - | 150 | -   | $\mu\text{V}$ |
| SVRR                  | supply voltage ripple rejection | $f_{ripple} = 1\text{ kHz}$                    | [2] - | 60  | -   | dB            |
|                       |                                 | $f_{ripple} = 100\text{ Hz to } 20\text{ kHz}$ | [2] - | 60  | -   | dB            |
| $V_{o(mute)}$         | mute output voltage             |                                                | [3] - | -   | 150 | $\mu\text{V}$ |
| $\alpha_{cs}$         | channel separation              | $Z_S = 0\text{ }\Omega$                        | 50    | 60  | -   | dB            |
| $ \Delta G_{V(max)} $ | maximum voltage gain difference |                                                | -     | -   | 1   | dB            |

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance  $Z_S = 0\text{ }\Omega$  at the input.

- [2] Supply voltage ripple rejection is measured at the output, with a source impedance  $Z_S = 0\ \Omega$  at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency  $f_{\text{ripple}}$  and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.
- [3] Output voltage in Mute mode ( $V_{I(VC)} = 1.35\text{ V}$ ) and an input voltage of 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, so including noise.

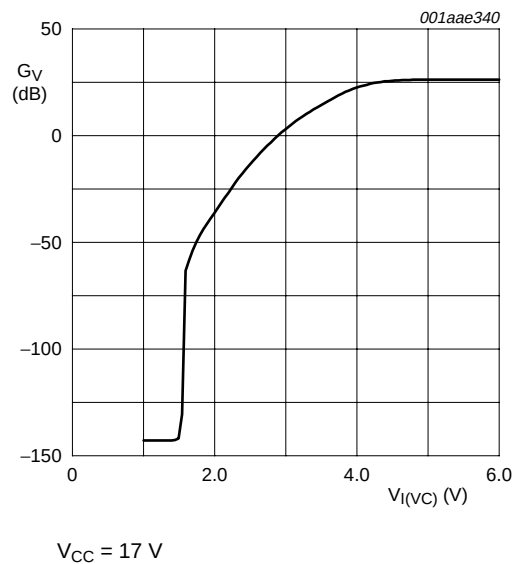


Fig 3. Voltage gain as a function of volume control voltage

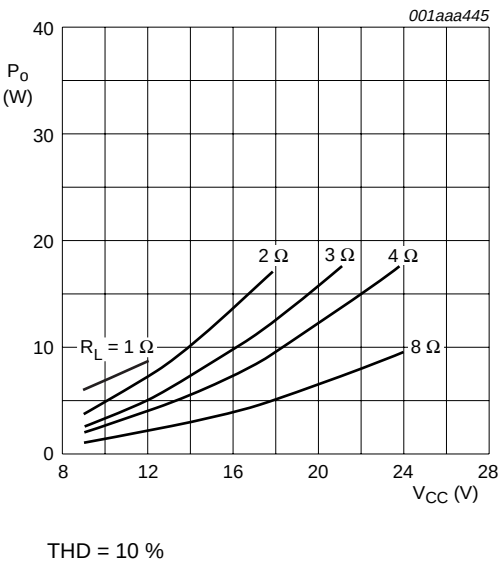


Fig 4. Output power (one channel) as a function of supply voltage for various SE loads

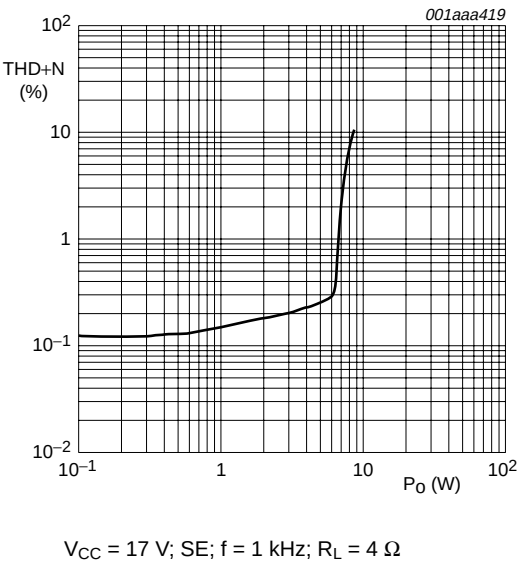


Fig 5. Total harmonic distortion-plus-noise as a function of output power

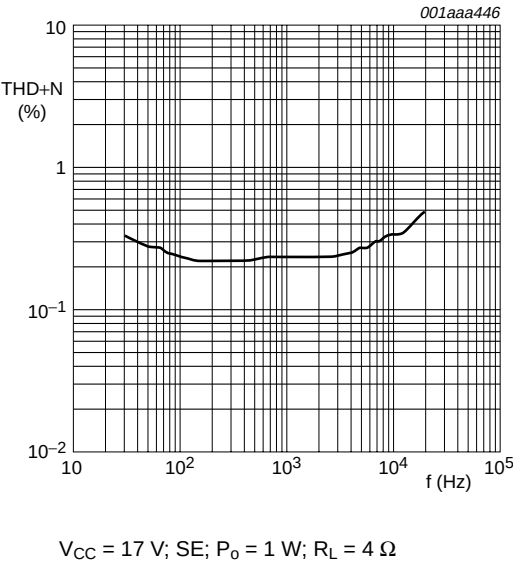
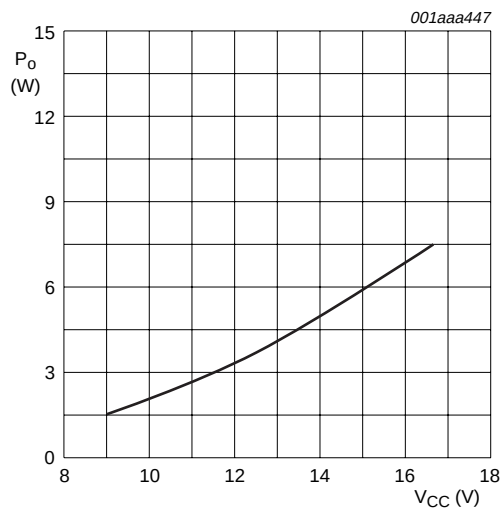


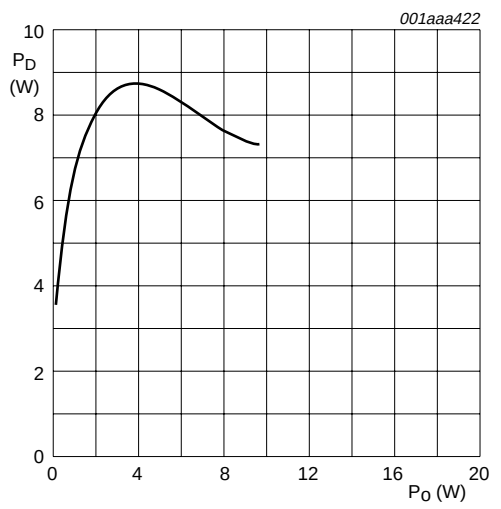
Fig 6. Total harmonic distortion-plus-noise as a function of frequency





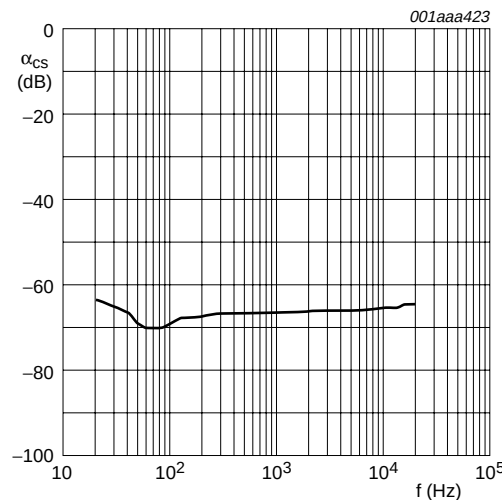
THD = 10 %; SE; R<sub>L</sub> = 4 Ω; f = 1 kHz

Fig 7. Output power as a function of supply voltage



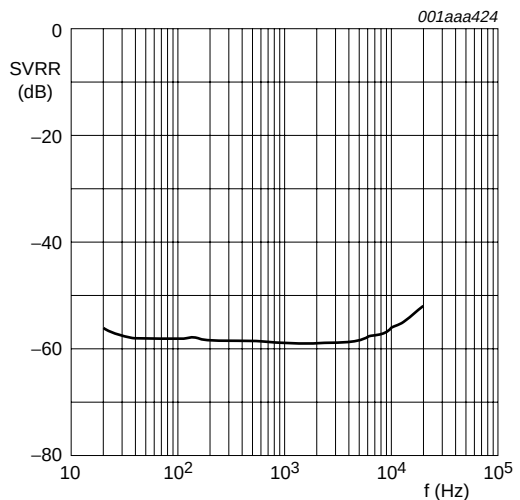
V<sub>CC</sub> = 17 V; SE; R<sub>L</sub> = 4 Ω

Fig 8. Total power dissipation as a function of channel output power per channel (worst case, both channels driven)



V<sub>CC</sub> = 17 V; SE; R<sub>L</sub> = 4 Ω

Fig 9. Channel separation as a function of frequency (no bandpass filter applied)



V<sub>CC</sub> = 17 V; SE; Z<sub>S</sub> = 0 Ω; V<sub>ripple</sub> = 300 mV (RMS); a bandpass filter of 20 Hz to 22 kHz has been applied; inputs short-circuited.

Fig 10. Supply voltage ripple rejection as a function of frequency

## 13. Application information

### 13.1 Application diagrams

#### 13.1.1 Single-ended Application

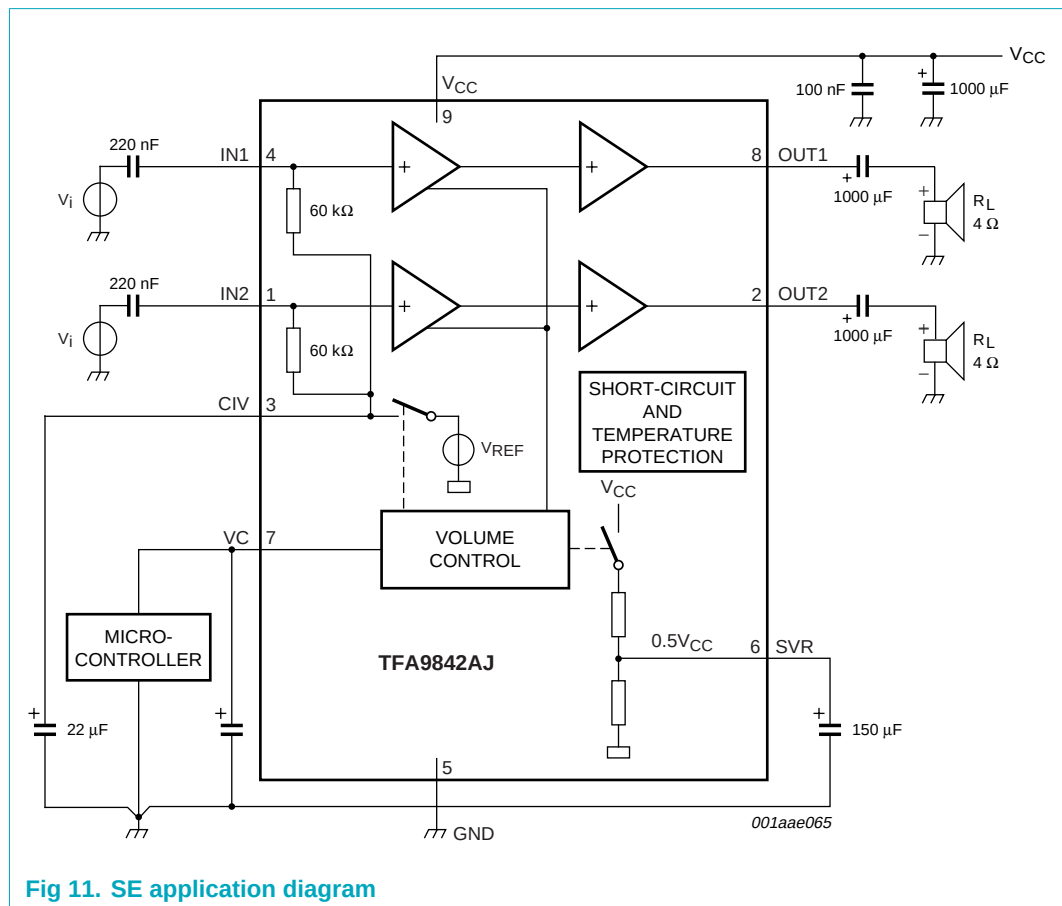
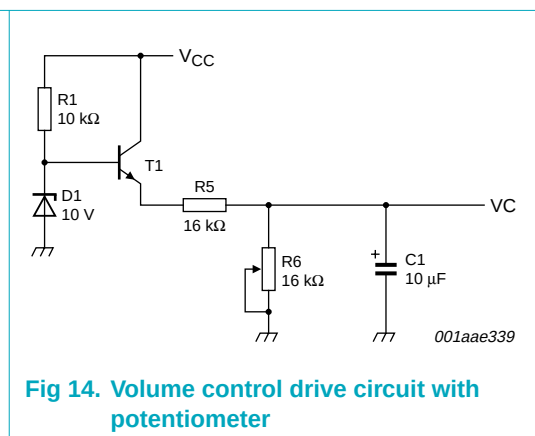
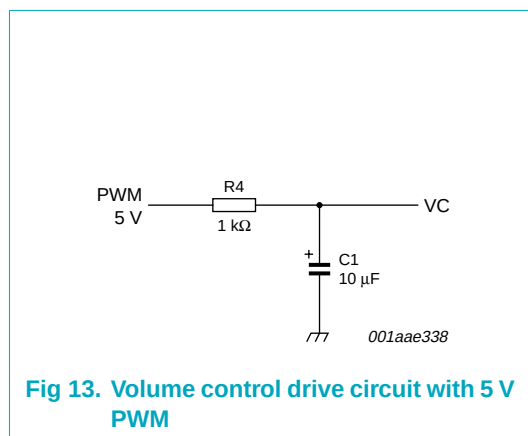
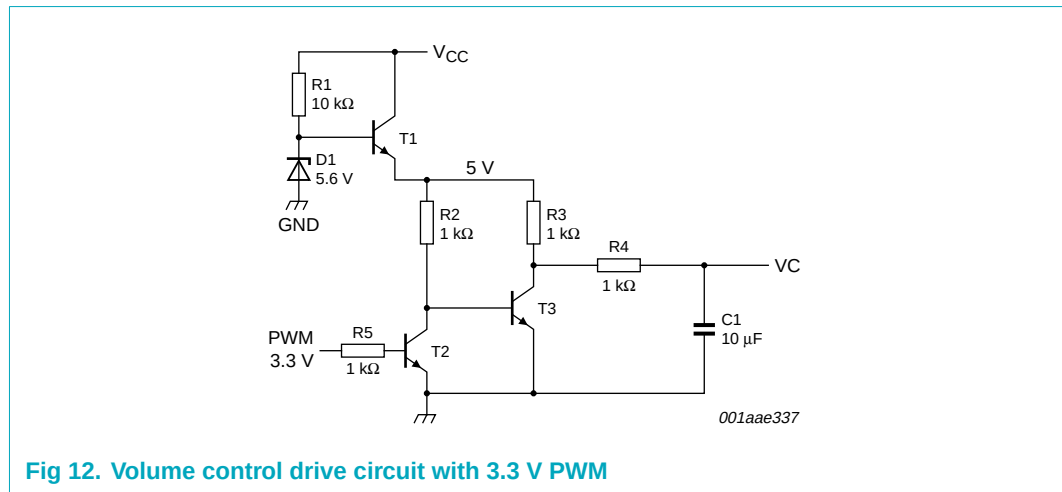


Fig 11. SE application diagram

**Remark:** Switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltage it is recommended to use (Schottky) diodes to the supply voltage and ground.

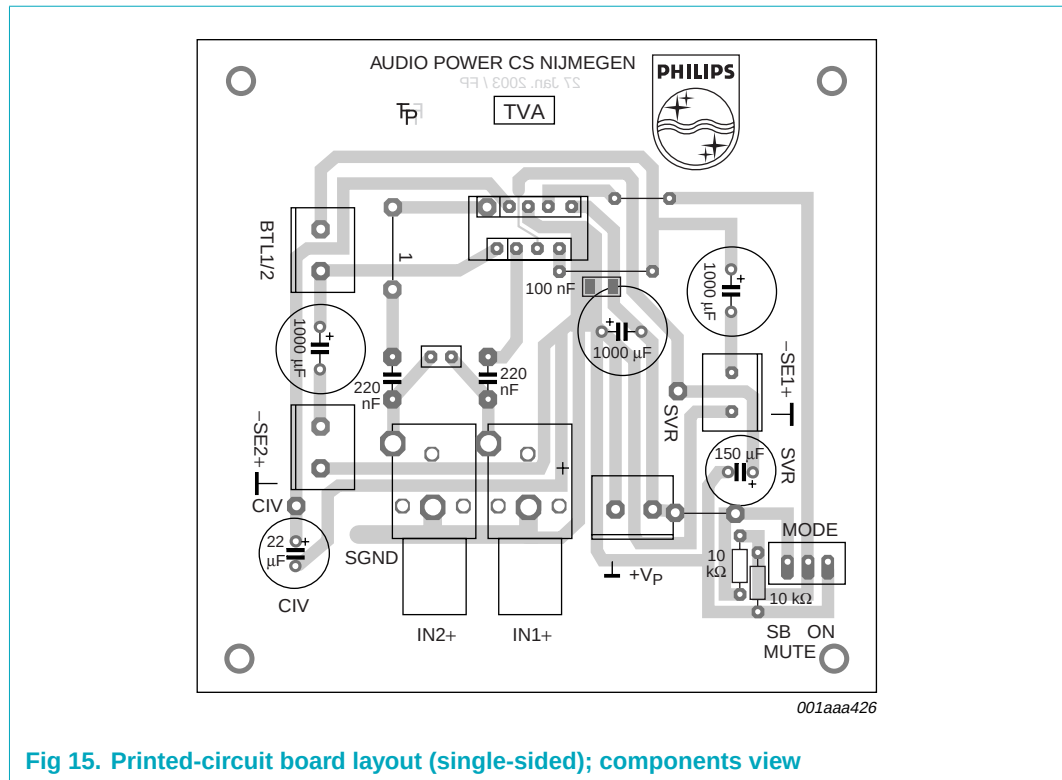
### 13.1.2 Volume control drive options



## 13.2 Printed-circuit board

### 13.2.1 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large output signal currents from interfering with the small AC input signals. The small-signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.



### 13.2.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR, typical 100 nF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 µF or greater, must be placed close to the device.

The bypass capacitor connected to pin SVR reduces the noise and ripple on the mid rail voltage. For good THD and noise performance a low ESR capacitor is recommended.

### 13.3 Thermal behavior and heatsink calculation

The measured maximum thermal resistance of the IC package,  $R_{th(j-mb)}$ , is 2.0 K/W. A calculation for the heatsink can be made, with the following parameters:

$$T_{amb(max)} = 60\text{ }^{\circ}\text{C (example)}$$

$$V_{CC} = 17\text{ V and } R_L = 4\text{ }\Omega\text{ (SE)}$$

$$T_{j(max)} = 150\text{ }^{\circ}\text{C (specification)}$$

$R_{th(tot)}$  is the total thermal resistance between the junction and the ambient including the heatsink. This can be calculated using the maximum temperature increase divided by the power dissipation:

$$R_{th(tot)} = (T_{j(max)} - T_{amb(max)})/P$$

At  $V_{CC} = 17\text{ V}$  and  $R_L = 4\ \Omega$  ( $2 \times \text{SE}$ ) the measured worst-case sine-wave dissipation is  $8.4\text{ W}$ ; see [Figure 8](#). For  $T_{j(max)} = 150\text{ }^\circ\text{C}$  the temperature raise, caused by the power dissipation, is:  $150\text{ }^\circ\text{C} - 60\text{ }^\circ\text{C} = 90\text{ }^\circ\text{C}$ :

$$P \times R_{th(tot)} = 90\text{ }^\circ\text{C}$$

$$R_{th(tot)} = 90/8.4\text{ K/W} = 10.7\text{ K/W}$$

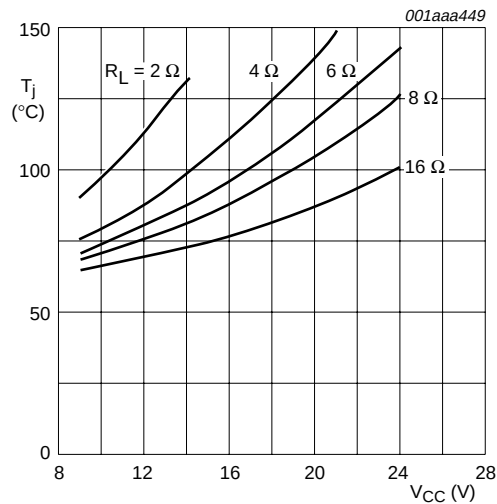
$$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 10.7\text{ K/W} - 2.0\text{ K/W} = 8.7\text{ K/W}$$

This calculation is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation (see [Section 8.2.2](#)). This allows for the use of a smaller heatsink:

$$P \times R_{th(tot)} = 90\text{ }^\circ\text{C}$$

$$R_{th(tot)} = 90/4.2\text{ K/W} = 21.4\text{ K/W}$$

$$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)} = 21.4\text{ K/W} - 2.0\text{ K/W} = 19.4\text{ K/W}$$



$2 \times \text{SE}$  loads;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; external heatsink of  $10\text{ K/W}$ ; music signals

**Fig 16. Junction temperature as function of supply voltage**

## 14. Test information

### 14.1 Quality information

The *General Quality Specification for Integrated Circuits*, SNW-FQ-611 is applicable.

15. Package outline

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die padSOT523-1

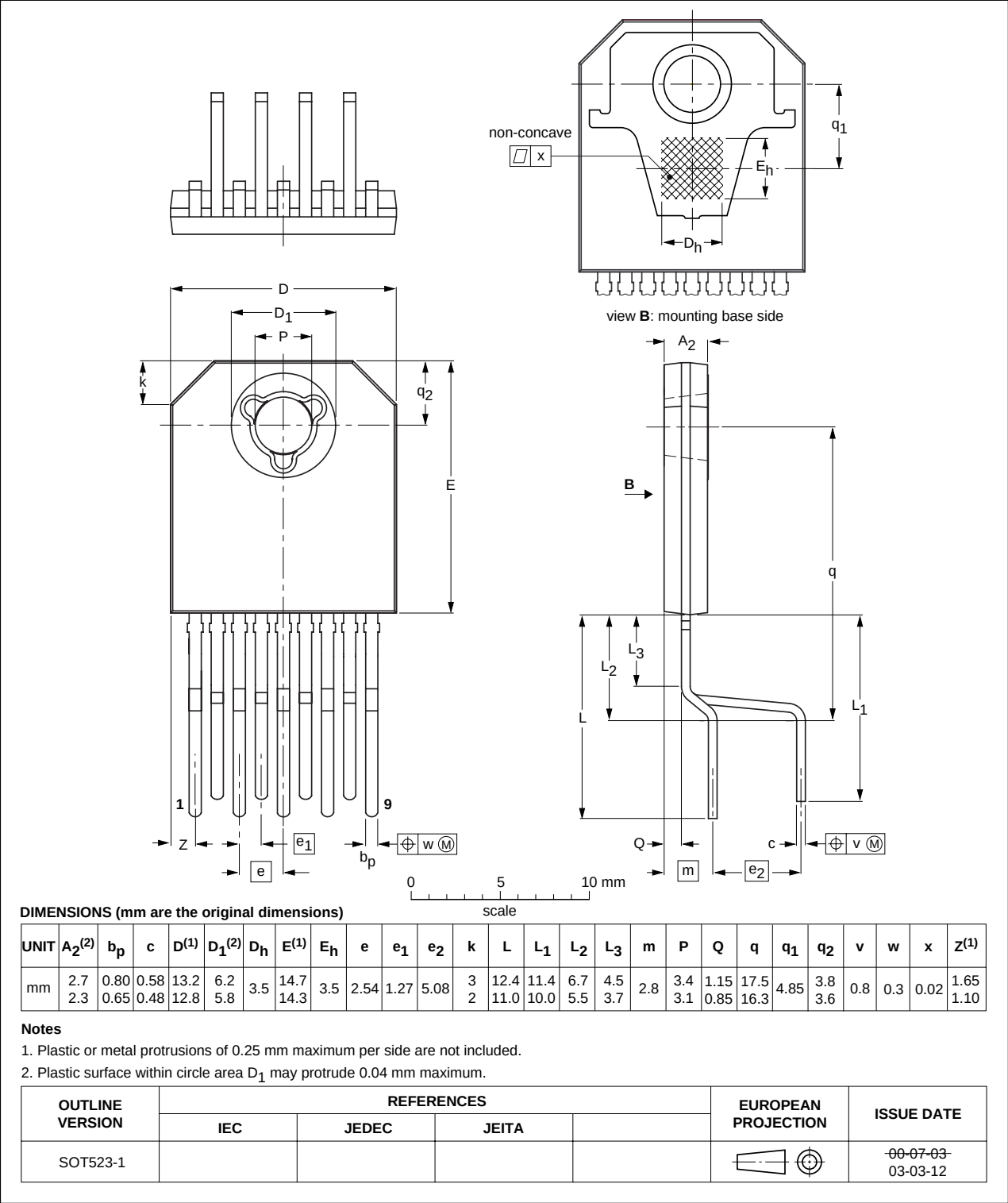


Fig 17. Package outline SOT523-1 (DBS9P)

## 16. Soldering

### 16.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

### 16.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{\text{stg(max)}}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### 16.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

### 16.4 Package related soldering information

**Table 10. Suitability of through-hole mount IC packages for dipping and wave soldering methods**

| Package                         | Soldering method |                         |
|---------------------------------|------------------|-------------------------|
|                                 | Dipping          | Wave                    |
| CPGA, HCPGA                     | -                | suitable                |
| DBS, DIP, HDIP, RDBS, SDIP, SIL | suitable         | suitable <sup>[1]</sup> |
| PMFP <sup>[2]</sup>             | -                | not suitable            |

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

17. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status      | Change notice | Supersedes |
|-------------|--------------|------------------------|---------------|------------|
| TFA9842AJ_1 | 20060428     | Preliminary data sheet | -             | -          |



## 18. Legal information

### 18.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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## 20. Contents

|           |                                                                 |           |           |                                      |           |
|-----------|-----------------------------------------------------------------|-----------|-----------|--------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> . . . . .                            | <b>1</b>  | <b>19</b> | <b>Contact information</b> . . . . . | <b>17</b> |
| <b>2</b>  | <b>Features</b> . . . . .                                       | <b>1</b>  | <b>20</b> | <b>Contents</b> . . . . .            | <b>18</b> |
| <b>3</b>  | <b>Applications</b> . . . . .                                   | <b>1</b>  |           |                                      |           |
| <b>4</b>  | <b>Quick reference data</b> . . . . .                           | <b>2</b>  |           |                                      |           |
| <b>5</b>  | <b>Ordering information</b> . . . . .                           | <b>2</b>  |           |                                      |           |
| <b>6</b>  | <b>Block diagram</b> . . . . .                                  | <b>3</b>  |           |                                      |           |
| <b>7</b>  | <b>Pinning information</b> . . . . .                            | <b>3</b>  |           |                                      |           |
| 7.1       | Pinning . . . . .                                               | 3         |           |                                      |           |
| 7.2       | Pin description . . . . .                                       | 4         |           |                                      |           |
| <b>8</b>  | <b>Functional description</b> . . . . .                         | <b>4</b>  |           |                                      |           |
| 8.1       | Input configuration . . . . .                                   | 4         |           |                                      |           |
| 8.2       | Power amplifier . . . . .                                       | 4         |           |                                      |           |
| 8.2.1     | Output power measurement . . . . .                              | 4         |           |                                      |           |
| 8.2.2     | Headroom . . . . .                                              | 5         |           |                                      |           |
| 8.3       | Mode selection . . . . .                                        | 5         |           |                                      |           |
| 8.4       | Supply voltage ripple rejection . . . . .                       | 5         |           |                                      |           |
| 8.5       | Built-in protection circuits . . . . .                          | 6         |           |                                      |           |
| <b>9</b>  | <b>Limiting values</b> . . . . .                                | <b>6</b>  |           |                                      |           |
| <b>10</b> | <b>Thermal characteristics</b> . . . . .                        | <b>6</b>  |           |                                      |           |
| <b>11</b> | <b>Static characteristics</b> . . . . .                         | <b>7</b>  |           |                                      |           |
| <b>12</b> | <b>Dynamic characteristics</b> . . . . .                        | <b>7</b>  |           |                                      |           |
| <b>13</b> | <b>Application information</b> . . . . .                        | <b>10</b> |           |                                      |           |
| 13.1      | Application diagrams . . . . .                                  | 10        |           |                                      |           |
| 13.1.1    | Single-ended Application . . . . .                              | 10        |           |                                      |           |
| 13.1.2    | Volume control drive options . . . . .                          | 11        |           |                                      |           |
| 13.2      | Printed-circuit board . . . . .                                 | 11        |           |                                      |           |
| 13.2.1    | Layout and grounding . . . . .                                  | 11        |           |                                      |           |
| 13.2.2    | Power supply decoupling . . . . .                               | 12        |           |                                      |           |
| 13.3      | Thermal behavior and heatsink calculation . . . . .             | 12        |           |                                      |           |
| <b>14</b> | <b>Test information</b> . . . . .                               | <b>13</b> |           |                                      |           |
| 14.1      | Quality information . . . . .                                   | 13        |           |                                      |           |
| <b>15</b> | <b>Package outline</b> . . . . .                                | <b>14</b> |           |                                      |           |
| <b>16</b> | <b>Soldering</b> . . . . .                                      | <b>15</b> |           |                                      |           |
| 16.1      | Introduction to soldering through-hole mount packages . . . . . | 15        |           |                                      |           |
| 16.2      | Soldering by dipping or by solder wave . . . . .                | 15        |           |                                      |           |
| 16.3      | Manual soldering . . . . .                                      | 15        |           |                                      |           |
| 16.4      | Package related soldering information . . . . .                 | 15        |           |                                      |           |
| <b>17</b> | <b>Revision history</b> . . . . .                               | <b>16</b> |           |                                      |           |
| <b>18</b> | <b>Legal information</b> . . . . .                              | <b>17</b> |           |                                      |           |
| 18.1      | Data sheet status . . . . .                                     | 17        |           |                                      |           |
| 18.2      | Definitions . . . . .                                           | 17        |           |                                      |           |
| 18.3      | Disclaimers . . . . .                                           | 17        |           |                                      |           |
| 18.4      | Trademarks . . . . .                                            | 17        |           |                                      |           |

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