

# CD4031B Types

## CMOS 64-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

■ CD4031B is a static shift register that contains 64 D-type, master-slave flip-flop stages and one stage which is a D-type master flip-flop only (referred to as a 1/2 stage).

The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 12 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031B has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. The MODE CONTROL input can also be used to select between two separate data sources. Register packages can be cascaded and the clock lines driven directly for high-speed operation. Alternatively, a delayed clock output (CL<sub>D</sub>) is provided that enables cascading register packages while allowing reduced clock drive fan-out and transition-time requirements. A third cascading option makes use of the Q' output from the 1/2 stage, which is available on the next negative-going transition of the clock after the Q output occurs. This delayed output, like the delayed clock CL<sub>D</sub>, is used with clocks having slow rise and fall times.

The CD4031B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal) ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub>+0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

### Features:

■ Fully static operation: DC to 12 MHz typ. @ V<sub>DD</sub>-V<sub>SS</sub> = 15 V

■ Standard TTL drive capability on Q output

■ Recirculation capability

■ Three cascading modes:

Direct clocking for high-speed operation

Delayed clocking for reduced clock drive requirements

Additional 1/2 stage for slow clocks

■ 100% tested for quiescent current at 20 V

■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C

■ Noise margin (over full package-temperature range)

1 V at V<sub>DD</sub> = 5 V

2 V at V<sub>DD</sub> = 10 V

2.5 V at V<sub>DD</sub> = 15 V

■ 5-V, 10-V, and 15-V parametric ratings

■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

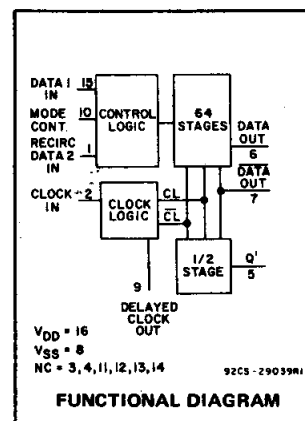
■ Serial shift registers

■ Time delay circuits

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> =Full Package-Temperature Range)	3	18	V



### INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE 1
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

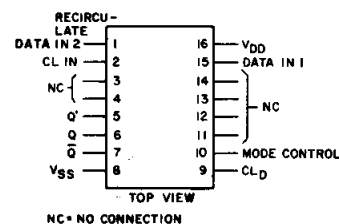
### TYPICAL STAGE TRUTH TABLE

Data	CL	Data + 1
0		0
1		1
X		NC

### TRUTH TABLE FOR OUTPUT FROM Q' (TERMINAL 5)

Data + 64	CL	Data + 64½
0		0
1		1
X		NC

1 = HIGH LEVEL      0 = LOW LEVEL  
X = DON'T CARE      NC = NO CHANGE



### TERMINAL ASSIGNMENT

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4031B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25				
								Min.	Typ.	Max.		
Quiescent Device Current, I <sub>DD</sub> Max.	—	0.5	5	5	5	150	150	—	0.04	5	μA	
	—	0.10	10	10	10	300	300	—	0.04	10		
	—	0.15	15	20	20	600	600	—	0.04	20		
	—	0.20	20	100	100	3000	3000	—	0.08	100		
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0.5	5	2.56	2.44	1.68	1.44	2.04	4	—	mA	
Q, Q̄, Q', CL <sub>D</sub>	0.5	0.10	10	6.4	6	4.4	3.6	5.2	10.4	—		
	1.5	0.15	15	16.8	16	11.2	9.6	13.6	27.2	—		
	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—		
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—		
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA	
Q, Q̄, Q', CL <sub>D</sub>	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—		
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.5	5	0.05			—			0	0.05	V
	—	0.10	10	0.05			—			0	0.05	
	—	0.15	15	0.05			—			0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.5	5	4.95			4.95			5	—	V
	—	0.10	10	9.95			9.95			10	—	
	—	0.15	15	14.95			14.95			15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5			—			—	1.5	V
	1.9	—	10	3			—			—	3	
	1.5, 13.5	—	15	4			—			—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5			3.5			—	—	V
	1.9	—	10	7			7			—	—	
	1.5, 13.5	—	15	11			11			—	—	
Input Current I <sub>IN</sub> Max.		0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA	

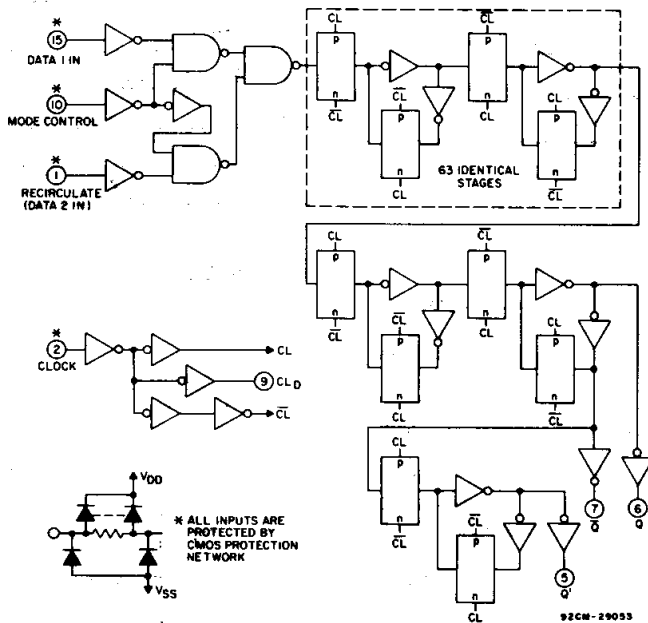


Fig. 1 — Logic diagram.

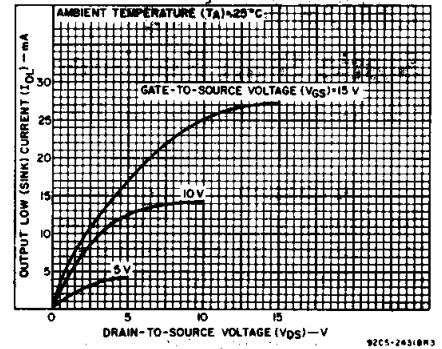


Fig. 2 — Typical output low (sink) current characteristics ( $I_{OL}$  sink current = 4X ordinate).

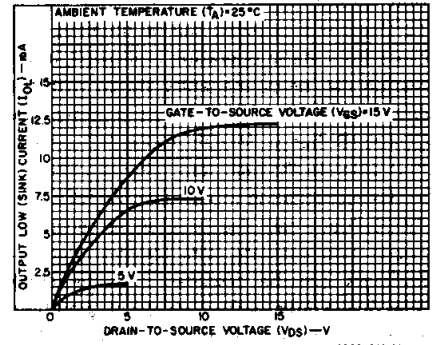


Fig. 3 — Minimum output low (sink) current characteristics ( $I_{OL}$  sink current = 4X ordinate).

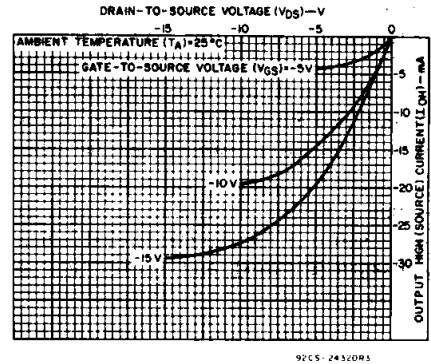


Fig. 4 — Typical output high (source) current characteristics.

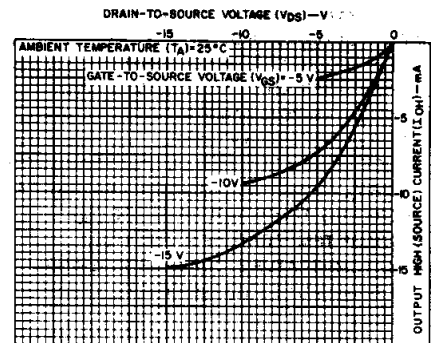


Fig. 5 — Minimum output high (source) current characteristics.

# CD4031B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  
 $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	$V_{DD}(\text{V})$	Min.	Typ.	Max.	
Propagation Delay Time: Clock to $\bar{Q}$ , $t_{PHL}$ , $t_{PLH}$ ; Clock to $Q$ , $t_{PLH}$	5	—	250	500	ns
	10	—	110	220	
	15	—	90	180	
Clock to $Q'$ , $t_{PHL}$ , $t_{PLH}$ ; Clock to $Q$ , $t_{PHL}$	5	—	190	380	ns
	10	—	80	160	
	15	—	65	130	
Clock to $CL_D$	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Transition Time, $t_{THL}$ , $t_{TLH}$ (Any Output, except $Q$ , $t_{THL}$ )	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
$Q$ , $t_{THL}$	5	—	50	100	ns
	10	—	25	50	
	15	—	20	40	
Minimum Data Setup Time, $t_S$	5	—	30	60	ns
	10	—	15	30	
	15	—	10	20	
Minimum Data Hold Time, $t_H$	5	—	30	60	ns
	10	—	15	30	
	15	—	10	20	
Minimum Clock Pulse Width, $t_W$	5	—	120	240	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, $f_{CL}^{**}$	5	2	4	—	MHz
	10	5	10	—	
	15	6	12	—	
Clock Input Rise or Fall Time, $t_{rCL}$ , $t_{fCL}^*$	5	—	—	1000	$\mu\text{s}$
	10	—	—	1000	
	15	—	—	200	
Input Capacitance, $C_{IN}$ (Any Input)	—	—	5	7.5	pF

\*If more than one unit is cascaded in the parallel clocked application,  $t_{rCL}$  should be made less than or equal to the sum of the propagation delay at 50 pF and the transition time of the output driving stage.

\*\*Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature in Recirculation Mode:

$$f_{\max} = \frac{1}{(n-1) C_{LD} \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}} \quad \text{where } n = \text{number of packages}$$

b) Not Using Delayed Clock:

$$f_{\max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$$

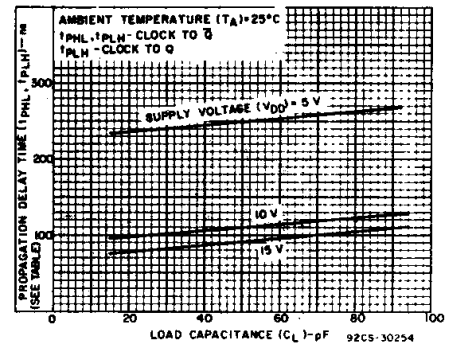


Fig. 6 — Typical propagation delay time as a function of load capacitance (see table).

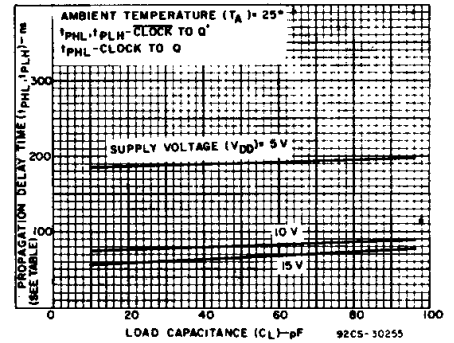


Fig. 7 — Typical propagation delay time as a function of load capacitance (see table).

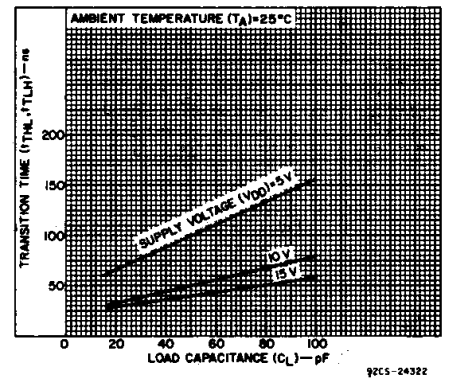


Fig. 8 — Typical transition time as a function of load capacitance (except  $Q$ ,  $t_{THL}$ ).

## CD4031B Types

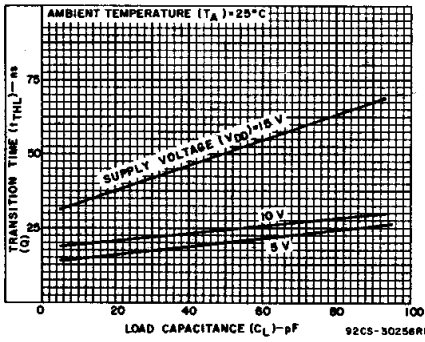


Fig. 9 - Typical transition time as a function of load capacitance ( $Q$ ,  $t_{TL}$ ).

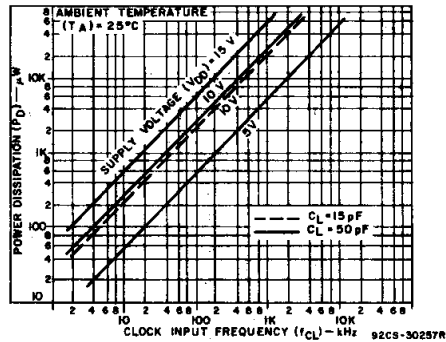


Fig. 10 - Typical dynamic power dissipation as a function of clock input frequency.

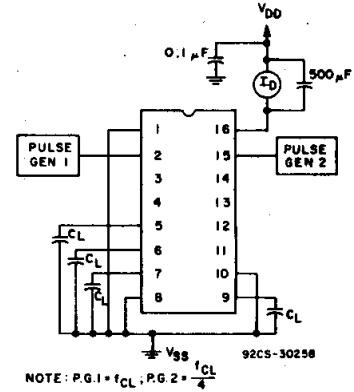


Fig. 11 - Dynamic power dissipation test circuit.

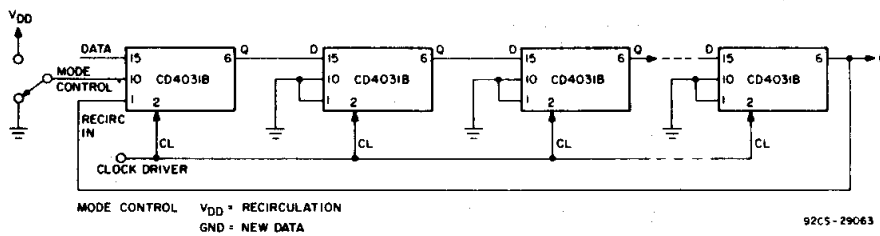


Fig. 12 - Cascading using direct clocking for high-speed operation (see clock rise and fall time requirement).

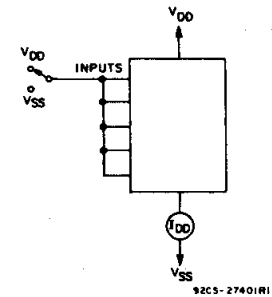


Fig. 13 - Quiescent-device-current test circuit.

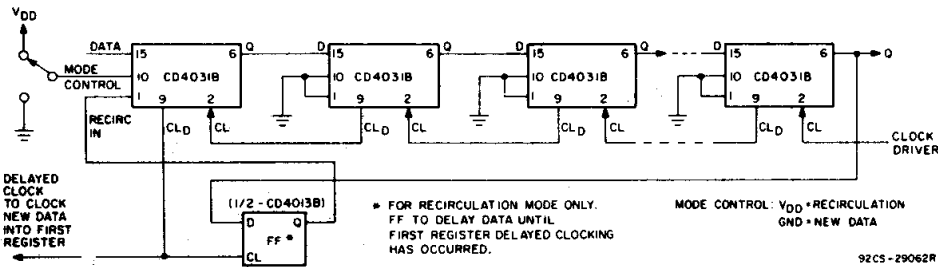


Fig. 14 - Cascading using delayed clocking for reduced clock drive requirements.

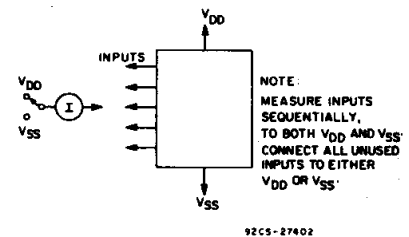


Fig. 15 - Input-leakage current.

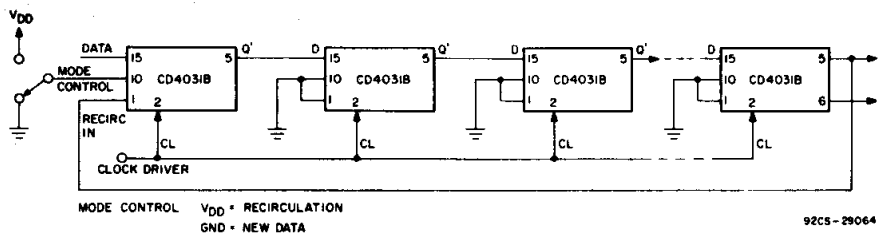


Fig. 16 - Cascading using half-clock-pulse delayed data output ( $Q'$ ) to permit use of slow rise and fall time clock inputs.

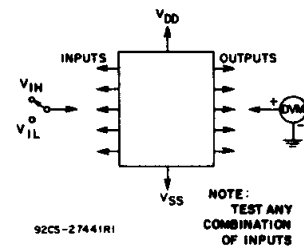
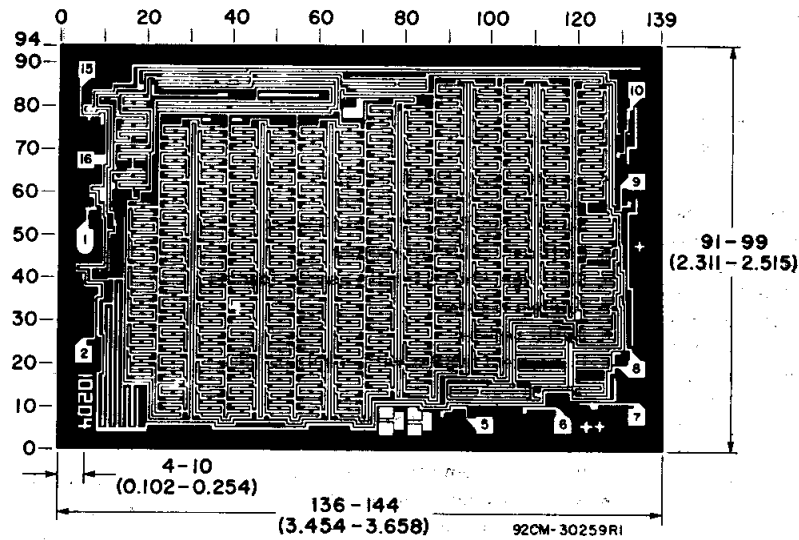


Fig. 17 - Input-voltage test circuit.

## CD4031B Types



Chip dimensions and pad layout for CD4031B

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4031BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4031BE	<a href="#">Samples</a>
CD4031BF3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4031BF3A	<a href="#">Samples</a>
CD4031BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B	<a href="#">Samples</a>
CD4031BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM031B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD4031B, CD4031B-MIL :**

- Catalog : [CD4031B](#)
- Military : [CD4031B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4031BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4031BPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

## TUBE



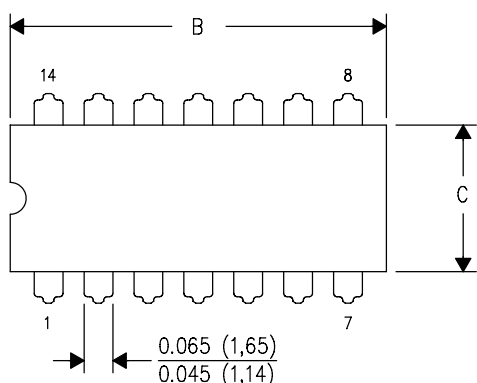
\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4031BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4031BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4031BPW	PW	TSSOP	16	90	530	10.2	3600	3.5

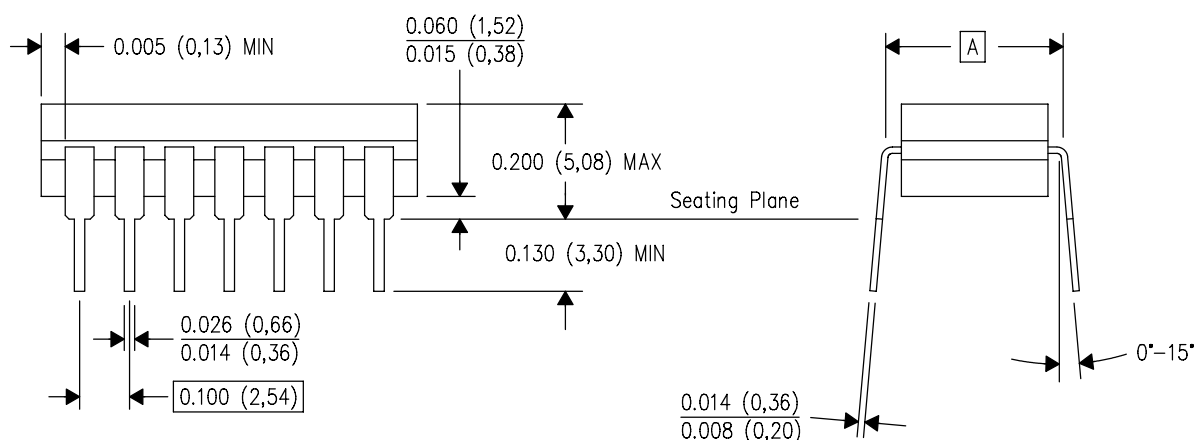
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



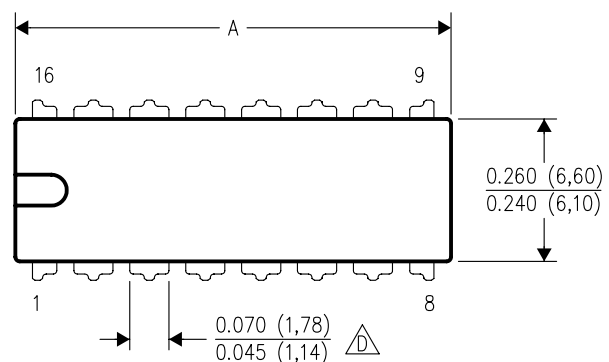
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

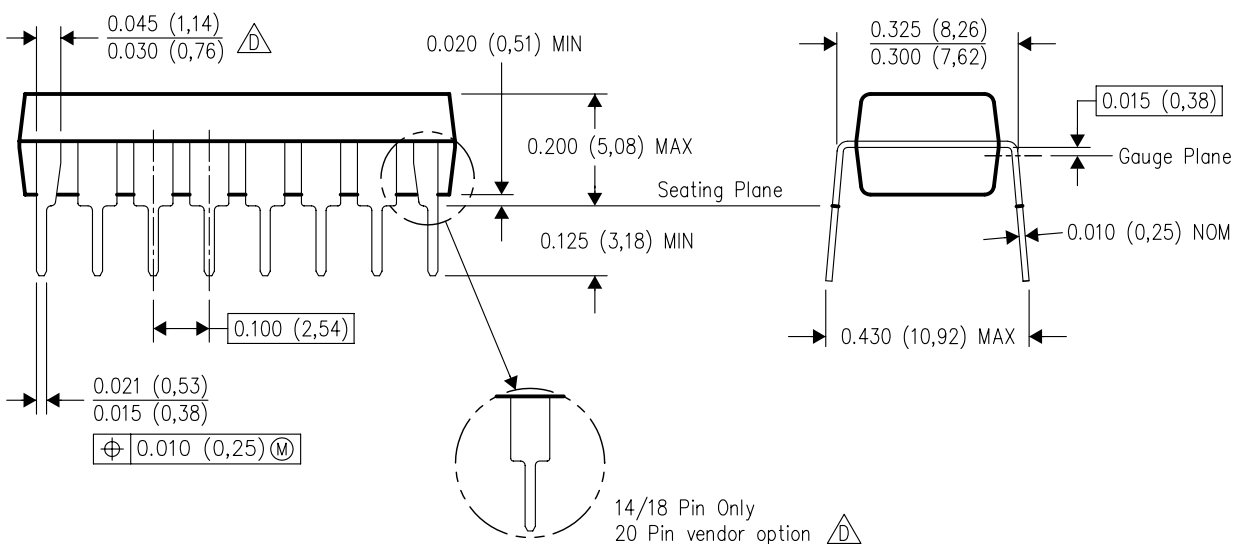
N (R-PDIP-T\*\*)

16 PINS SHOWN



## PLASTIC DUAL-IN-LINE PACKAGE

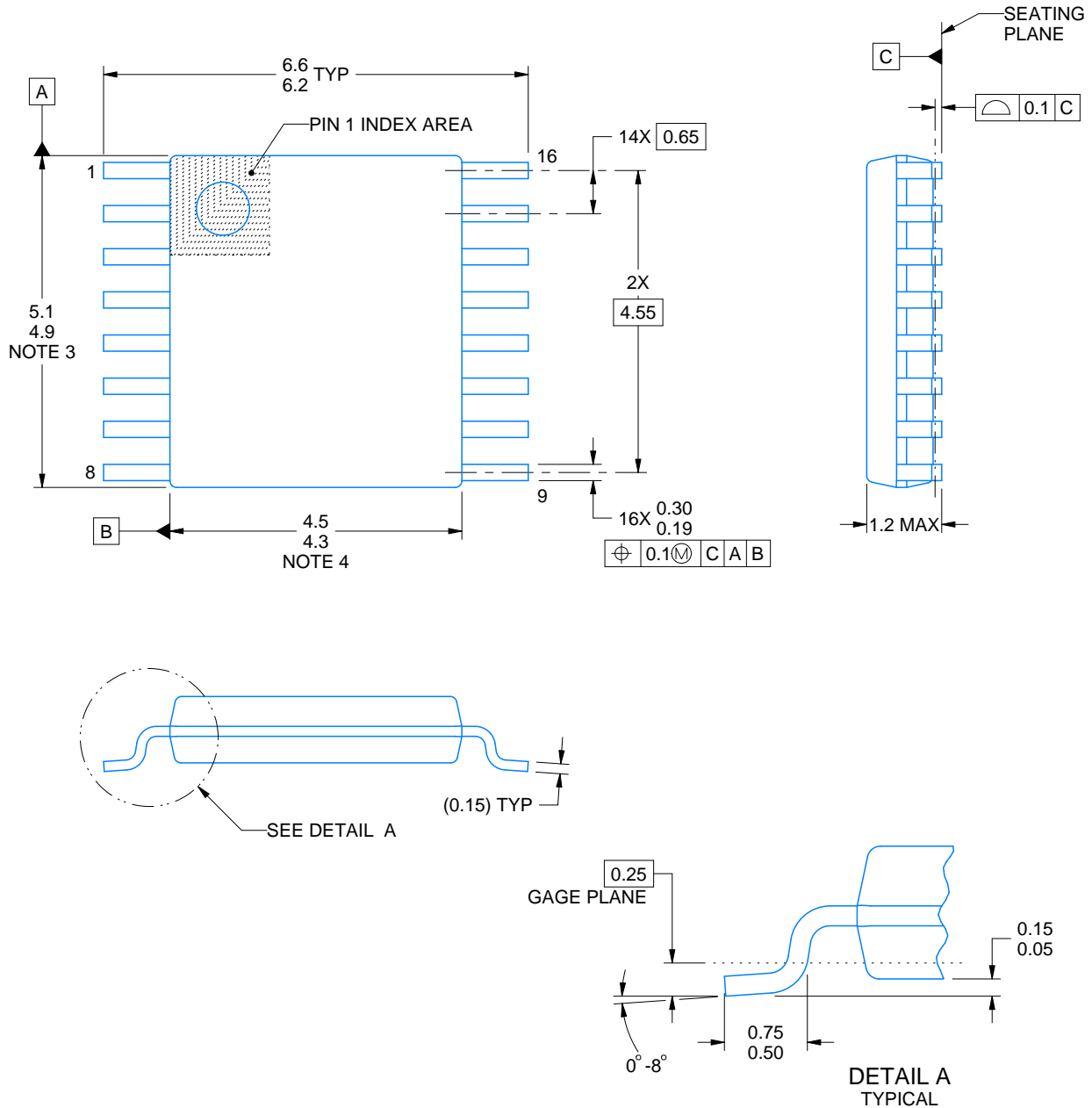


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220204/A 02/2017

## NOTES:

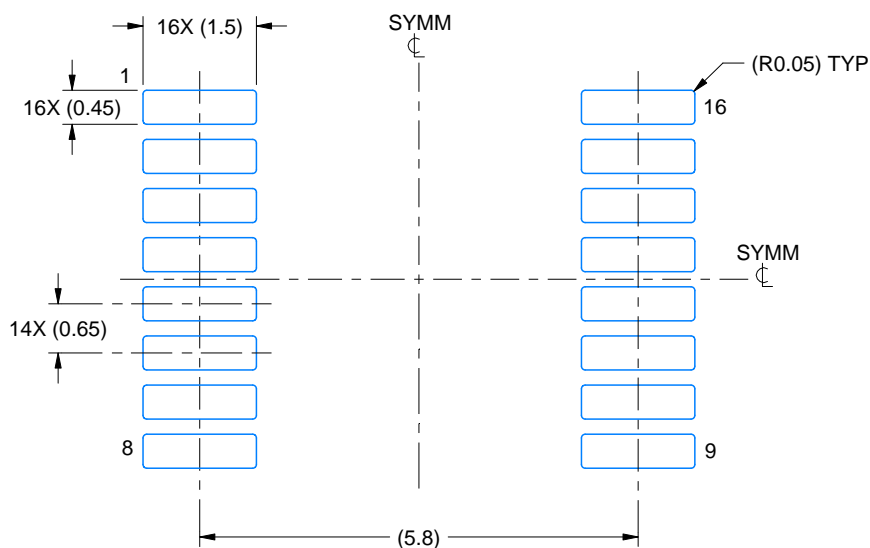
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

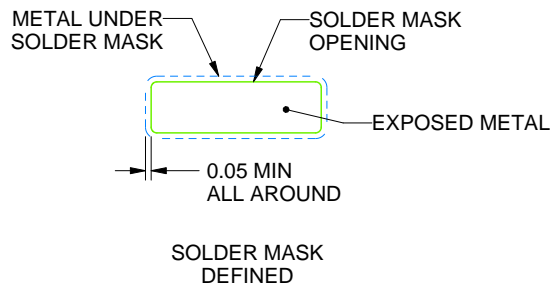
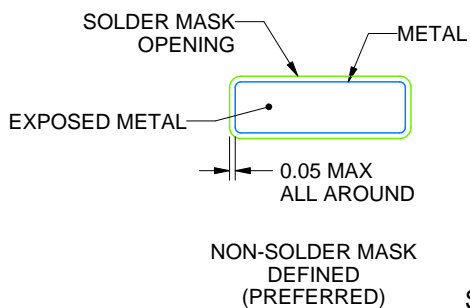
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

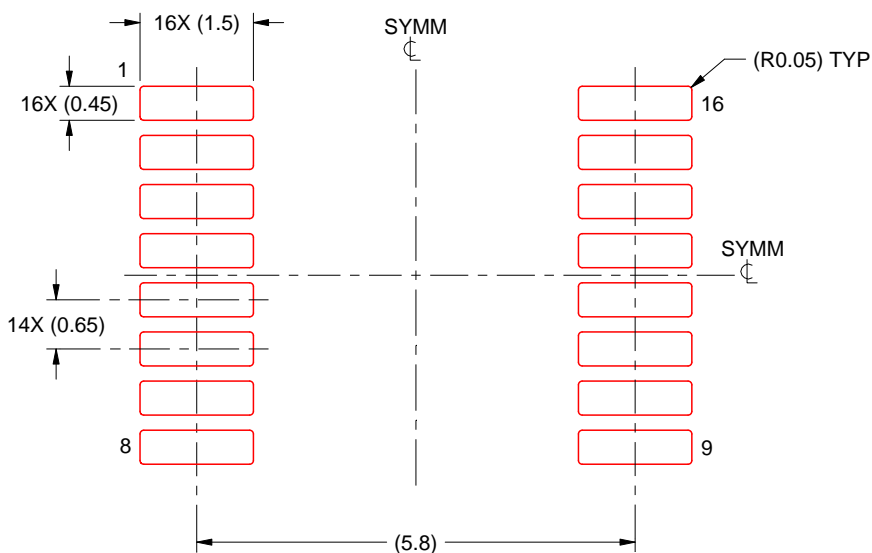
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated