



FSA2257

Low R_{ON} , Low-Voltage Dual SPDT Bi-Directional Analog Switch

Features

- Maximum 1.15 Ω On Resistance (R_{ON}) at 4.5 V V_{CC}
- 0.3 Ω Maximum R_{ON} Flatness at +5 V V_{CC}
- Space-Saving MicroPak™
- Broad V_{CC} Operating Range: 1.65 V to 5.50 V
- Fast Turn-On and Turn-Off Time
- Break-Before-Make Enable Circuitry
- Over-Voltage Tolerant TTL-Compatible Control Input

Applications

- Cell Phone
- PDA
- Mobile Devices

Description

The FSA2257 is a high-performance bi-directional dual Single-Pole/Double-Throw (SPDT) analog switch. This switch can be configured as either a multiplexer or a de-multiplexer by select pins. The device features ultra-low R_{ON} of 1.3 Ω maximum at 4.5 V V_{CC} and operates over the wide V_{CC} range of 1.65 V to 5.50 V. The device is fabricated with submicron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation. The select input is TTL-level compatible.

Ordering Information

Part Number	Package Number	Top Mark	Package Description	Packing Method
FSA2257L10X	MAC10A	EP	10-Lead MicroPak™, 1.6 x 2.1 mm	5000 Units Tape and Reel
FSA2257MTCX	MCT14	FSA2257	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	2500 Units Tape and Reel
FSA2257MUX	MUA10A	FSA 2257	10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0 mm	4000 Units Tape and Reel

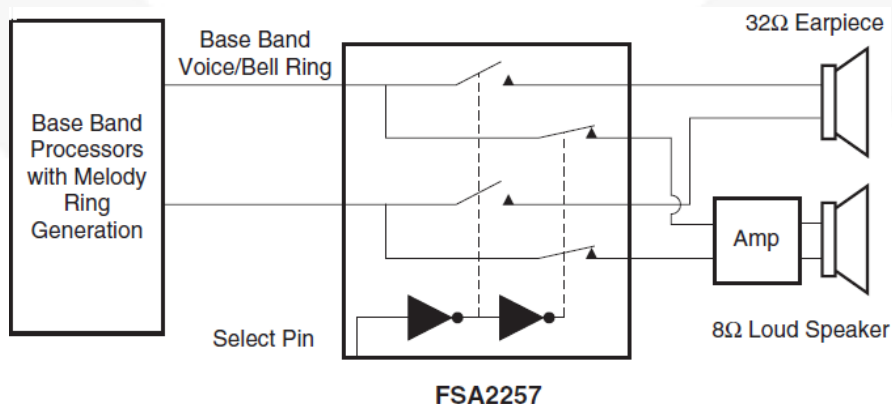


Figure 1. Block Diagram

Pin Configurations

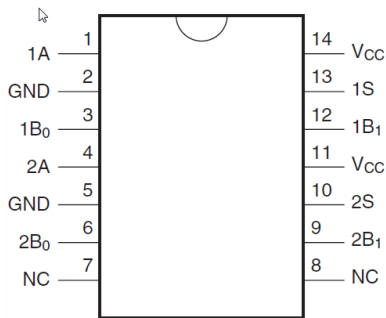


Figure 2. Pin Assignments for TSSOP (Top View)

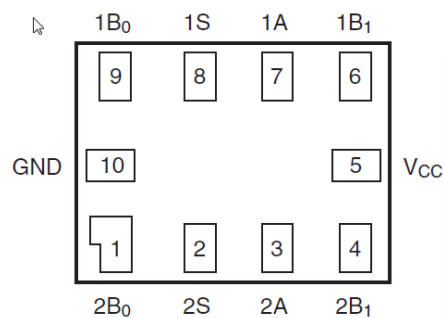


Figure 3. MicroPak™ Pad Assignments (Top View)

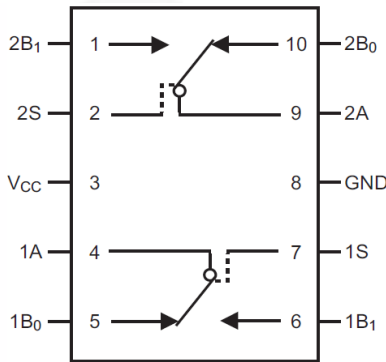


Figure 4. Pin Assignments for MSOP (Top View)

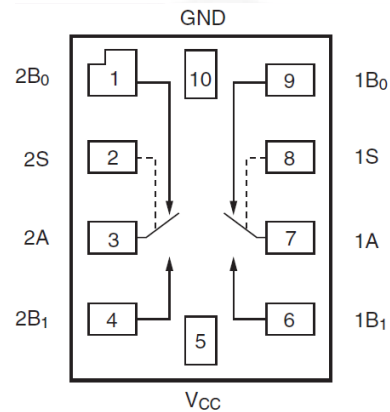


Figure 5. Analog Symbols (Top Through View)

Pin Definitions

Pin# TSSOP	Pin# MicroPak™	Pin # MSOP	Name	Description
1	7	4	1A	Data Ports
2,5	10	8	GND	Ground
3	9	5	1B ₀	Data Ports
4	3	9	2A	Data Ports
6	1	10	2B ₀	Data Ports
7,8			NC	No Connect
9	4	1	2B ₁	Data Ports
10	2	2	2S	Control Inputs
11,14	5	3	V _{CC}	Power Supply
12	6	6	1B ₁	Data Ports
13	8	7	1S	Control Inputs

Truth Table

Control Input (S)	Function
Low Logic Level	B ₀ connected to A
High Logic Level	B ₁ connected to A

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		-0.5	6.0	V
V _{SW}	DC Switch Voltage ⁽¹⁾		-0.5	V _{CC} + 0.5	V
V _{IN}	DC Input Voltage ⁽¹⁾		-0.5	6.0	V
I _{IK}	Input Diode Current		-50		mA
	Switch Current			200	
	Peak Switch Current (Pulsed at 1 ms duration, <10% duty cycle)			400	
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Maximum Junction Temperature			+150	°C
T _L	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		8000	V
		Charged Device Model, JESD22-C101		2000	

Note:

1. Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V _{CC}	Supply Voltage		1.65	5.50	V
V _{CNTRL}	Control Input Voltage ⁽²⁾		0	V _{CC}	V
V _{SW}	Switch Input Voltage		0	V _{CC}	V
T _A	Operating Temperature		-40	+85	°C

Note:

2. Unused control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			T _A =-40°C to +85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	Input Voltage High		1.8 to 2.7				1.0		V
			2.7 to 3.6				2.0		
			4.5 to 5.5				2.4		
V _{IL}	Input Voltage Low		1.8 to 2.7					0.4	V
			2.7 to 3.6					0.6	
			4.5 to 5.5					0.8	
I _{IN}	Control Input Leakage	V _{IN} =0 V to V _{CC}	2.7 to 3.6				-1.0	1.0	μA
			4.5 to 5.5				-1.0	1.0	
I _{NO(OFF)} , I _{NC(OFF)}	Off Leakage Current of Port B ₀ and B ₁	A=1 V, 4.5 V, B ₀ or B ₁ =1 V, 4.5 V	5.5	-2		2	-20	20	nA
I _{A(ON)}	On Leakage Current of Port A	A=1 V, 4.5V, B ₀ or B ₁ =1 V, 4.5 V or Floating	5.5	-4		2	-40	40	nA
R _{ON}	Switch On Resistance MicroPak ⁽³⁾	I _{OUT} =100 mA, B ₀ or B ₁ =1.5 V	1.8		4.6				Ω
			2.7		2.6	4.0		4.3	
	Switch On Resistance MSOP/TSSOP ⁽³⁾	I _{OUT} =100 mA, B ₀ or B ₁ =3.5 V	4.5		0.95	1.15		1.30	
ΔR _{ON}	On Resistance Matching Between Channels MicroPak ⁽⁴⁾	I _{OUT} =100 mA, B ₀ or B ₁ =3.5 V	4.5		0.06	0.12		0.15	Ω
	On Resistance Matching Between Channels MSOP / TSSOP ⁽⁴⁾		4.5		0.7			0.3	
R _{FLAT(ON)}	On Resistance Flatness ⁽⁵⁾	I _{OUT} =100 mA, B ₀ or B ₁ =0 V, 0.75 V, 1.5 V	1.8		3.0				Ω
			2.7		1.4				
		I _{OUT} =100 mA, B ₀ or B ₁ =0 V, 1 V, 2 V	4.5		0.2	0.3		0.4	
I _{CC}	Quiescent Supply Current	V _{IN} =0 V or V _{CC} , I _{OUT} =0 V	3.6		0.1	0.5		1.0	μA
			5.5		0.1	0.5		1.0	

Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- ΔR_{ON} = R_{ONmax} – R_{ONmin} measured at identical V_{CC}, temperature, and voltage.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

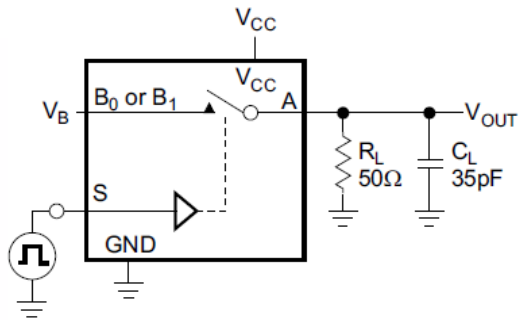
Typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			T _A =-40°C to +85°C		Unit	Figure
				Min.	Typ.	Max.	Min.	Max.		
t _{ON}	Turn-On Time	B ₀ or B ₁ =1.5 V, R _L =50 Ω, C _L =35 pF	1.8 to 2.7		75				ns	Figure 6
			2.7 to 3.6			50		60		
		B ₀ or B ₁ =3.0 V, R _L =50 Ω, C _L =35 pF	4.5 to 5.5			35		40		
t _{OFF}	Turn-Off Time	B ₀ or B ₁ =1.5 V, R _L =50 Ω, C _L =35 pF	1.8 to 2.7		20				ns	Figure 6
			2.7 to 3.6			20		30		
		B ₀ or B ₁ =3.0 V, R _L =50 Ω, C _L =35 pF	4.5 to 5.5			15		20		
t _{BBM}	Break-Before-Make Time	B ₀ or B ₁ =1.5 V, R _L =50 Ω, C _L =35 pF	2.7 to 3.6				1		ns	Figure 7
		B ₀ or B ₁ =3.0 V, R _L =50 Ω, C _L =35 pF	4.5 to 5.5		20		1			
Q	Charge Injection	C _L =1.0 nF, V _{GEN} =0 V, R _{GEN} =0 Ω	2.7 to 3.6		20				pC	Figure 9
			4.5 to 5.5		10					
OIRR	Off Isolation	f=1 MHz, R _L =50 Ω	2.7 to 3.6		-70				dB	Figure 8
			4.5 to 5.5		-70					
Xtalk	Crosstalk	f=1 MHz, R _L =50 Ω	2.7 to 3.6		-75				dB	Figure 8
			4.5 to 5.5		-75					
BW	-3 db Bandwidth	R _L =50 Ω	2.7 to 3.6		200				MHz	Figure 11
			4.5 to 5.5		200					
THD	Total Harmonic Distortion	R _L =600 Ω, V _{IN} =0.5 V _{PP} f=20 Hz to 20 kHz	2.7 to 3.6		0.002				%	Figure 12
			4.5 to 5.5		0.002					

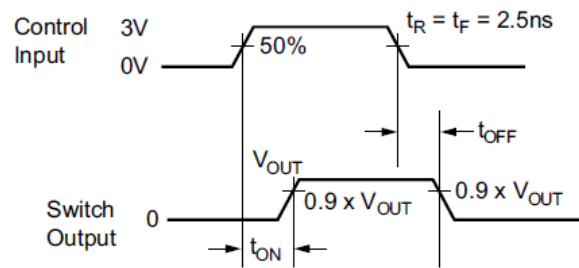
Capacitance

Symbol	Parameter	Conditions	V _{CC} (V)	T _A =+25°C			Unit	Figure
				Min.	Typ.	Max.		
C _{IN}	Control Pin Input Capacitance	f=1 MHz	0		3.5		pF	Figure 10
C _{OFF}	B Port Off Capacitance	f=1 MHz	4.5		12.0		pF	Figure 10
C _{ON}	A Port On Capacitance	f=1 MHz	4.5		40.0		pF	Figure 10

AC Loadings and Waveforms

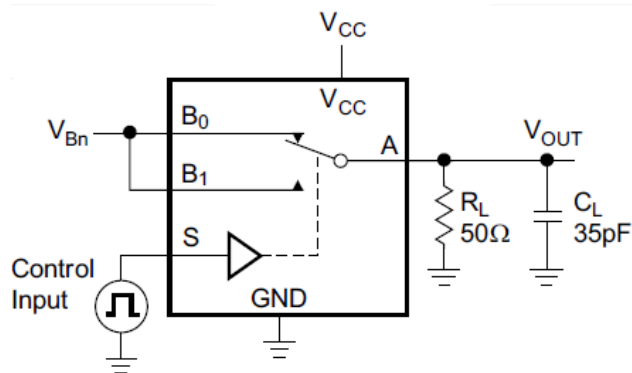


C_L Includes Fixture and Stray Capacitance



Logic Input Waveforms Inverted for Switches that have the Opposite Logic Sense

Figure 6. Turn On / Off Timing



C_L Includes Fixture and Stray Capacitance

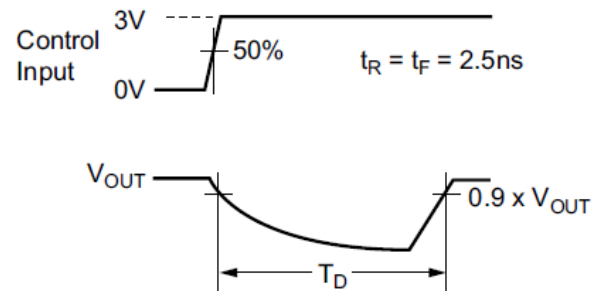


Figure 7. Break Before Make Timing

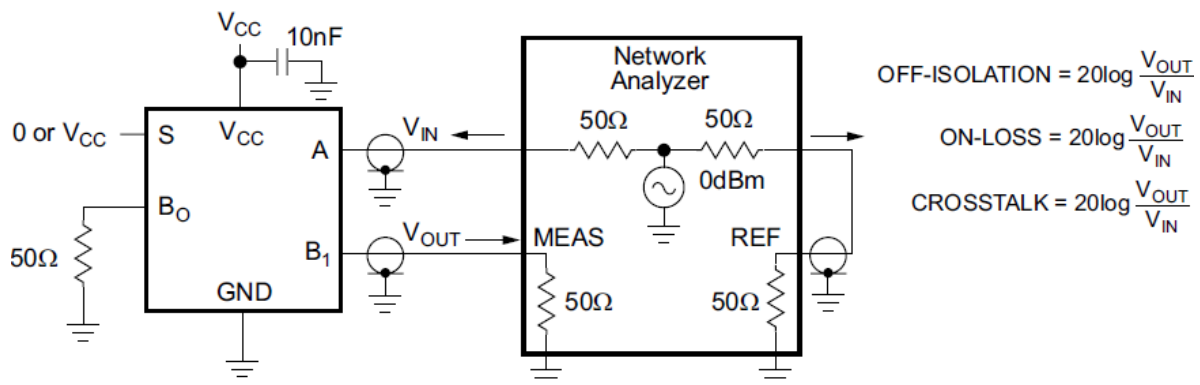


Figure 8. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)

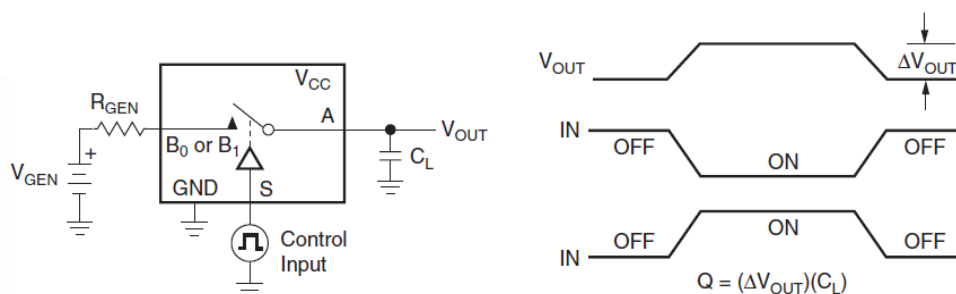


Figure 9. Charge Injection

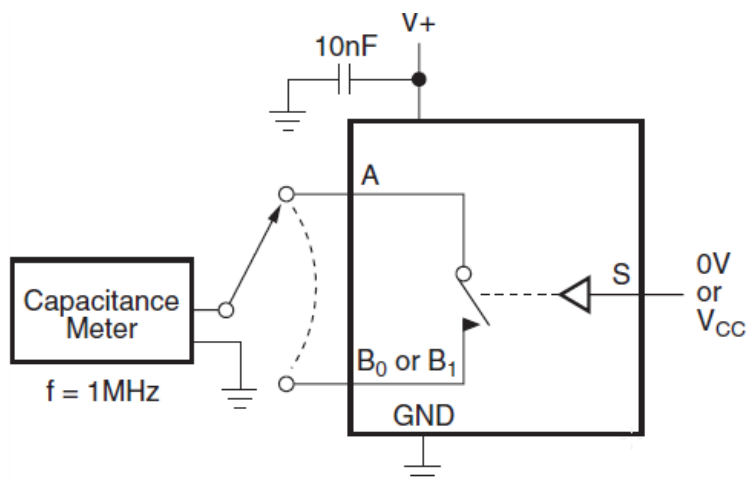


Figure 10. On / Off Capacitance Measurement Setup

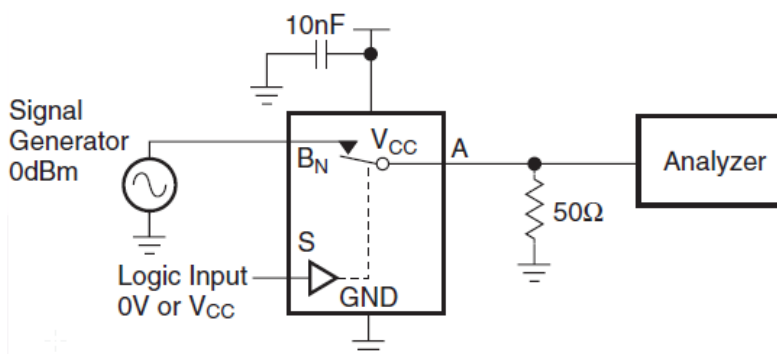


Figure 11. Bandwidth

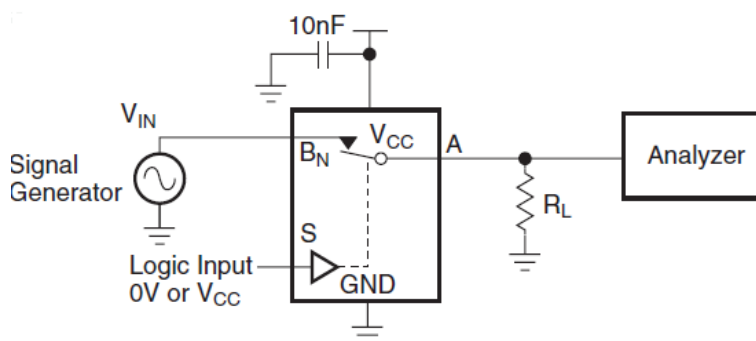
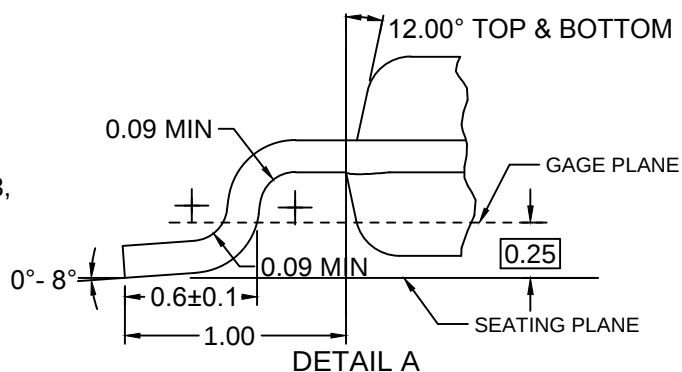
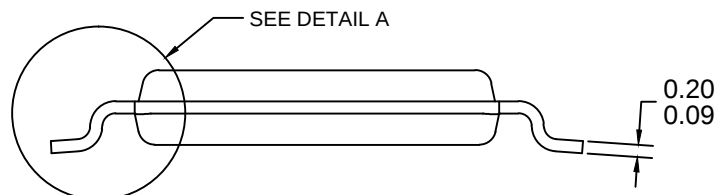
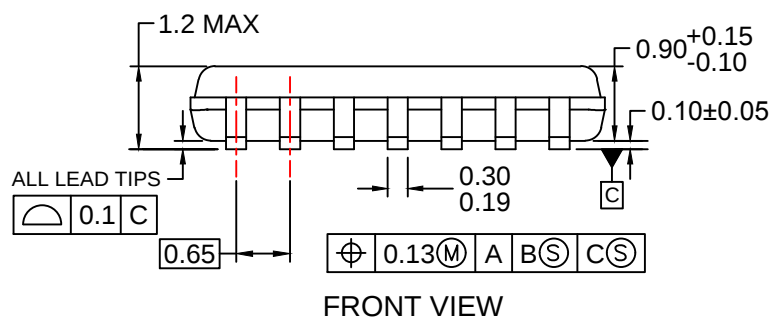
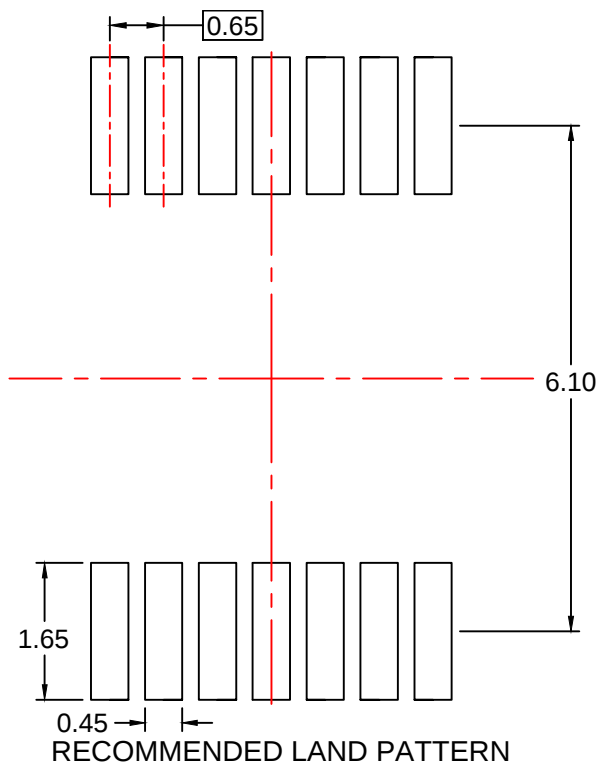
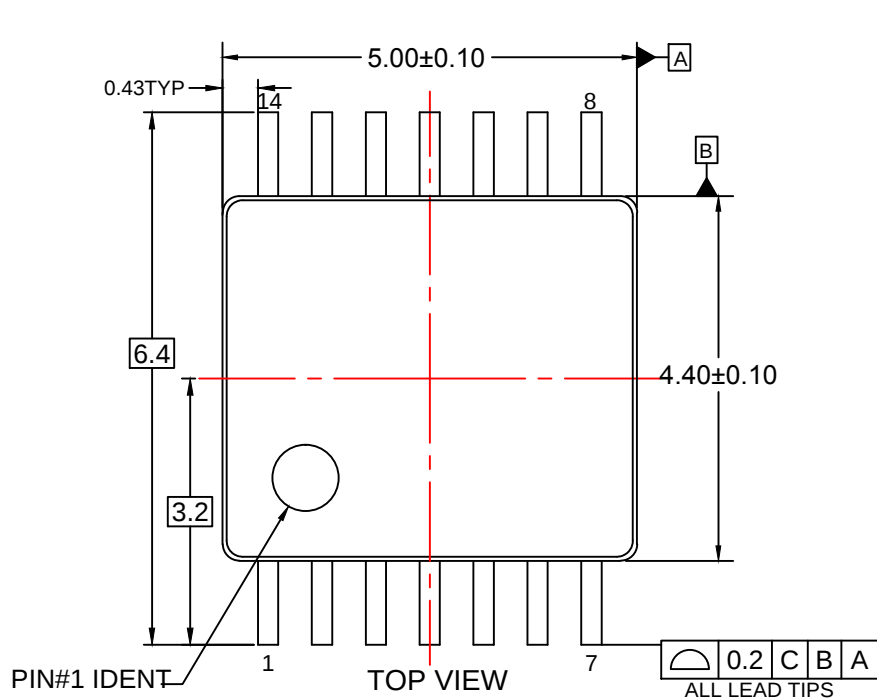


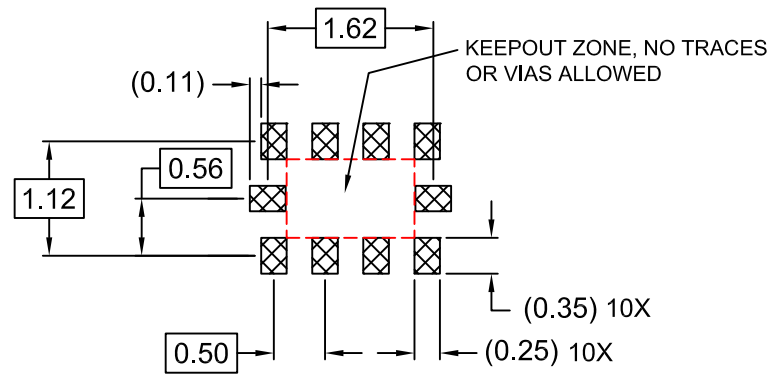
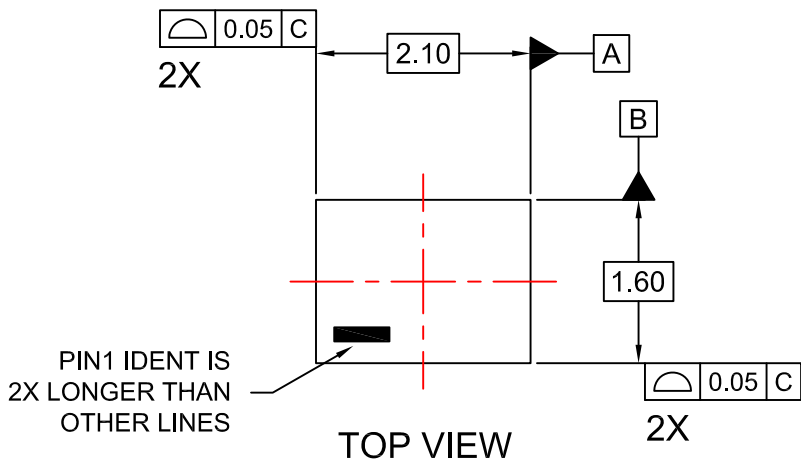
Figure 12. Harmonic Distortion



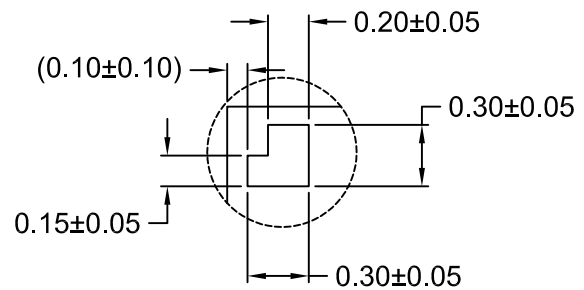
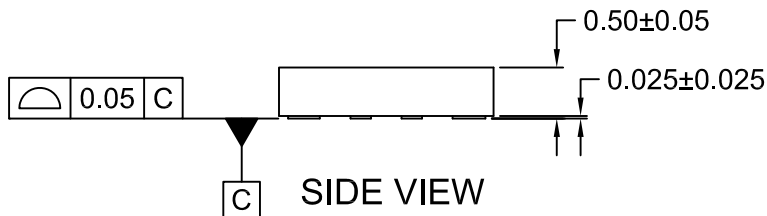
NOTES:

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- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 2009.
- LANDPATTERN STANDARD: SOP65P640X110-14M.
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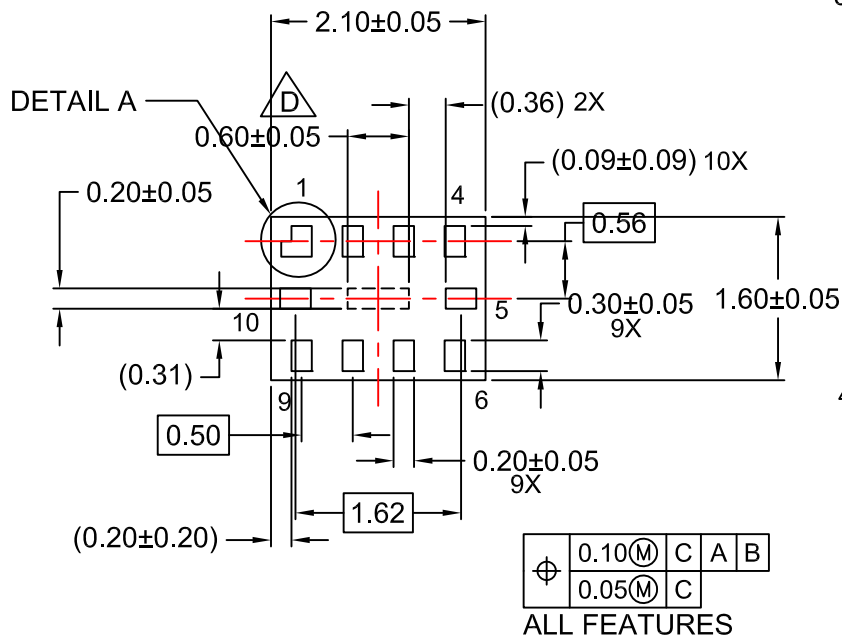




RECOMMENDED LAND PATTERN



DETAIL A 2X SCALE



BOTTOM VIEW

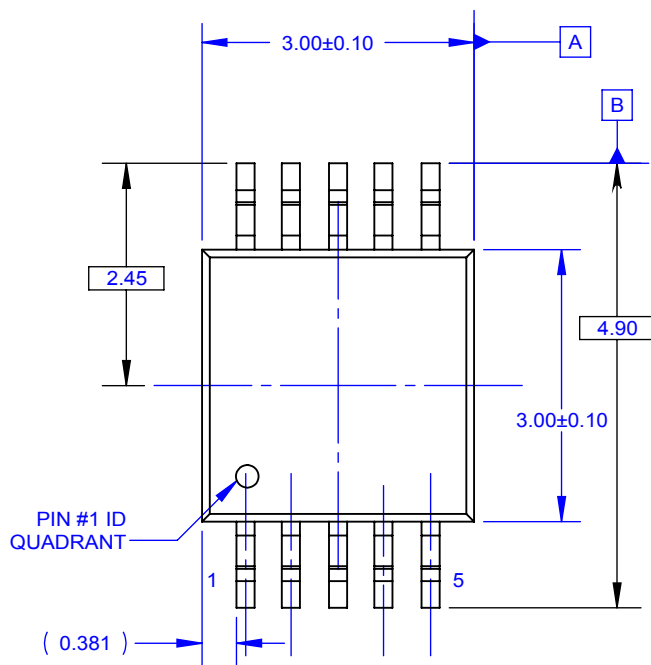
NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.
- E. DRAWING FILENAME: MKT-MAC10Arev6.
- F. DIMENSIONS WITHIN () ARE UNCONTROLLED

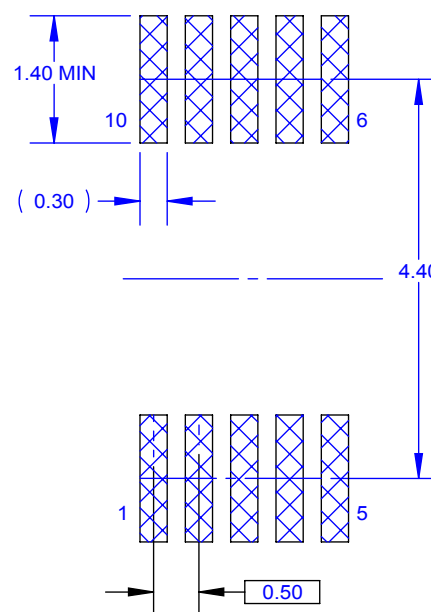


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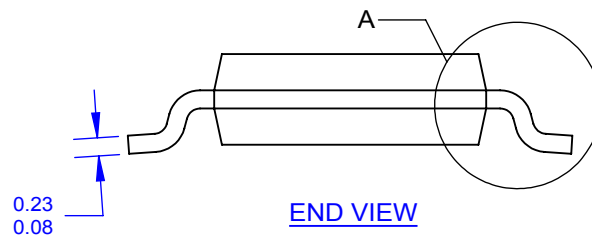
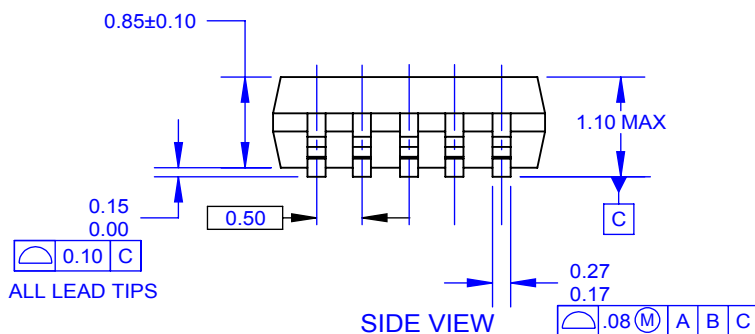
REVISIONS			
NBR	DESCRIPTION	DATE	BY/APP'D
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2	* REMOVE SITE ADDRESS AND CHANGE REVISION TO NUMERICAL & CHANGED LAND PATTERN TO IPC. * CHANGE LEAD WIDTH FROM 0.27MAX TO 0.33MAX. * REMOVE DATE OF JEDEC REVISION	20AUG2009	KHLEE/FSSZ
3	* REVERT LEAD WIDTH TO 0.27MAX.	24SEP2009	KHLEE/FSSZ



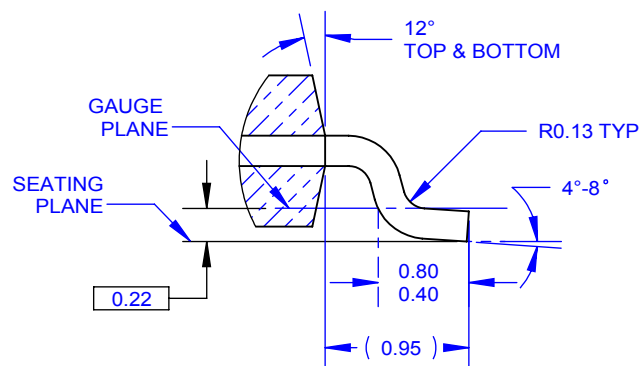
TOP VIEW



LAND PATTERN RECOMMENDATION



END VIEW



DETAIL A
SCALE 20 : 1

NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE CONFORMS TO JEDEC MO-187 VARIATION BA.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-1994.
- E. LAND PATTERN AS PER IPC7351#SOP50P490X110-10AN
- F. FILE NAME: MKT-MUA10AREV3

APPROVALS		DATE		 FAIRCHILD SEMICONDUCTOR™			
DRAWN:	BOBOY MALDO	24SEP09					
CHECKED:	KH LEE						
APPROVED:	BY HUANG						
APPROVED:	HOWARD ALLEN			10LD, MSOP, JEDEC MO-187, 3.0MM WIDE			
PROJECTION				SCALE 1:1	SIZE N/A	DRAWING NUMBER MKT-MUA10A	REVISION 3
[MM] [INCH]				FORMERLY: N/A		SHEET : 1 OF 1	



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ANTI-COUNTERFEITING POLICY

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Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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