

SN65C198, SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051B – JULY 1990 – REVISED JANUARY 1995

- Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Supply Current
- Sleep Mode:
3-State Outputs in High-Impedance State
Ultra-Low Supply Current . . . 17 μ A Typ
- Improved Functional Replacement for:
SN75188,
Motorola MC1488,
National Semiconductor DS14C88, and
DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/ μ s
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . . ± 4.5 V to ± 15 V

description

The SN65C198 and SN75C198 are monolithic low-power BI-MOS quadruple low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN65C198 and SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/ μ s. This feature eliminates the need for external components.

The sleep-mode input, $\overline{SM}$, can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

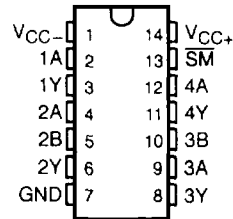
The SN65C198 is characterized for operation from -40°C to 85°C . The SN75C198 is characterized for operation from 0°C to 70°C .

FUNCTION TABLE

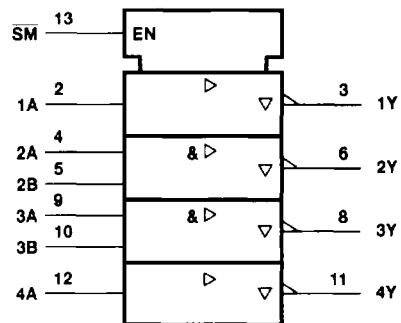
$\overline{SM}$	INPUTS		OUTPUT
	A	B	Y
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance

D OR N PACKAGE
(TOP VIEW)

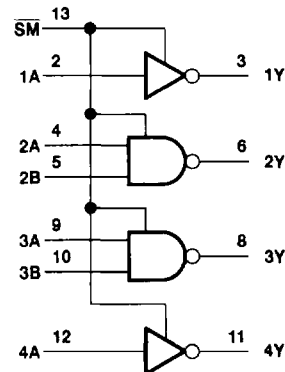


logic symbol



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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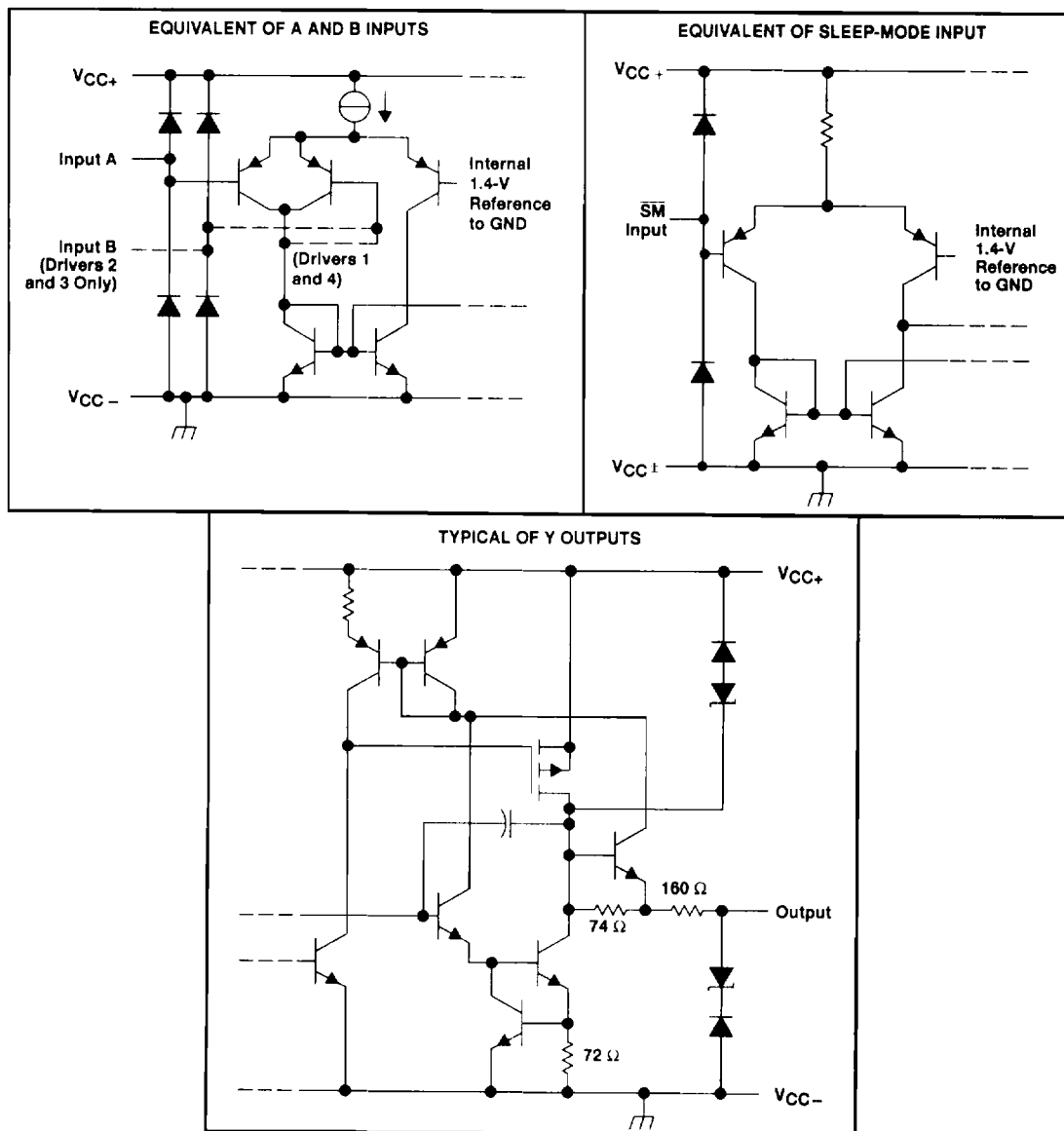
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schematics of inputs and outputs



All resistor values shown are nominal.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1)	15 V
Supply voltage, V_{CC-}	-15 V
Input voltage range, V_I	-15 V to 15 V
Output voltage range, V_O	$V_{CC-} - 6\text{ V}$ to $V_{CC+} + 6\text{ V}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN65C198	-40°C to 85°C
SN75C198	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}		4.5	12	15	V
Supply voltage, V_{CC-}		-4.5	-12	-15	V
Input voltage, V_I (see Figure 2)		$V_{CC-} + 2$		V_{CC+}	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}	A and B inputs			0.8	V
	SM input			0.6	
Operating free-air temperature, T_A	SN65C198	-40		85	°C
	SN75C198	0		70	



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SN65C198, SN75C198

QUADRUPLE LOW-POWER LINE DRIVERS

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electrical characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12$ V, SM at 2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYPT	MAX	UNIT
V_{OH}	High-level output voltage	$V_{IH} = 0.8$ V, $R_L = 3$ k Ω	$V_{CC\pm} = +5$ V		4		V
			$V_{CC\pm} = \pm 12$ V		10		
V_{OL}	Low-level output voltage (see Note 2)	$V_{IH} = 2$ V, $R_L = 3$ k Ω	$V_{CC\pm} = +5$ V			-4	V
			$V_{CC\pm} = \pm 12$ V			-10	
I_{IH}	High-level input current	$V_I = 5$ V				10	μ A
I_{IL}	Low-level input current	$V_I = 0$ V				-10	μ A
I_{OZ}	High-impedance-state output current	$\overline{SM}$ at 0.6 V	$V_O = 12$ V, $V_{CC\pm} = \pm 12$ V			100	μ A
			$V_O = -12$ V, $V_{CC\pm} = \pm 12$ V			-100	
$I_{OS(H)}$	High-level short-circuit output current†	$V_I = 0.8$ V, $V_O = 0$ or V_{CC-}		-4.5	-10	-19.5	mA
$I_{OS(L)}$	Low-level short-circuit output current†	$V_I = 2$ V, $V_O = 0$ or V_{CC+}		4.5	10	19.5	mA
r_o	Output resistance	$V_{CC+} = 0$, $V_O = -2$ V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	A and B inputs at 0.8 V or 2 V, No load	$V_{CC\pm} = \pm 5$ V		90	160	μ A
			$V_{CC\pm} = \pm 12$ V		95	160	
		A and B inputs at 0.8 V or 2 V, $R_L = 3$ k Ω , $\overline{SM}$ at 0.6 V	$V_{CC\pm} = \pm 5$ V		40		
			$V_{CC\pm} = \pm 12$ V		40		
I_{CC-}	Supply current from V_{CC-}	A and B inputs at 0.8 V or 2 V, No load	$V_{CC\pm} = \pm 5$ V		-90	-160	μ A
			$V_{CC\pm} = \pm 12$ V		-95	-160	
		A and B inputs at 0.8 V or 2 V, $R_L = 3$ k Ω , $\overline{SM}$ at 0.6 V	$V_{CC\pm} = \pm 5$ V		-40		
			$V_{CC\pm} = \pm 12$ V		-40		

† All typical values are at $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

switching characteristics over recommended operating free-air temperature range, $V_{CC\pm} = \pm 12$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t _{PLH}	Propagation delay time, low- to high-level output§	R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 1				3	μs
t _{PHL}	Propagation delay time, high- to low-level output§				3.5	μs	
t _{TLH}	Transition time, low- to high-level output†		0.53	1	3.2	μs	
t _{THL}	Transition time, high- to low-level output†		0.53	1	3.2	μs	
t _{TLH}	Transition time, low- to high-level output#	R _L = 3 kΩ to 7 kΩ, C _L = 2500 pF, See Figure 2			1.5		μs
t _{THL}	Transition time, high- to low-level output#				1.5		μs
t _{PZH}	Output enable time to high level	R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 3				50	μs
t _{PHZ}	Output disable time from high level				10	μs	
t _{PZL}	Output enable time to low level	R _L = 3 kΩ to 7 kΩ, C _L = 15 pF, See Figure 4				15	μs
t _{PLZ}	Output disable time from low level				10	μs	
SR	Output slew rate#	R _L = 3 kΩ to 7 kΩ, C _L = 15 pF		6	15	30	V/μs

† All typical values are at $T_A = 25^\circ\text{C}$.

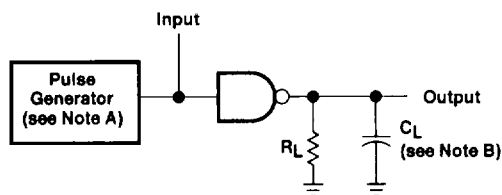
§ t_{PHL} and t_{PLH} include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

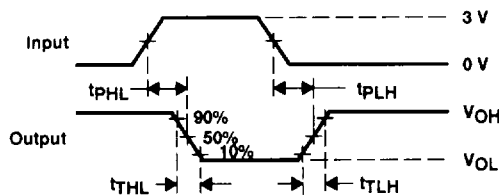
Measured between 3-V and -3-V points of output waveform



PARAMETER MEASUREMENT INFORMATION



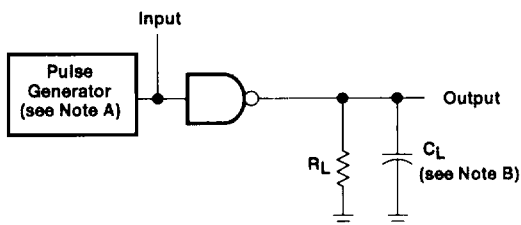
TEST CIRCUIT



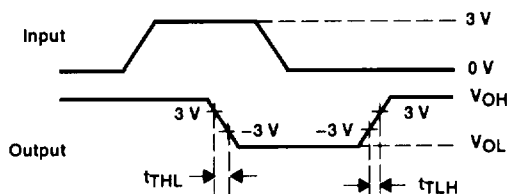
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times



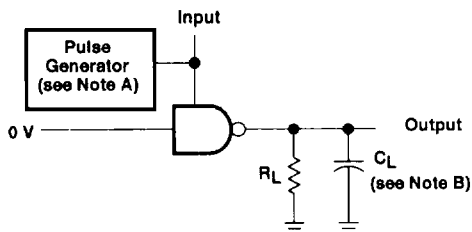
TEST CIRCUIT



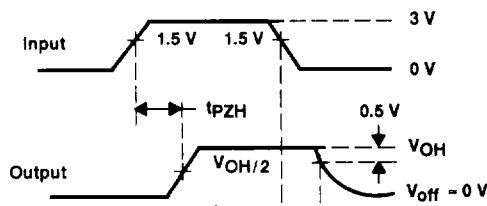
VOLTAGE WAVEFORMS

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B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms, Transition Times



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



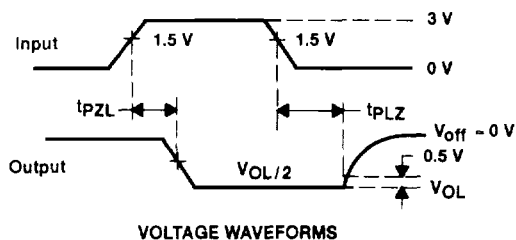
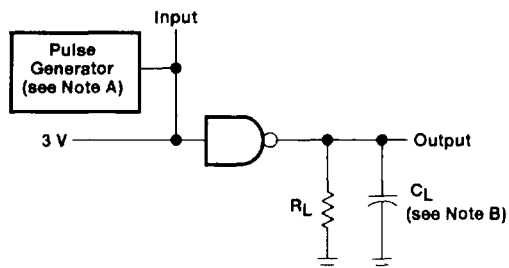
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f \leq 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms



TYPICAL CHARACTERISTICS

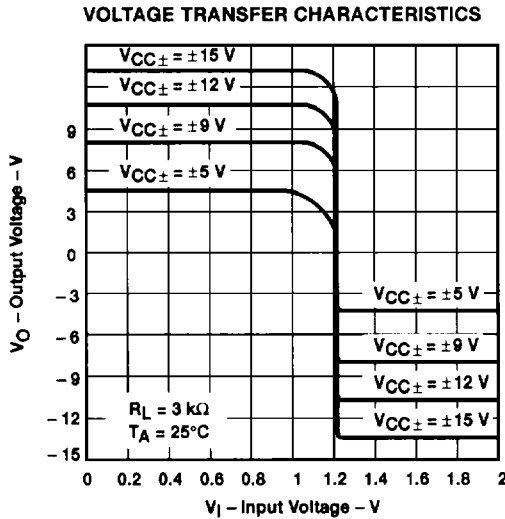


Figure 5

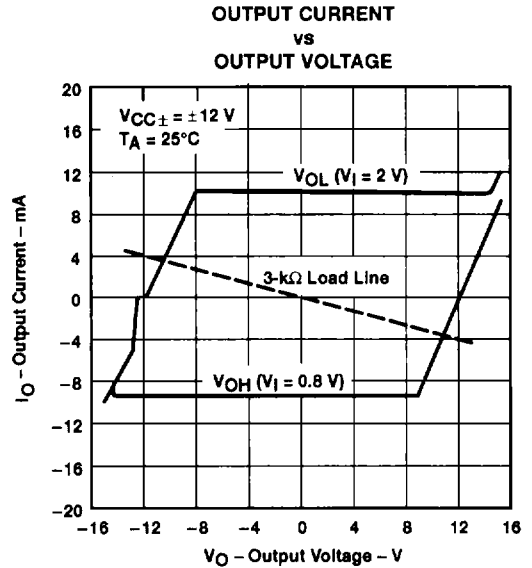


Figure 6

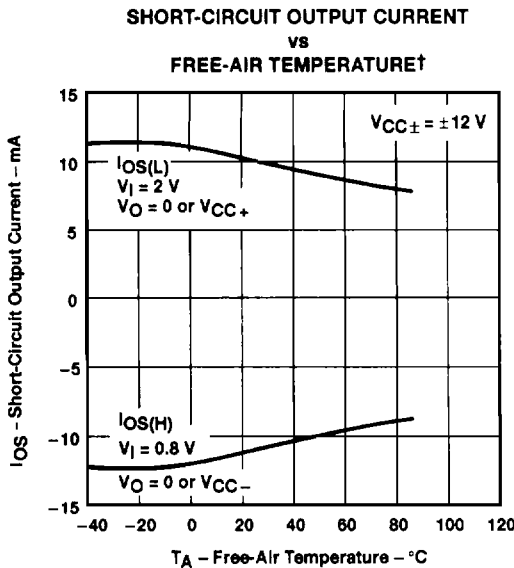


Figure 7

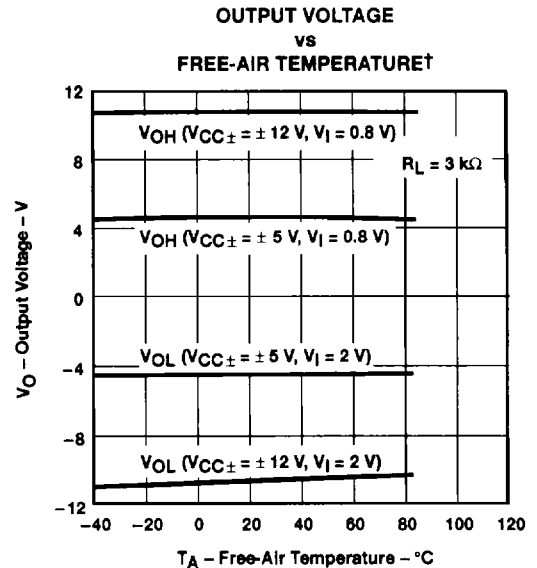


Figure 8

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

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TYPICAL CHARACTERISTICS

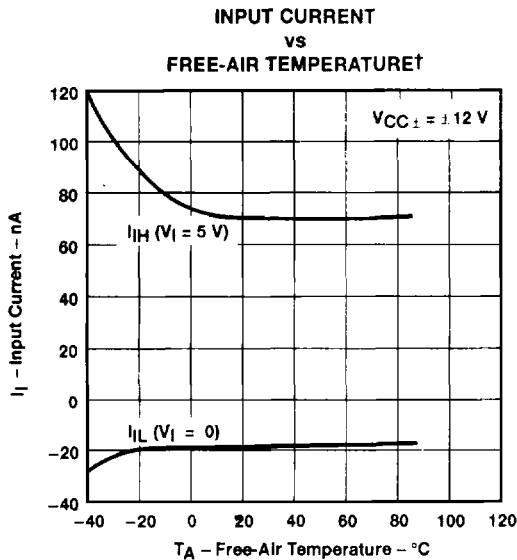


Figure 9

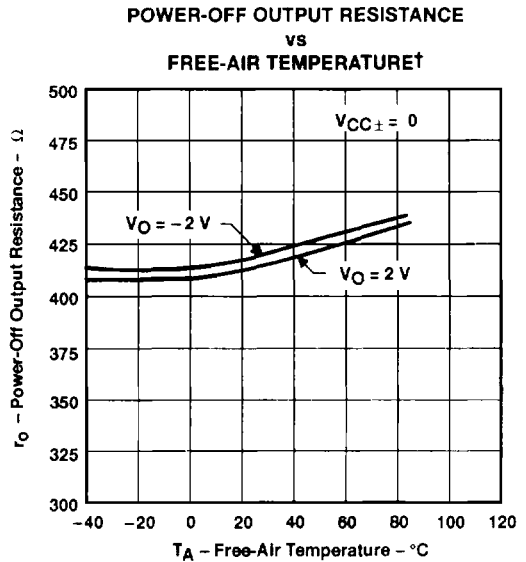


Figure 10

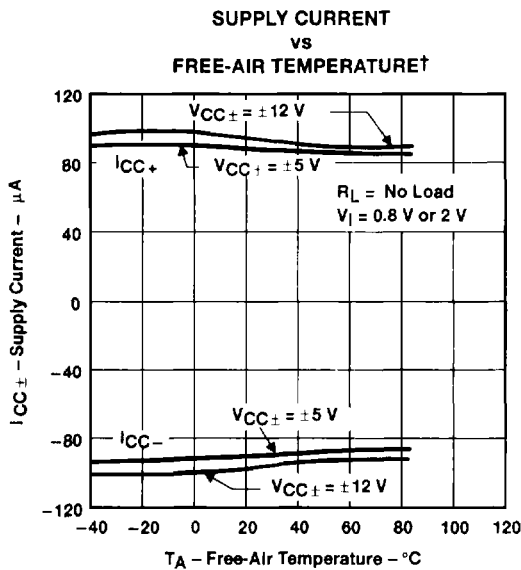


Figure 11

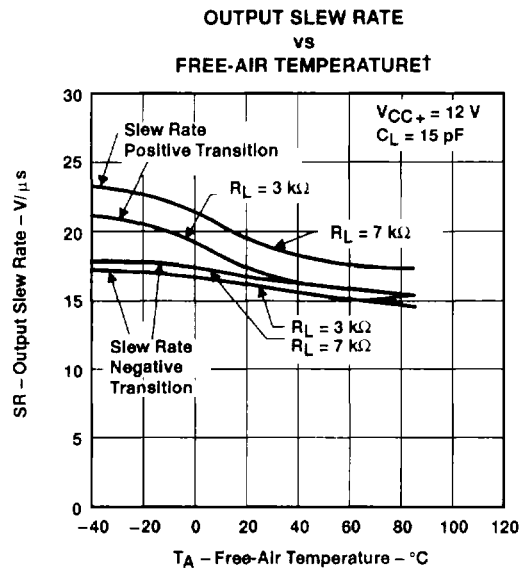


Figure 12

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.



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TYPICAL CHARACTERISTICS

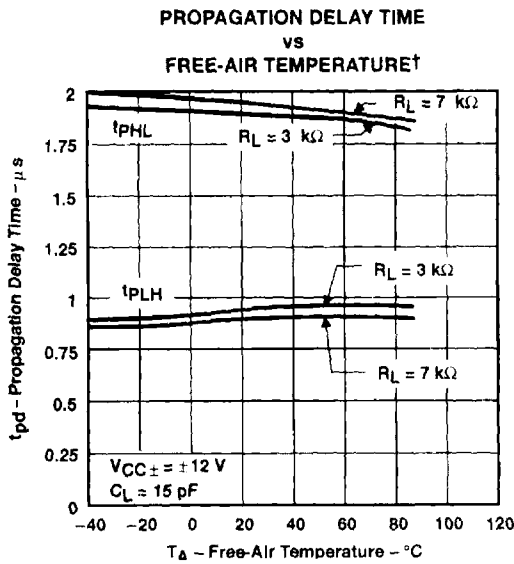


Figure 13

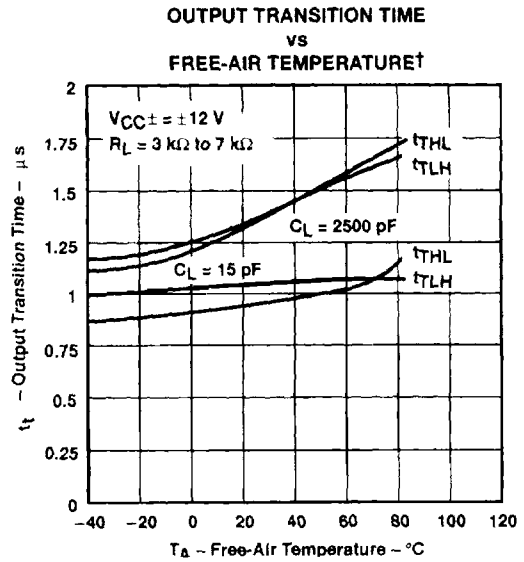


Figure 14

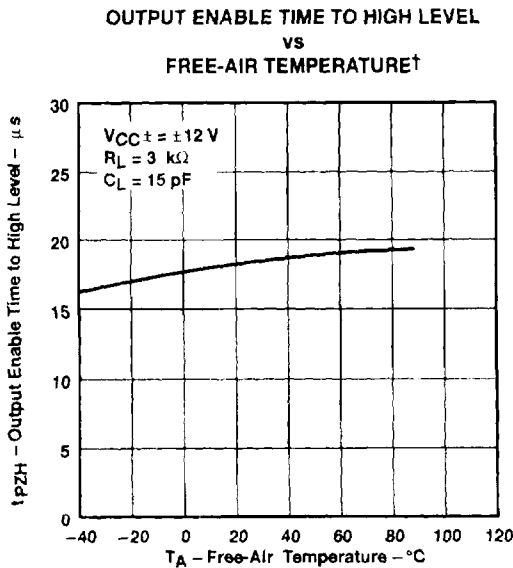


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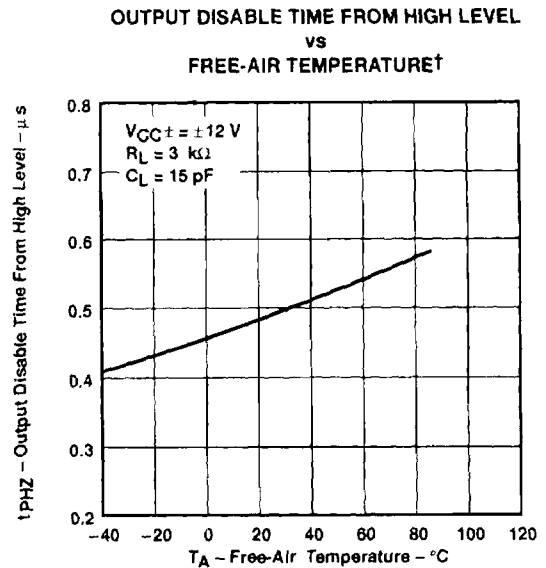


Figure 16

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.

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TYPICAL CHARACTERISTICS

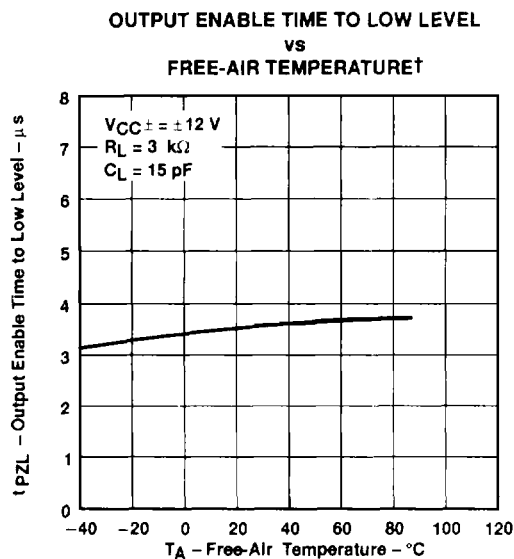


Figure 17

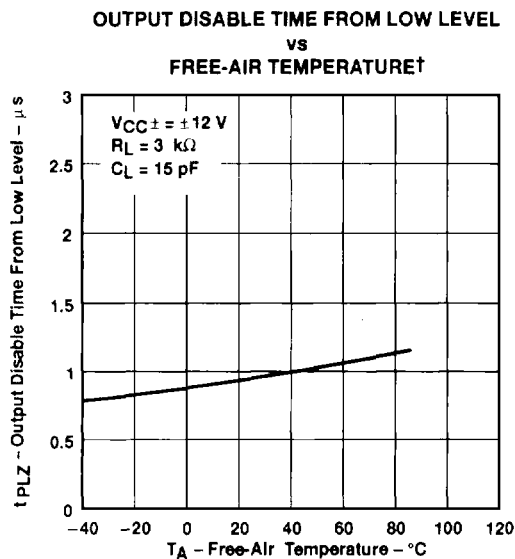


Figure 18

† Only the 0°C to 70°C portion of the curves applies to the SN75C198.



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