CAT5269

Dual Digitally Programmable Potentiometers (DPP™) with 256 Taps and 2-wire Interface

FEATURES

- Two linear taper digitally programmable potentiometers
- 256 resistor taps per potentiometer
- End to end resistance 50kΩ or 100kΩ
- Potentiometer control and memory access via 2-wire interface (I²C like)
- Low wiper resistance, typically 100Ω
- Nonvolatile memory storage for up to four wiper settings for each potentiometer
- Automatic recall of saved wiper settings at power up
- 2.5 to 6.0 volt operation
- Standby current less than 1 μA
- 1,000,000 nonvolatile WRITE cycles
- 100 year nonvolatile memory data retention
- 24-lead SOIC and TSSOP packages
- Industrial temperature range

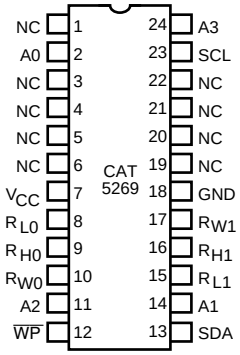
DESCRIPTION

The CAT5269 is two digitally programmable potentiometers (DPPs™) integrated with control logic and 18 bytes of NVRAM memory. Each DPP consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. A separate 8-bit control register (WCR) independently controls the wiper tap switches for each DPP. Associated with each wiper control register are four 8-bit non-volatile memory data registers (DR) used for storing up to four wiper settings. Writing to the wiper control register or any of the non-volatile data registers is via a 2-wire serial bus. On power-up, the contents of the first data register (DR0) for each of the four potentiometers is automatically loaded into its respective wiper control registers.

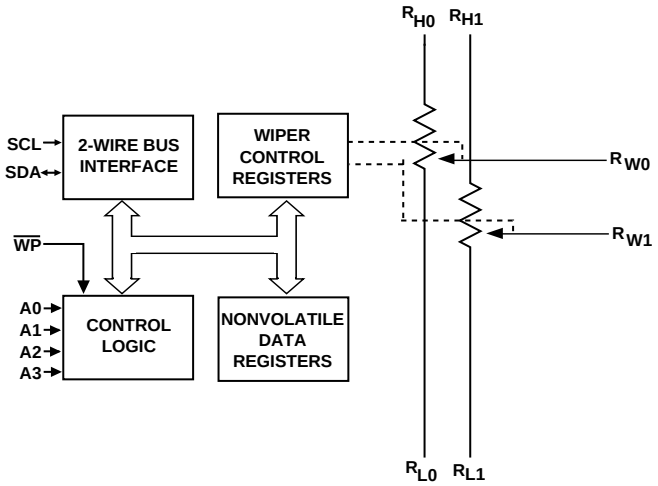
The CAT5269 can be used as a potentiometer or as a two terminal, variable resistor. It is intended for circuit level or system level adjustments in a wide variety of applications. It is available in the -40°C to 85°C industrial operating temperature range and offered in a 24-lead SOIC and TSSOP packages.

PIN CONFIGURATION

SOIC Package (J, W)
TSSOP Package (U, Y)



FUNCTIONAL DIAGRAM



Document No. 2123, Rev. B

PIN DESCRIPTION

Pin (SOIC)	Name	Function
1	NC	No Connect
2	A0	Device Address, LSB
3	NC	No Connect
4	NC	No Connect
5	NC	No Connect
6	NC	No Connect
7	VCC	Supply Voltage
8	R_{L0}	Low Reference Terminal for Potentiometer 0
9	R_{H0}	High Reference Terminal for Potentiometer 0
10	R_{W0}	Wiper Terminal for Potentiometer 0
11	A2	Device Address
12	$\overline{WP}$	Write Protection
13	SDA	Serial Data Input/Output
14	A1	Device Address
15	R_{L1}	Low Reference Terminal for Potentiometer 1
16	R_{H1}	High Reference Terminal for Potentiometer 1
17	R_{W1}	Wiper Terminal for Potentiometer 1
18	GND	Ground
19	NC	No Connect
20	NC	No Connect
21	NC	No Connect
22	NC	No Connect
23	SCL	Bus Serial Clock
24	A3	Device Address

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT5269 serial clock input pin is used to clock all data transfers into or out of the device.

SDA: Serial Data
The CAT5269 bidirectional serial data pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-Ored with the other open drain or open collector I/Os.

A0, A1, A2, A3: Device Address Inputs
These inputs set the device address when addressing multiple devices. A total of sixteen devices can be addressed on a single bus. A match in the slave address must be made with the address input in order to initiate communication with the CAT5269.

R_H, R_L: Resistor End Points
The two sets of R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper
The R_W pins are equivalent to the wiper terminal of a mechanical potentiometer.

$\overline{WP}$: Write Protect Input
The $\overline{WP}$ pin when tied low prevents non-volatile writes to the data registers (change of wiper control register is allowed) and when tied high or left floating normal read/write operations are allowed. See Write Protection on page 7 for more details.

DEVICE OPERATION

The CAT5269 is two resistor arrays integrated with a 2-wire serial interface, two 8-bit wiper control registers and eight 8-bit, non-volatile memory data registers. Each resistor array contains 255 separate resistive elements connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). The tap positions between and at the ends of the series resistors are connected to the output wiper terminals (R_W)by a CMOS transistor switch. Only one tap point for each potentiometer is connected to its wiper terminal at a time and is determined by the value of the wiper control register. Data can be read or written to the wiper control registers or the non-volatile memory data registers via the 2-wire bus. Additional instructions allow data to be transferred between the wiper control registers and each respective potentiometer's non-volatile data registers. Also, the device can be instructed to operate in an "increment/decrement" mode.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to V_{SS} (1)(2) ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Wiper Current ..... ±6mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

Recommended Operating Conditions:

V_{CC} = +2.5V to +6.0V

Temperature	Min	Max
Industrial	-40°C	85°C

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20 ns.
(2) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

POTENTIOMETER CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
R_{POT}	Potentiometer Resistance (100KΩ)		100		kΩ	
R_{POT}	Potentiometer Resistance (50KΩ)		50		kΩ	
	Potentiometer Resistance Tolerance			±20	%	
	R_{POT} Matching			1	%	
	Power Rating			50	mW	25°C, each pot
I_W	Wiper Current			±3	mA	
R_W	Wiper Resistance		200	300	Ω	I_W = ±3mA @ V_{CC} = 3V
R_W	Wiper Resistance		100	150	Ω	I_W = ±3mA @ V_{CC} = 5V
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS}		V_{CC}	V	V_{SS} = 0V
V_N	Noise				nV/√Hz	(1)
	Resolution		0.4		%	
	Absolute Linearity (2)			±1	LSB (4)	$R_{w(n)(actual)}$-$R_{(n)(expected)}$(5)
	Relative Linearity (3)			±0.2	LSB (4)	$R_{w(n+1)}$-[$R_{w(n)+LSB}$](5)
TC_{RPOT}	Temperature Coefficient of R_{POT}		±300		ppm/°C	(1)
TC_{RATIO}	Ratiometric Temp. Coefficient			20	ppm/°C	(1)
$C_H/C_L/C_W$	Potentiometer Capacitances		10/10/25		pF	(1)
fc	Frequency Response		0.4		MHz	R_{POT} = 50KΩ(1)

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) Absolute linearity is utilitzed to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(3) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(4) LSB = R_{TOT} / 255 or (R_H - R_L) / 255, single pot
(5) n = 0, 1, 2, ..., 255

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +6.0V, unless otherwise specified.

Symbol	Parameter	Min	Max	Units	Test Conditions
I_{CC1}	Power Supply Current		1	mA	f_{SCL} = 400 KHz, SDA Open V_{CC} = 6 V, Input = GND
I_{CC2}	Power Supply Current Non-volatile WRITE		5	mA	f_{SCK} = 400 KHz, SDA Open V_{CC} = 6 V, Input = GND
I_{SB}	Standby Current (V_{CC} = 5.0V)		5	µA	V_{IN} = GND or V_{CC}, SDA Open
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-1	V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7	V_{CC} + 1.0	V	
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)		0.4	V	I_{OL} = 3 mA
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)		0.5	V	I_{OL} = 1.5 mA

CAPACITANCE

T_A = 25˚C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance (A0, A1, A2, A3, SCL, $\overline{WP}$)	6	pF	V_{IN} = 0V

A.C. CHARACTERISTICS

		2.5V-6.0V		
Symbol	Parameter	Min.	Max.	Units
f_{SCL}	Clock Frequency		400	kHz
T_I(1)	Noise Suppression Time Constant at SCL, SDA Inputs		200	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out		1	µs
t_{BUF}(1)	Time the bus must be free before a new transmission can start	1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
t_{LOW}	Clock Low Period	1.2		µs
t_{HIGH}	Clock High Period	0.6		µs
$t_{SU:STA}$	Start Condition SetupTime (for a Repeated Start Condition)	0.6		µs
$t_{HD:DAT}$	Data in Hold Time	0		ns
$t_{SU:DAT}$	Data in Setup Time	50		ns
t_R(1)	SDA and SCL Rise Time		0.3	µs
t_F(1)	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	100		ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.

POWER UP TIMING (1)(2)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

XDCP TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	µs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	µs

WRITE CYCLE LIMITS

Symbol	Parameter	Max.	Units
t_{WR}	Write Cycle Time	5	ms

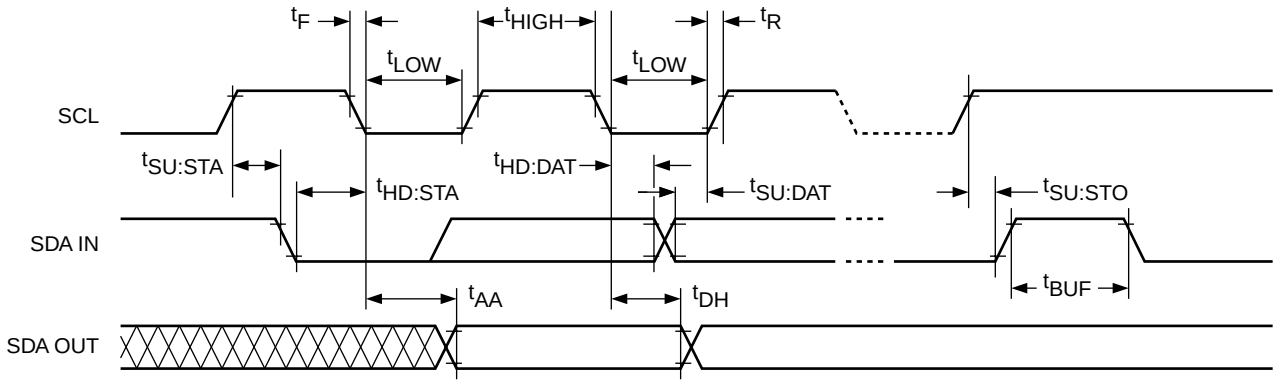
The write cycle is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(1)	Endurance	1,000,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(1)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)	Latch-Up	100		mA	JEDEC Standard 17

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Figure 1. Bus Timing



SERIAL BUS PROTOCOL

The following defines the features of the 2-wire bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.
(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5269 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5269 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 0101 for the CAT5269 (see Figure 5). The next four significant bits (A3, A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to sixteen devices may be individually addressed by the system. Typically, +5V and ground are hard-wired to these pins to establish the device's address.

After the Master sends a START condition and the slave address byte, the CAT5269 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

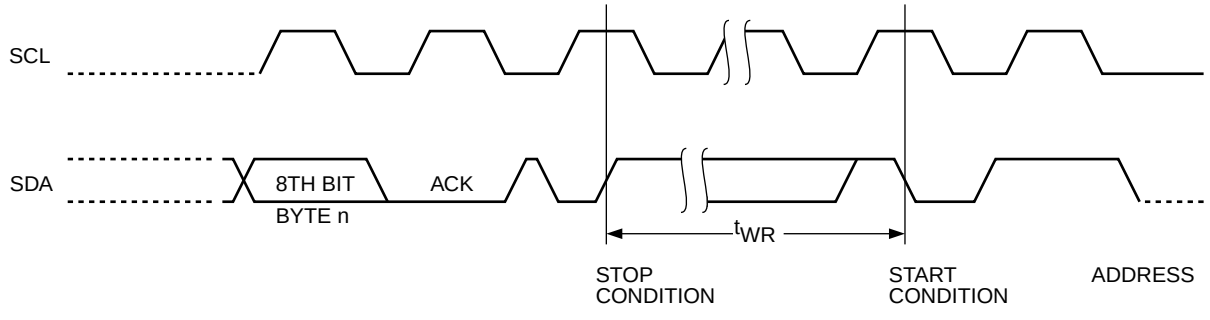
The CAT5269 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5269 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5269 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. After the Slave generates an acknowledge, the Master sends the instruction byte that defines the requested operation of CAT5269. The instruction byte consist of a four-bit opcode followed by two register selection bits and two pot selection bits. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the selected register. The CAT5269 acknowledges once more and the Master generates the STOP condition, at which time if a non-volatile data register is being selected, the device begins an internal programming cycle to non-volatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Figure 2. Write Cycle Timing



Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT5269 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address. If the CAT5269 is still busy with the write operation, no ACK will be returned. If the CAT5269 has completed the write operation, an ACK will be returned and the host can then proceed with the next instruction operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the non-volatile data registers. If the $\overline{WP}$ pin is tied to LOW, the data registers are protected and become read only. Similarly, the $\overline{WP}$ pin going low after start will interrupt a non-volatile write to data registers, while the $\overline{WP}$ pin going low after an internal write cycle has stated will have no effect on any write operation (see also CAT5409 or CAT5259). The CAT5269 will accept both slave addresses and instructions, but the data registers are protected from programming by the device's failure to send an acknowledge after data is received.

Figure 3. Start/Stop Condition

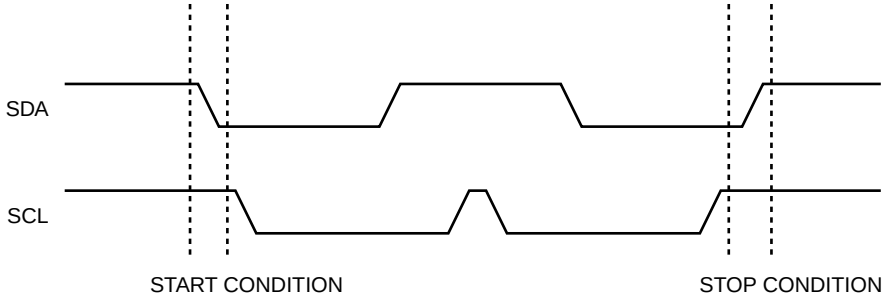


Figure 4. Acknowledge Condition

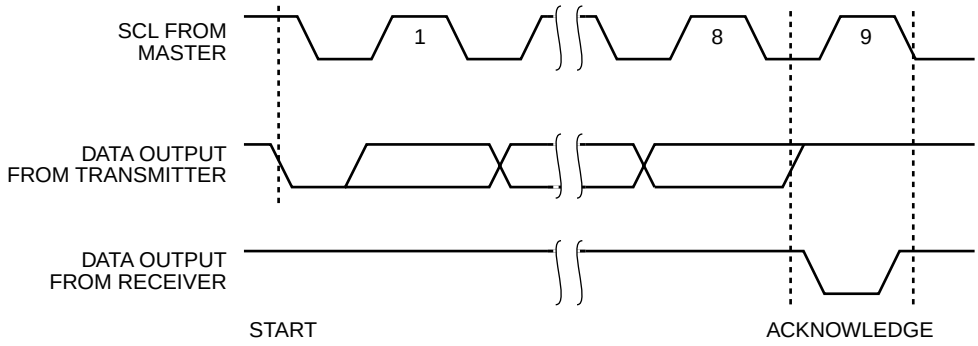


Figure 5. Slave Address Bits

CAT5269	0	1	0	1	A3	A2	A1	A0

* A0, A1, A2 and A3 correspond to pin A0, A1, A2 and A3 of the device.
** A0, A1, A2 and A3 must compare to its corresponding hard wired input pins.

INSTRUCTION AND REGISTER DESCRIPTION

SLAVE ADDRESS BYTE

The first byte sent to the CAT5269 from the master/ processor is called the Slave/DPP Address Byte. The most significant four bits of the slave address are a device type identifier. These bits for the CAT5269 are fixed at 0101[B] (refer to Table 1).

The next four bits, A3 - A0, are the internal slave address and must match the physical device address which is defined by the state of the A3 - A0 input pins for the CAT5269 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3 - A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

INSTRUCTION BYTE

The next byte sent to the CAT5269 contains the instruction and register pointer information. The four most significant bits used provide the instruction opcode I3 - I0. The R1 and R0 bits point to one of the four data registers of each associated potentiometer. The least two significant bits point to one of two Wiper Control Registers. The format is shown in Table 2.

Data Register Selection

Data Register Selected	R1	R0
DR0	0	0
DR1	0	1

Figure 6. Write Timing

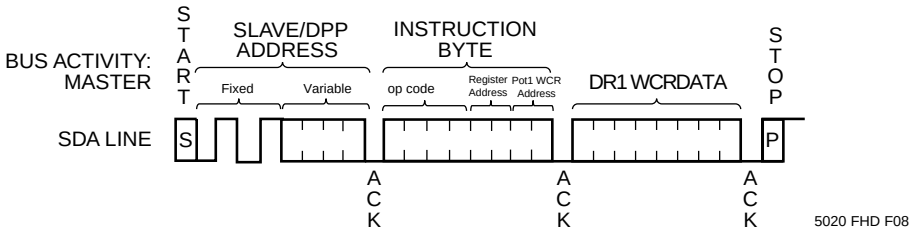


Table 1. Identification Byte Format

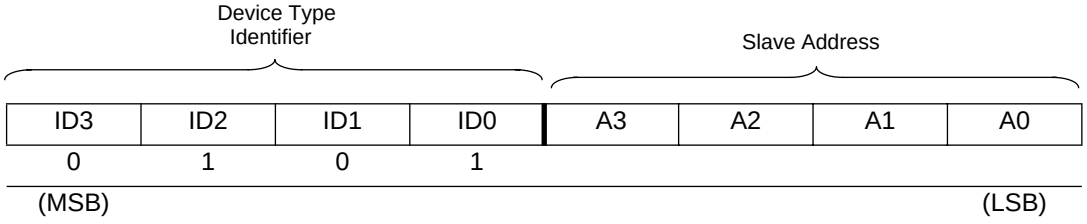
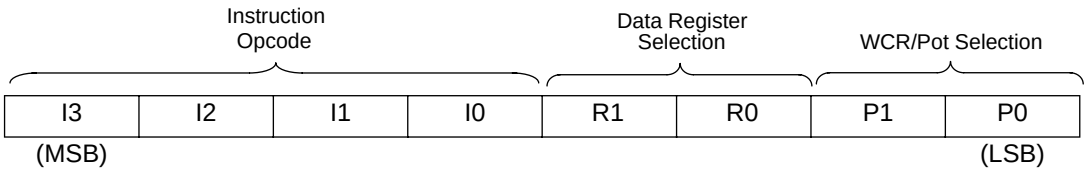


Table 2. Instruction Byte Format



WIPER CONTROL AND DATA REGISTERS

Wiper Control Register (WCR)

The CAT5269 contains two 8-bit Wiper Control Registers, one for each potentiometer. The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written by the host via Write Wiper Control Register instruction; it may be written by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction, it can be modified one step at a time by the Increment/decrement instruction (see Instruction section for more details). Finally, it is loaded with the content of its data register zero (DR0) upon power-up.

The Wiper Control Register is a volatile register that loses its contents when the CAT5269 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down.

Data Registers (DR)

Each potentiometer has four 8-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Control Register. Any data changes in one of the Data Registers is a non-volatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as standard memory locations for system parameters or user preference data.

INSTRUCTIONS

Four of the nine instructions are three bytes in length. These instructions are:

— **Read Wiper Control Register** - read the current wiper position of the selected potentiometer in the WCR

— **Write Wiper Control Register** - change current wiper position in the WCR of the selected potentiometer

— **Read Data Register** - read the contents of the selected Data Register

— **Write Data Register** - write a new value to the selected Data Register

The basic sequence of the three byte instructions is illustrated in Figure 8. These three-byte instructions

Table 3. Instruction Set

Instruction	Instruction Set								Operation
	I3	I2	I1	I0	R1	R0	WCR1/ P1	WCR0/ P0	
Read Wiper Control Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Control Register pointed to by P1-P0
Write Wiper Control Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Control Register pointed to by P1-P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1-P0 and R1-R0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1-P0 and R1-R0
XFR Data Register to Wiper Control Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1-P0 and R1-R0 to its associated Wiper Control Register
XFR Wiper Control Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Control Register pointed to by P1-P0 to the Data Register pointed to by R1-R0
Gang XFR Data Registers to Wiper Control Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by R1-R0 of both pots to their respective Wiper Control Registers
Gang XFR Wiper Control Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Control Registers to their respective data Registers pointed to by R1-R0 of both pots
Increment/Decrement Wiper Control Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1-P0

Note: 1/0 = data is one or zero

exchange data between the WCR and one of the Data Registers. The WCR controls the position of the wiper. The response of the wiper to this action will be delayed by t_{WR}. A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the two potentiometers and one of its associated registers; or the transfer can occur between both potentiometers and one associated register.

Four instructions require a two-byte sequence to complete, as illustrated in Figure 7. These instructions transfer data between the host/processor and the CAT5269; either between the host and one of the data registers or directly between the host and the Wiper Control Register. These instructions are:

— **XFR Data Register to Wiper Control Register**
This transfers the contents of one specified Data Register to the associated Wiper Control Register.

— **XFR Wiper Control Register to Data Register**
This transfers the contents of the specified Wiper Control Register to the specified associated Data Register.

— **Gang XFR Data Register to Wiper Control Register**
This transfers the contents of all specified Data Registers to the associated Wiper Control Registers.

— **Gang XFR Wiper Counter Register to Data Register**
This transfers the contents of all Wiper Control Registers to the specified associated Data Registers.

INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (Figure 9 and 10). The Increment/Decrement command is different from the other commands. Once the command is issued and the CAT5269 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal.

See Instructions format for more detail.

Figure 7. Two-Byte Instruction Sequence

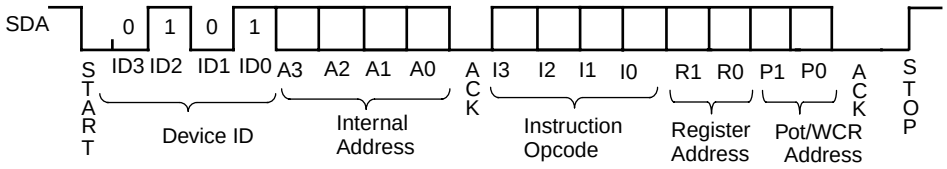


Figure 8. Three-Byte Instruction Sequence

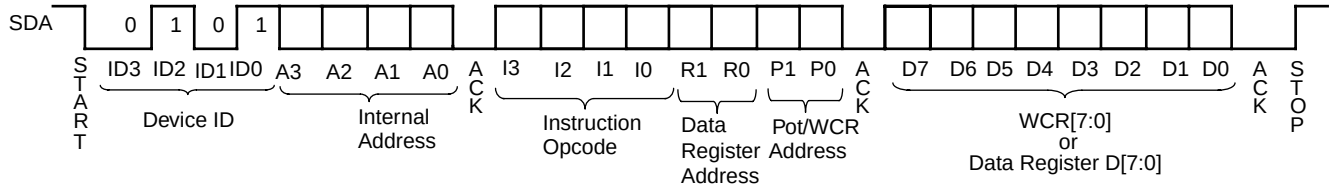


Figure 9. Increment/Decrement Instruction Sequence

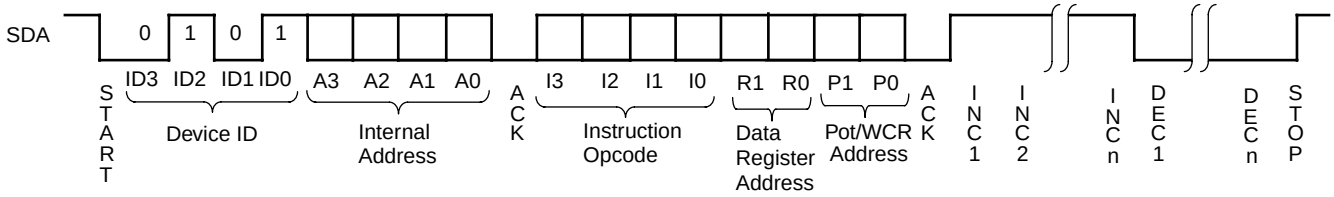
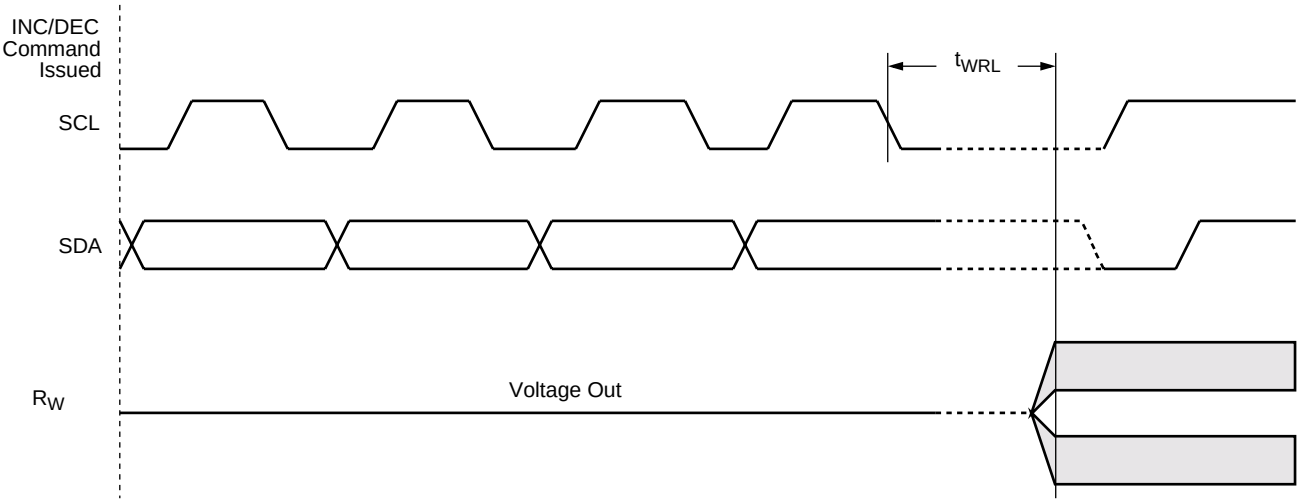


Figure 10. Increment/Decrement Timing Limits



INSTRUCTION FORMAT

Read Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A	A	A	A	C	1	0	0	1	0	0	P	P	C	7	6	5	4	3	2	1	0	C	T
A					3	2	1	0	K							1	0	K									K	O
R																												P
T																												

Write Wiper Control Register (WCR)

S	DEVICE ADDRESS								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A	A	A	A	C	1	0	1	0	0	0	P	P	C	7	6	5	4	3	2	1	0	C	T
A					3	2	1	0	K							1	0	K									K	O
R																												P
T																												

Read Data Register (DR)

S	DEVICE ADDRESS								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A	A	A	A	C	1	0	1	1	R	R	P	P	C	7	6	5	4	3	2	1	0	C	T
A					3	2	1	0	K					1	0	1	0	K									K	O
R																												P
T																												

Write Data Register (DR)

S	DEVICE ADDRESS								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A	A	A	A	C	1	1	0	0	R	R	P	P	C	7	6	5	4	3	2	1	0	C	T
A					3	2	1	0	K					1	0	1	0	K									K	O
R																												P
T																												

INSTRUCTION FORMAT (continued)

Gang Transfer Data Register (DR) to Wiper Control Register (WCR)

START	DEVICE ADDRESS								ACK	INSTRUCTION								ACK	STOP
	0	1	0	1	A3	A2	A1	A0		0	0	0	1	R1	R0	0	0		

Gang Transfer Wiper Control Register (WCR) to Data Register (DR)

START	DEVICE ADDRESS								ACK	INSTRUCTION								ACK	STOP
	0	1	0	1	A3	A2	A1	A0		1	0	0	0	R1	R0	0	0		

Transfer Wiper Control Register (WCR) to Data Register (DR)

START	DEVICE ADDRESS								ACK	INSTRUCTION								ACK	STOP
	0	1	0	1	A3	A2	A1	A0		1	1	1	0	R1	R0	P1	P0		

Transfer Data Register (DR) to Wiper Control Register (WCR)

START	DEVICE ADDRESS								ACK	INSTRUCTION								ACK	STOP
	0	1	0	1	A3	A2	A1	A0		1	1	0	1	R1	R0	P1	P0		

Increment (I)/Decrement (D) Wiper Control Register (WCR)

START	DEVICE ADDRESS								ACK	INSTRUCTION								ACK	DATA					ACK	STOP
	0	1	0	1	A3	A2	A1	A0		0	0	1	0	0	0	P1	P0		I/D	I/D	• • •	I/D	I/D		

Notes:
(1) Any write or transfer to the Non-volatile Data Registers is followed by a high voltage cycle after a STOP has been issued.

ORDERING INFORMATION

Prefix	Device #	Suffix

CAT — **Optional Company ID**

5269 — **Product Number**

J — **Package**
J: SOIC
U: TSSOP
W: SOIC (Lead free, Halogen free)
Y: TSSOP (Lead free, Halogen free)

I — **Temperature Range**
I = Industrial (-40˚C to 85˚C)

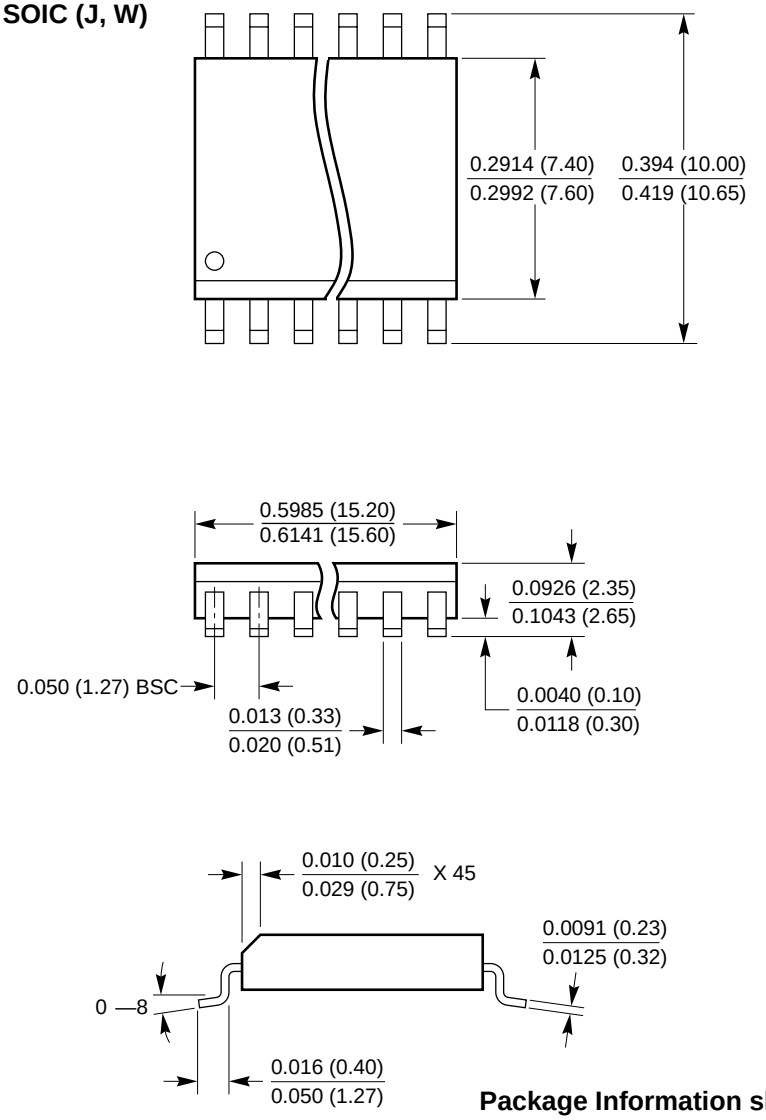
-00 — **Resistance**
-50: 50K Ohms
-00: 100K Ohms

-TE13 — **Tape & Reel**
TE13: 2000/Reel

Notes:
(1) The device used in the above example is a CAT5269JI00-TE13 (SOIC, Industrial Temperature, 100K Ohm, Tape & Reel)

PACKAGING INFORMATION

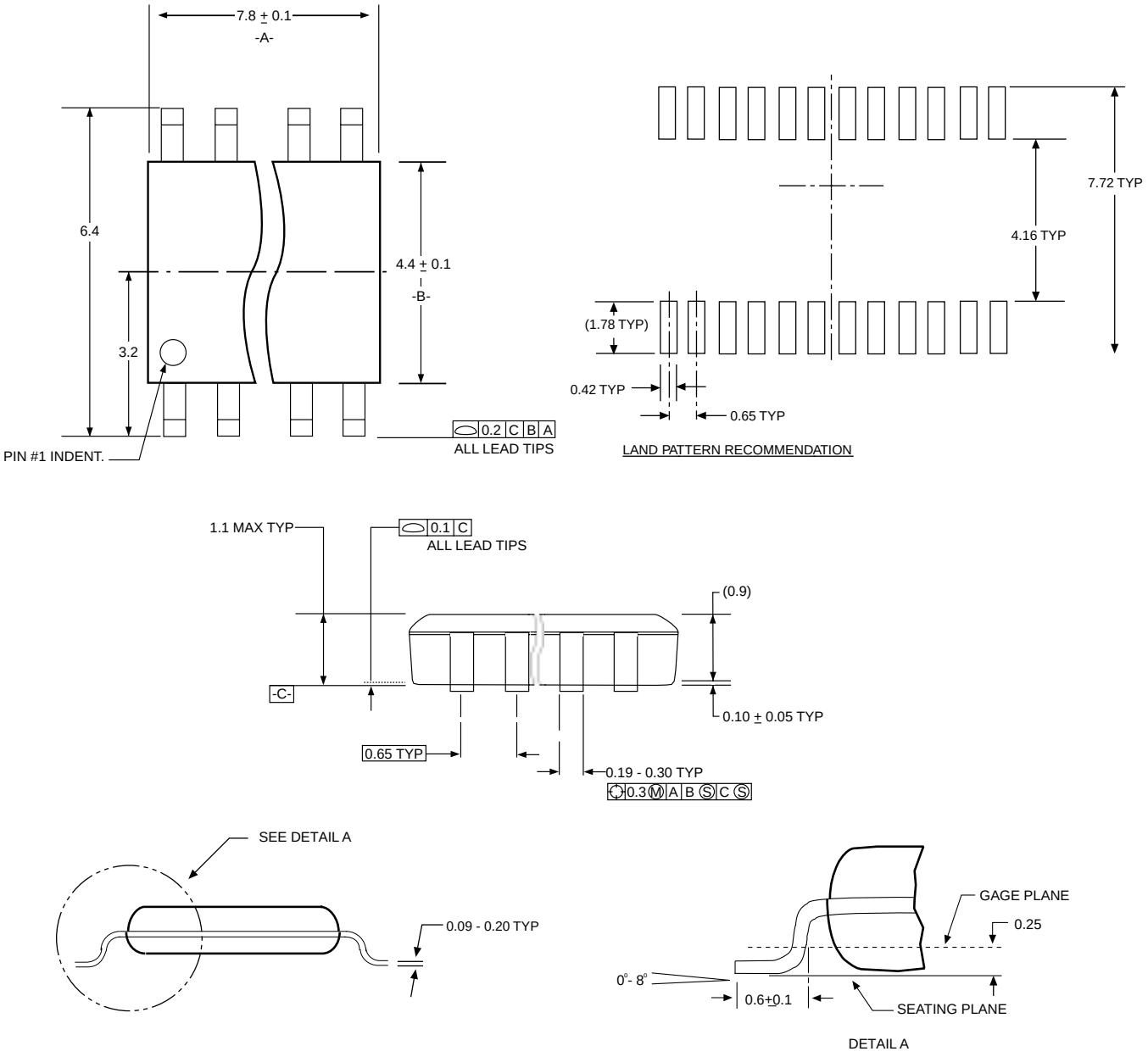
24-LEAD 300 MIL WIDE SOIC (J, W)



Package Information shown in inches (mm).

PACKAGING INFORMATION CON'T

24 Lead TSSOP (U)



Package Information shown in mm.

REVISION HISTORY

Date	Rev.	Reason
11/18/2003	A	Initial issue
5/6/2004	B	Added TSSOP package in all areas Updated Functional Diagram Updated Pin Descriptions Updated notes in Absolute Max Ratings Updated Potentiometer Characteristics table Updated DC Characteristics table Added XDCP Timing table Updated Write Cycle LImits table Changed Figure 3 drawing to Start/Stop Condition from Start/Stop Timing Changed Figure 4 title to Acknowlege Condition (from Acknowlege Timing) Updated Table 3 Gang XFR Operation information Corrected Instruction Format for Gang Transfer Data Register (DR) to Wiper Control Register (WCR)

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