

RL78/G13A

R01DS0376EJ0110

RENESAS MCU

Rev.1.10

Sep 18, 2020

RL78/G13A microcontrollers share the functionality of RL78/G13 products but have a much (over 40%) lower operating current of 47 $\mu\text{A}/\text{MHz}$ (typ.). Operation is guaranteed at ambient temperatures up to 105°C while this is not the case for RL78/G13 products with 384 or 512 Kbytes of code flash memory. RL78/G13A microcontrollers can be used in a wide variety of applications, from home and consumer appliances to industrial equipment.

1. OUTLINE

1.1 Features

Ultra-low power consumption technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μs : @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μs : @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register $\times$ 8) $\times$ 4 banks
- On-chip RAM: 24 or 32 KB

Code flash memory

- Code flash memory: 384 or 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: $\pm 1.0\%$ (V_{DD} = 1.6 to 5.5 V, T_A = -40 to +85°C)

Operating ambient temperature

- T_A = -40 to +85°C (A: Consumer applications)
- T_A = -40 to +105°C (G: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

DMA (Direct Memory Access) controller

- 2/4 channels
- Number of clocks during transfer between 8/16-bit SFR and internal RAM: 2 clocks

Multiplier and divider/multiply-accumulator

- 16 bits $\times$ 16 bits = 32 bits (Unsigned or signed)
- 32 bits $\div$ 32 bits = 32 bits (Unsigned)
- 16 bits $\times$ 16 bits + 32 bits = 32 bits (Unsigned or signed)

Serial interface

- CSI: 4 to 8 channels
- UART/UART (LIN-bus supported): 3 or 4 channels
- I²C/Simplified I²C communication: 5 to 10 channels

Timer

- 16-bit timer: 8 or 12 channels
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 10 to 20 channels
- Internal reference voltage (1.45 V) and temperature sensor ^{Note 1}

I/O port

- I/O port: 40 to 92 (N-ch open drain I/O [withstand voltage of 6 V]: 4, N-ch open drain I/O [V_{DD} withstand voltage ^{Note 2}/ EV_{DD} withstand voltage ^{Note 3}: 10 to 24)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

- Notes**
- Can be selected only in HS (high-speed main) mode
 - 44- and 48-pin products
 - 64- and 100-pin products

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

O ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G13A			
			44 pins	48 pins	64 pins	100 pins
512 KB	8 KB	32 KB ^{Note}	R5F140FL	R5F140GL	R5F140LL	R5F140PL
384 KB	8 KB	24 KB	R5F140FK	R5F140GK	R5F140LK	R5F140PK

Note The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F140xL (x = F, G, L, P): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13A

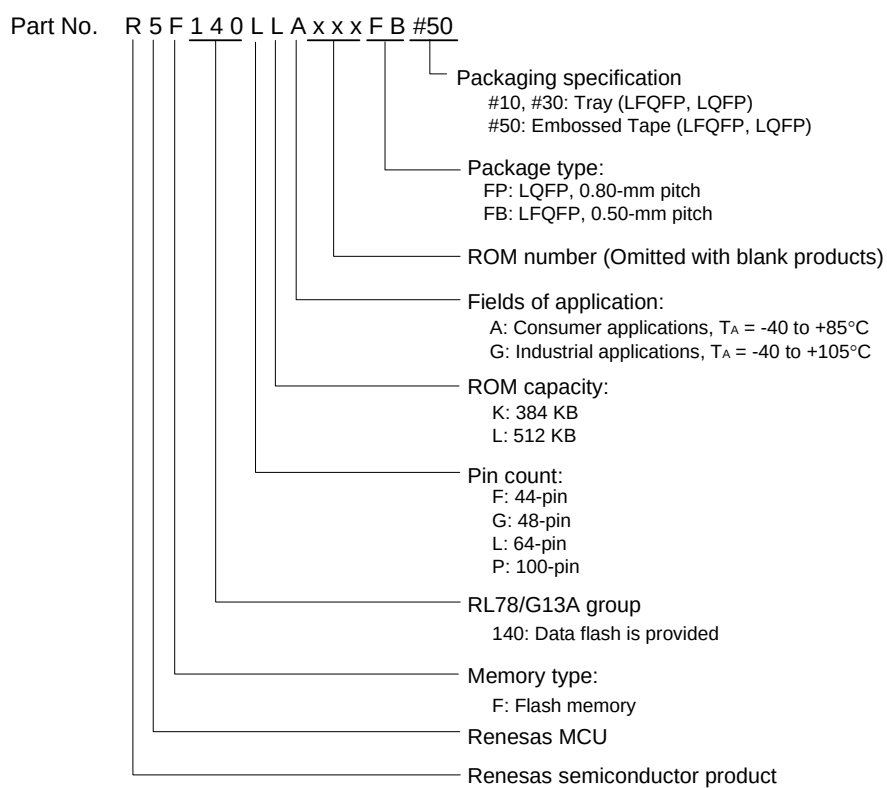


Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application ^{Note}	Ordering Part Number
44 pins	44-pin plastic LQFP (10 x 10 mm, 0.8-mm pitch)	Mounted	A G	R5F140FKAFP#10, R5F140FLAFP#10 R5F140FKAFP#30, R5F140FLAFP#30 R5F140FKAFP#50, R5F140FLAFP#50 R5F140FKGFP#10, R5F140FLGFP#10 R5F140FKGFP#30, R5F140FLGFP#30 R5F140FKGFP#50, R5F140FLGFP#50
48 pins	48-pin plastic LFQFP (7 x 7 mm, 0.5-mm pitch)	Mounted	A G	R5F140GKAFB#10, R5F140GLAFB#10 R5F140GKAFB#30, R5F140GLAFB#30 R5F140GKAFB#50, R5F140GLAFB#50 R5F140GKGFB#10, R5F140GLGFB#10 R5F140GKGFB#30, R5F140GLGFB#30 R5F140GKGFB#50, R5F140GLGFB#50
64 pins	64-pin plastic LFQFP (10 x 10 mm, 0.5-mm pitch)	Mounted	A G	R5F140LKAFB#10, R5F140LLAFB#10 R5F140LKAFB#30, R5F140LLAFB#30 R5F140LKAFB#50, R5F140LLAFB#50 R5F140LKGFB#10, R5F140LLGFB#10 R5F140LKGFB#30, R5F140LLGFB#30 R5F140LKGFB#50, R5F140LLGFB#50
100 pins	100-pin plastic LFQFP (14 x 14 mm, 0.5-mm pitch)	Mounted	A G	R5F140PKAFB#10, R5F140PLAFB#10 R5F140PKAFB#30, R5F140PLAFB#30 R5F140PKAFB#50, R5F140PLAFB#50 R5F140PKGFB#10, R5F140PLGFB#10 R5F140PKGFB#30, R5F140PLGFB#30 R5F140PKGFB#50, R5F140PLGFB#50

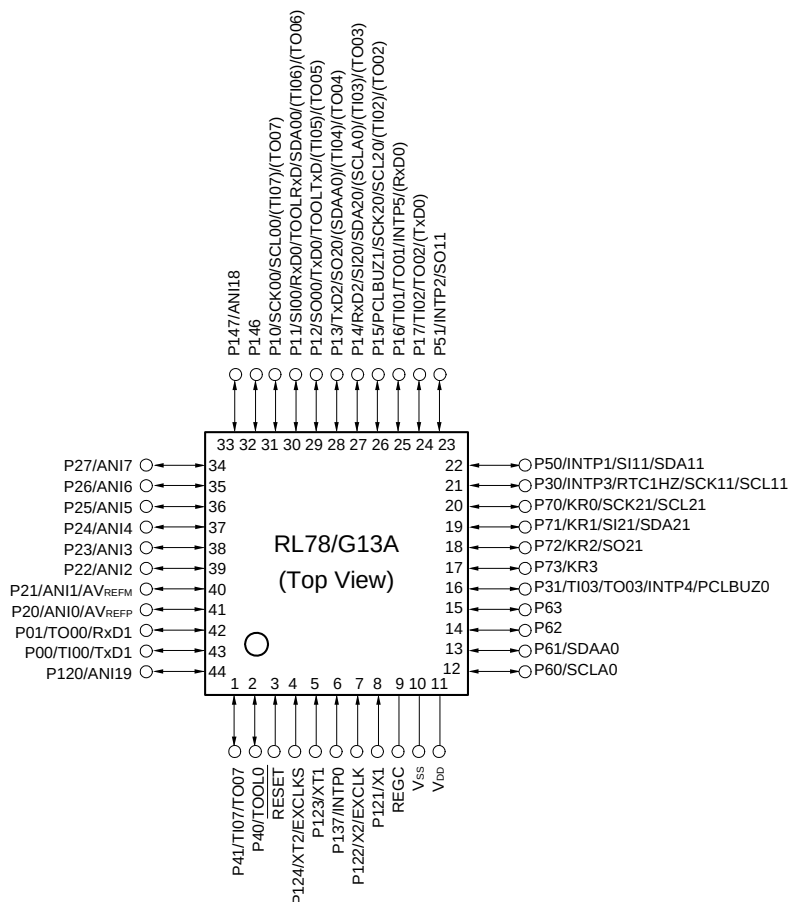
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13A**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8-mm pitch)



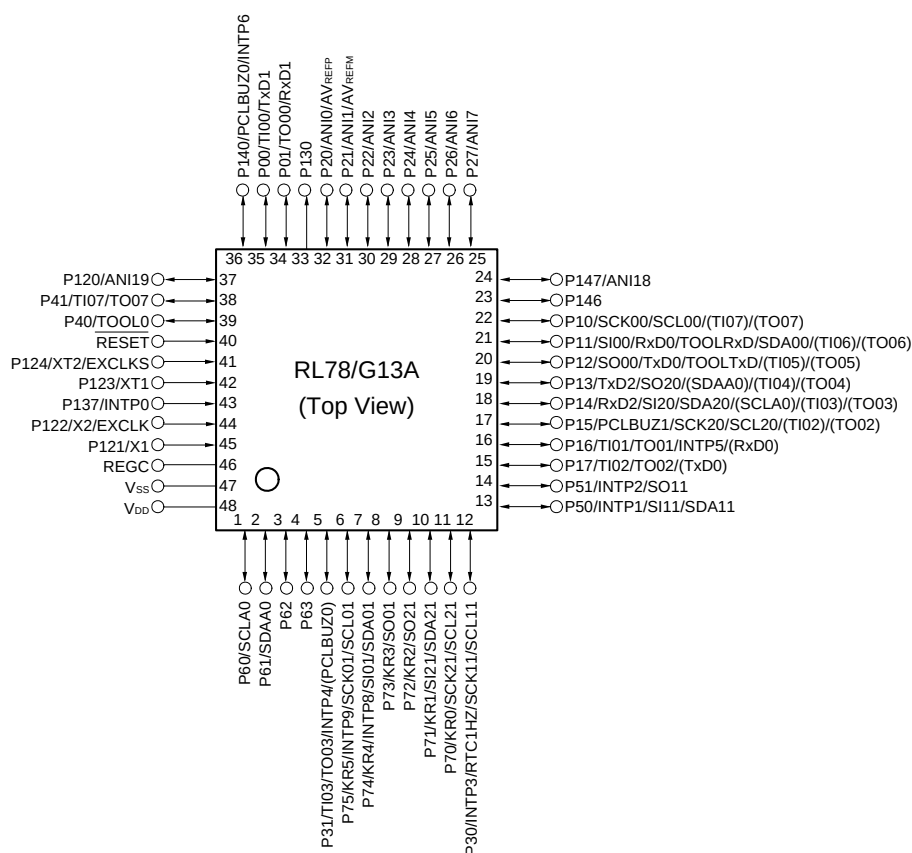
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.3.2 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5-mm pitch)



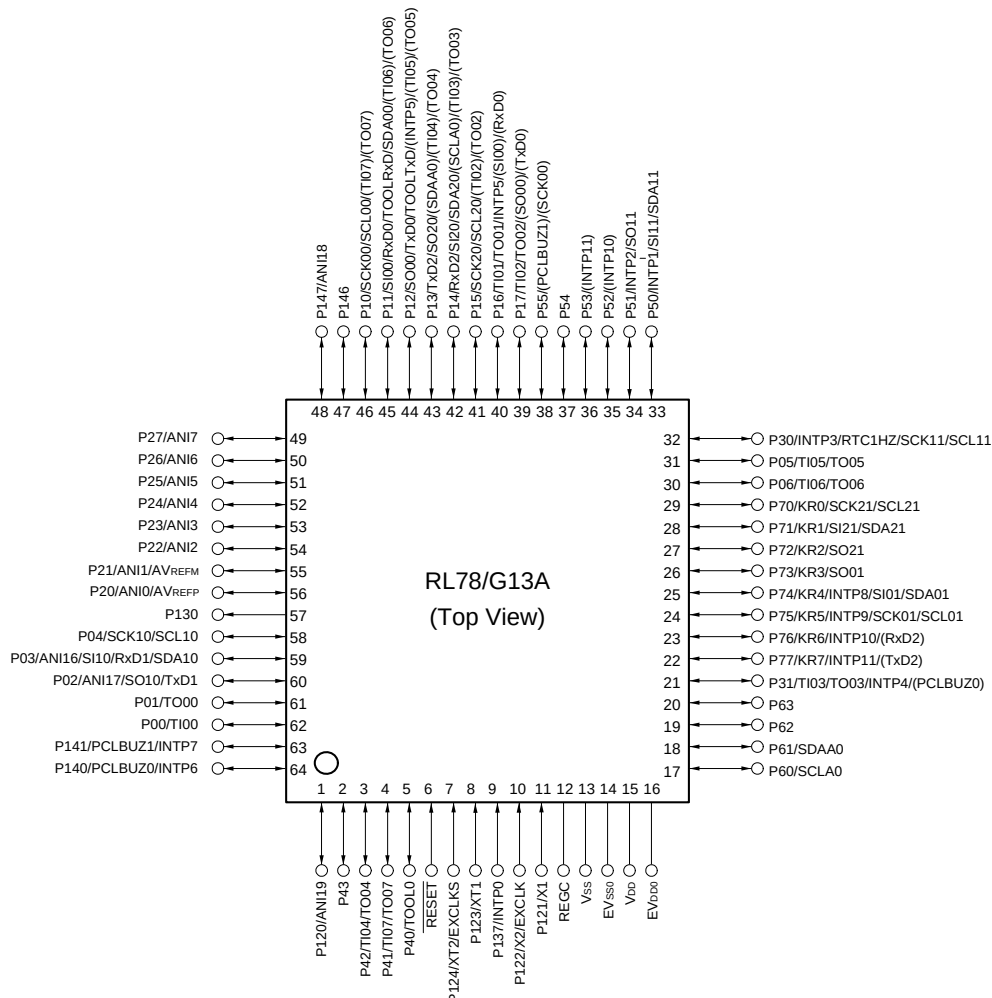
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.3.3 64-pin products

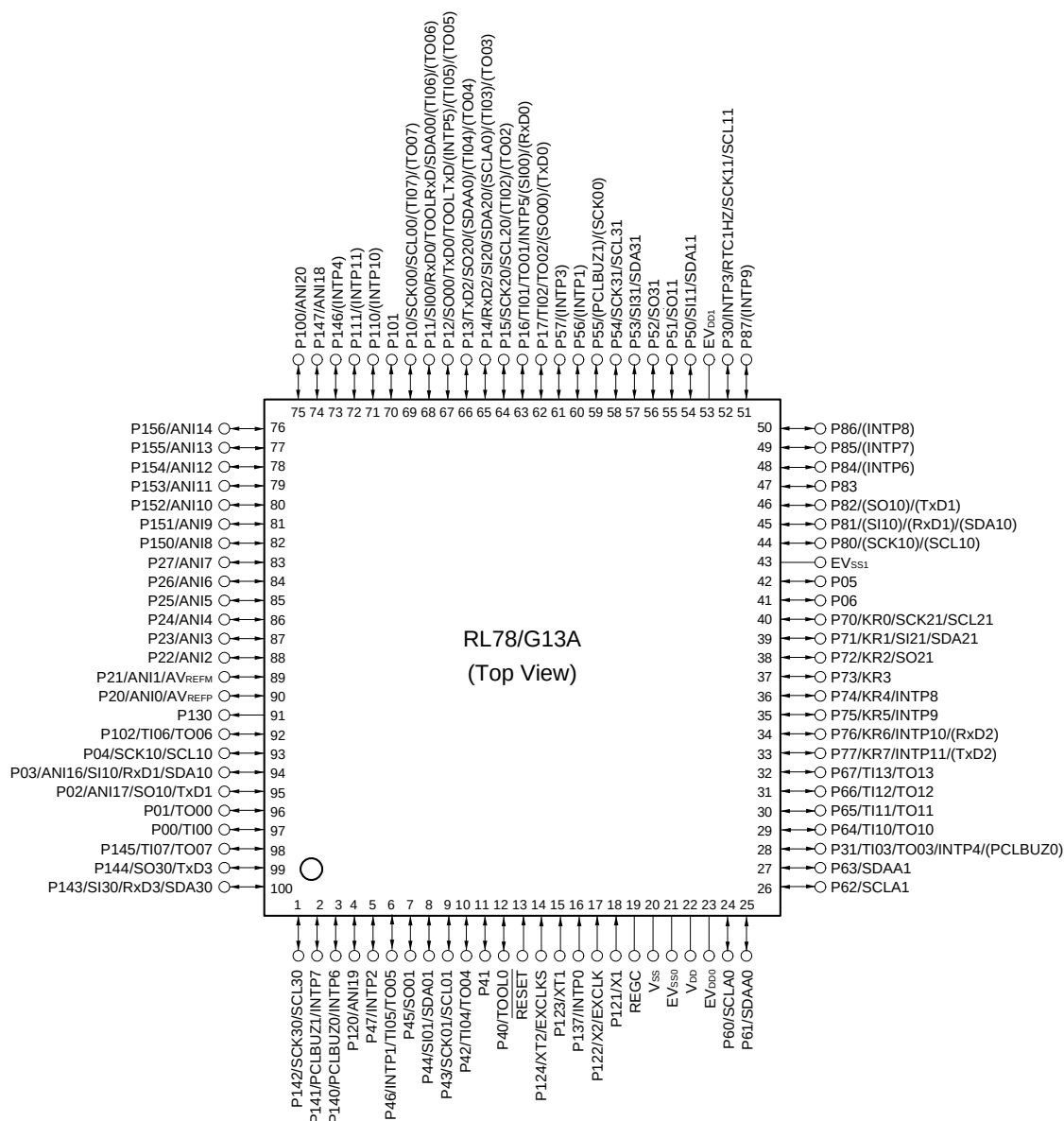
- 64-pin plastic LFQFP (10 × 10 mm, 0.5-mm pitch)



- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is no less than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

- 100-pin plastic LFQFP (14 × 14 mm, 0.5-mm pitch)



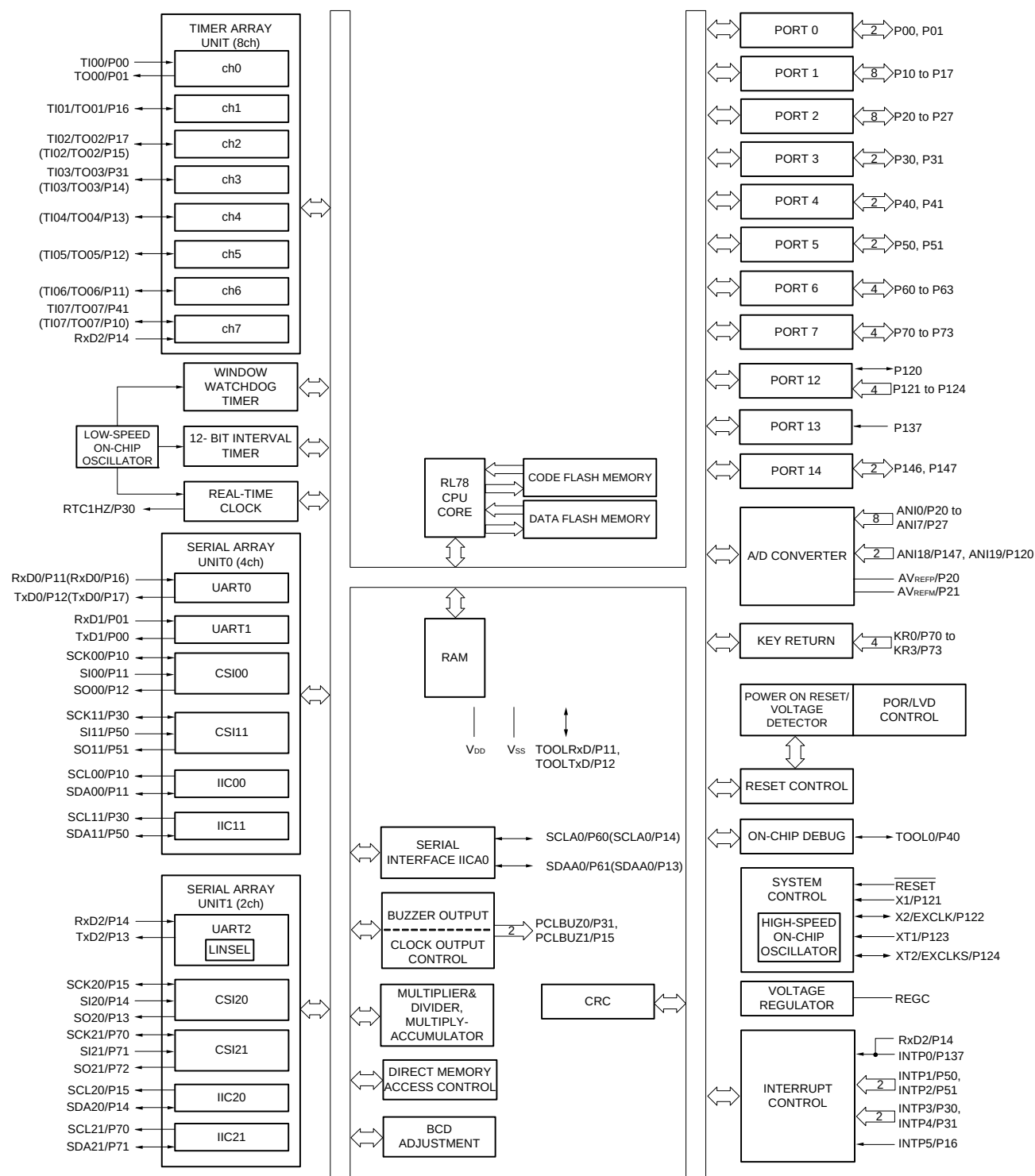
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.4 Pin Identification

ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI20:	Analog input	RESET:	Reset
AVREFM:	A/D converter negative reference voltage input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter positive reference voltage input	RxD0 to RxD3:	Receive data
EVDD0, EVDD1:	Power supply for port	SCLA0, SCLA1,	
EVSS0, EVSS1:	Ground for port	SCK00, SCK01, SCK10,	
EXCLK:	External clock input (Main system clock)	SCK11, SCK20, SCK21,	
EXCLKS:	External clock input (Subsystem clock)	SCK30, SCK31:	Serial clock input/output
INTP0 to INTP11:	Interrupt request from peripheral	SCL00, SCL01, SCL10,	
KR0 to KR7:	Key return	SCL11, SCL20, SCL21,	
P00 to P06:	Port 0	SCL30, SCL31:	Serial clock output
P10 to P17:	Port 1	SDAA0, SDAA1, SDA00,	
P20 to P27:	Port 2	SDA01, SDA10, SDA11,	
P30, P31:	Port 3	SDA20, SDA21, SDA30,	
P40 to P47:	Port 4	SDA31:	Serial data input/output
P50 to P57:	Port 5	SI00, SI01, SI10, SI11,	
P60 to P67:	Port 6	SI20, SI21, SI30, SI31:	Serial data input
P70 to P77:	Port 7	SO00, SO01, SO10,	
P80 to P87:	Port 8	SO11, SO20, SO21,	
P100 to P102:	Port 10	SO30, SO31:	Serial data output
P110, P111:	Port 11	TI00 to TI07,	
P120 to P124:	Port 12	TI10 to TI13:	Timer input
P130, P137:	Port 13	TO00 to TO07,	
P140 to P147:	Port 14	TO10 to TO13:	Timer output
P150 to P156:	Port 15	TOOL0:	Data input/output for tool
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	TOOLRxD, TOOLTxD:	Data input/output for external device
		TxD0 to TxD3:	Transmit data
		VDD:	Power supply
		VSS:	Ground
		X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

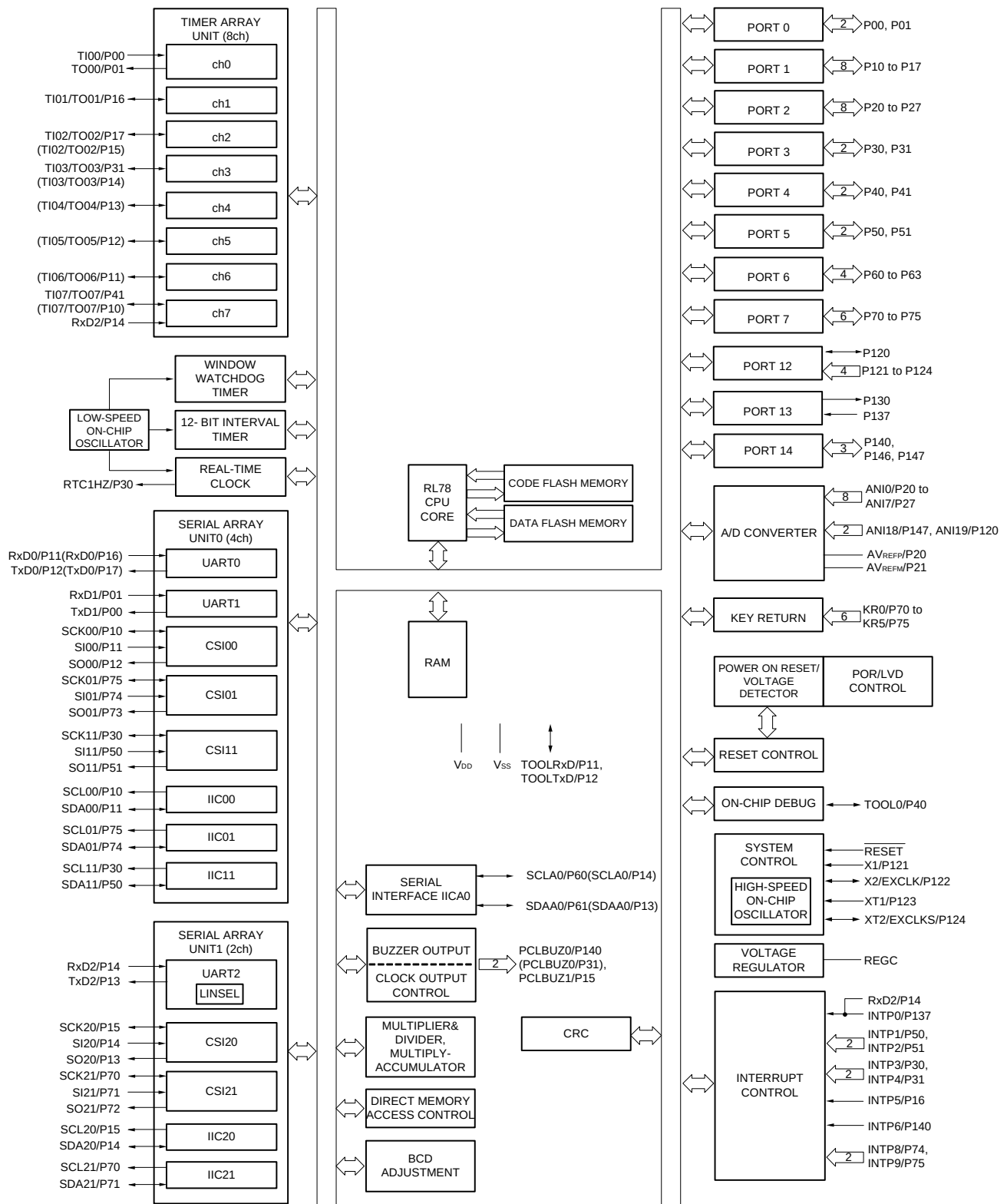
1.5 Block Diagram

1.5.1 44-pin products



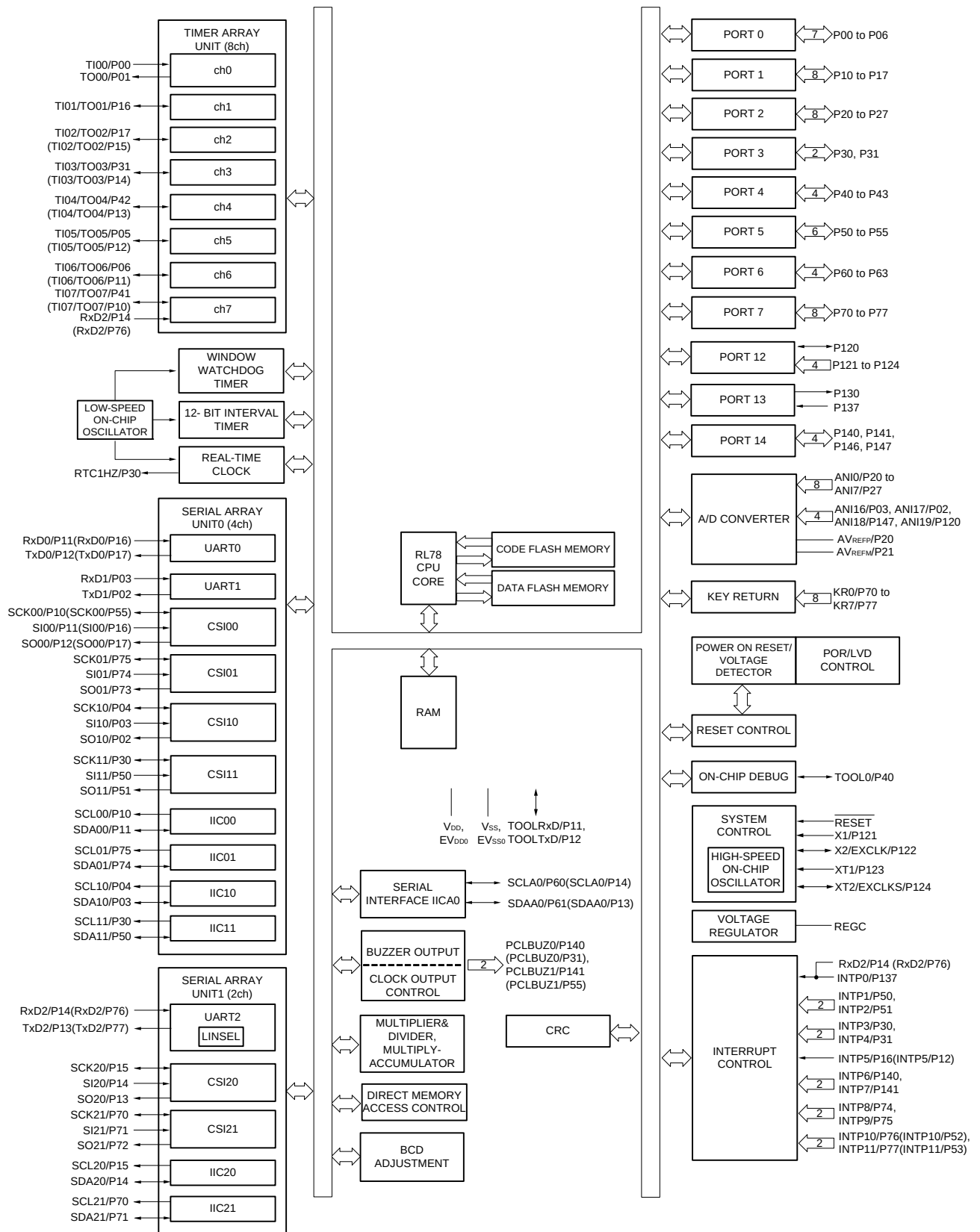
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.5.2 48-pin products



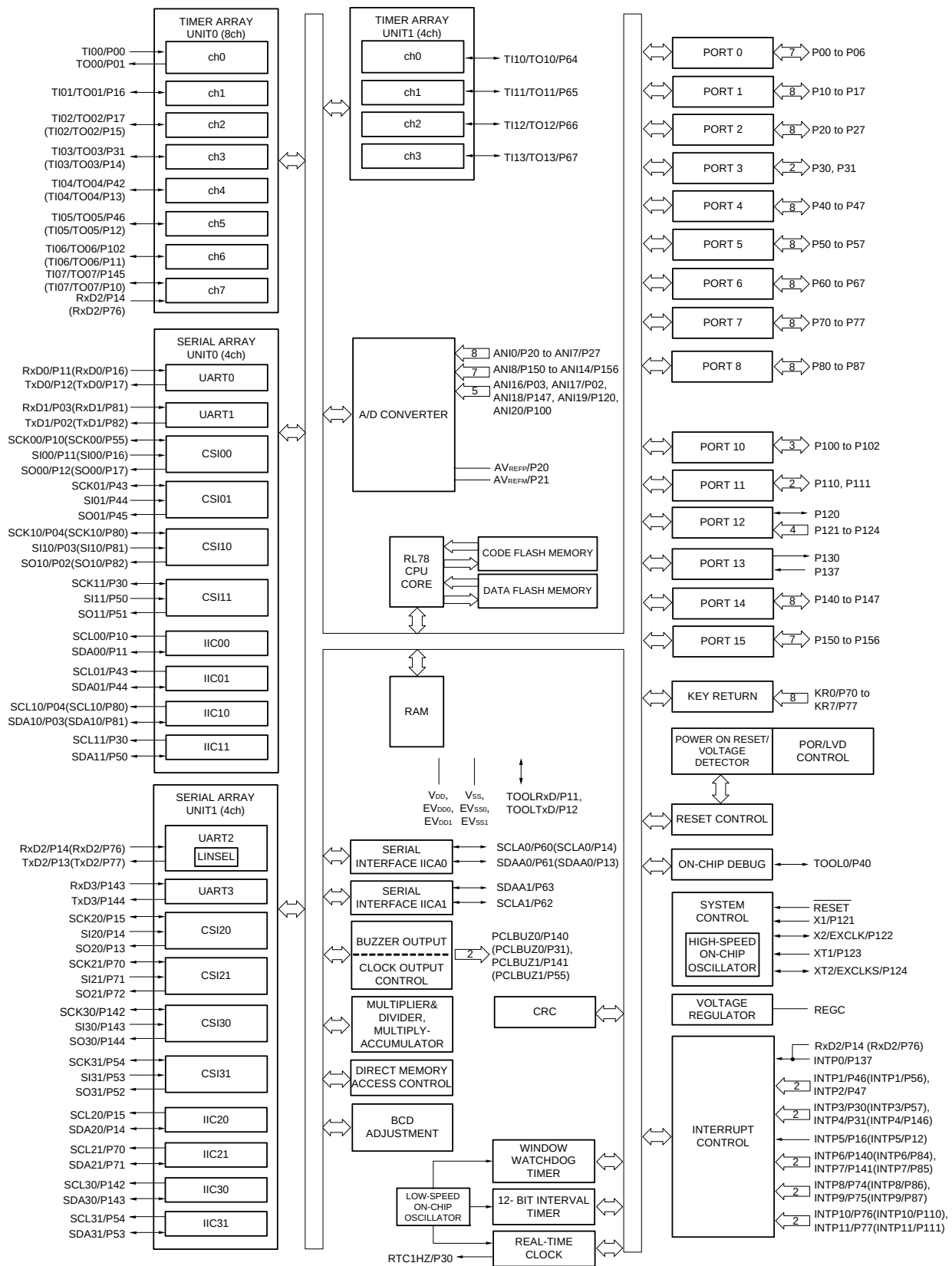
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.5.3 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.5.4 100-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13A User's Manual.

1.6 Outline of Functions

[44-pin, 48-pin, 64-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		44-pin	48-pin	64-pin
		R5F140Fx	R5F140Gx	R5F140Lx
Code flash memory (KB)		384, 512	384, 512	384, 512
Data flash memory (KB)		8	8	8
RAM (KB)		24, 32 ^{Note 1}	24, 32 ^{Note 1}	24, 32 ^{Note 1}
Address space		1 MB		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)		
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)		
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz		
Low-speed on-chip oscillator		15 kHz (typ.)		
General-purpose registers		(8-bit register $\times$ 8) $\times$ 4 banks		
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator: $f_{IH} = 32$ MHz operation)		
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)		
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits $\times$ 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		
I/O port	Total	40	44	58
	CMOS I/O	31 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)	34 (N-ch O.D. I/O [V_{DD} withstand voltage]: 11)	48 (N-ch O.D. I/O [V_{DD} withstand voltage]: 15)
	CMOS input	5	5	5
	CMOS output	—	1	1
	N-ch O.D. I/O (withstand voltage: 6 V)	4	4	4
Timer	16-bit timer	8 channels		
	Watchdog timer	1 channel		
	Real-time clock (RTC)	1 channel		
	12-bit interval timer (IT)	1 channel		
	Timer output	5 channels (PWM outputs: 4 ^{Note 2}), 8 channels (PWM outputs: 7 ^{Note 2}) ^{Note 3}		8 channels (PWM outputs: 7 ^{Note 2})
	RTC output	1 channel • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)		

- Notes**
- The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.
R5F140xL (x = F, G, L): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.
 - The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13A User's Manual).
 - When setting to PIOR = 1

(2/2)

Item		44-pin	48-pin	64-pin
		R5F140Fx	R5F140Gx	R5F140Lx
Clock output/buzzer output		2	2	2
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{\text{MAIN}} = 20 \text{ MHz}$ operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{\text{SUB}} = 32.768 \text{ kHz}$ operation)		
8/10-bit resolution A/D converter		10 channels	10 channels	12 channels
Serial interface		[44-pin products] - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin products] - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel		
		I ² C bus	1 channel	1 channel
Multiplier and divider/multiply-accumulator		16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)		
DMA controller		2 channels		
Vectored interrupt sources	Internal	27	27	27
	External	7	10	13
Key interrupt		4	6	8
Reset		- Reset by RESET pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access		
Power-on-reset circuit		- Power-on-reset: 1.51 V (typ.) - Power-down-reset: 1.50 V (typ.)		
Voltage detector		- Rising edge : 1.67 V to 4.06 V (14 stages) - Falling edge : 1.63 V to 3.98 V (14 stages)		
On-chip debug function		Provided		
Power supply voltage		$V_{\text{DD}} = 1.6 \text{ to } 5.5 \text{ V}$ ($T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$) $V_{\text{DD}} = 2.4 \text{ to } 5.5 \text{ V}$ ($T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$)		
Operating ambient temperature		$T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$ (A: Consumer applications) $T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$ (G: Industrial applications)		

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[100-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		100-pin
		R5F140Px
Code flash memory (KB)		384, 512
Data flash memory (KB)		8
RAM (KB)		24, 32 ^{Note 1}
Address space		1 MB
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator		15 kHz (typ.)
General-purpose register		(8-bit register × 8) × 4 banks
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator: $f_{IH} = 32$ MHz operation)
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.
I/O port	Total	92
	CMOS I/O	82 (N-ch O.D. I/O [E_{VDD} withstand voltage]: 24)
	CMOS input	5
	CMOS output	1
	N-ch O.D. I/O (withstand voltage: 6 V)	4
Timer	16-bit timer	12 channels
	Watchdog timer	1 channel
	Real-time clock (RTC)	1 channel
	12-bit interval timer (IT)	1 channel
	Timer output	12 channels (PWM outputs: 10 ^{Note 2})
	RTC output	1 channel • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F140xL (x = P): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13A User's Manual).

(2/2)

Item		100-pin
		R5F140Px
Clock output/buzzer output	2	
	2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{\text{MAIN}} = 20 \text{ MHz}$ operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{\text{SUB}} = 32.768 \text{ kHz}$ operation)	
8/10-bit resolution A/D converter		20 channels
Serial interface		[100-pin products]
		- CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel
	I ² C bus	2 channels
Multiplier and divider/multiply-accumulator		16 bits $\times$ 16 bits = 32 bits (Unsigned or signed) 32 bits $\div$ 32 bits = 32 bits (Unsigned) 16 bits $\times$ 16 bits + 32 bits = 32 bits (Unsigned or signed)
DMA controller		4 channels
Vectored interrupt sources	Internal	37
	External	13
Key interrupt		8
Reset		- Reset by $\overline{\text{RESET}}$ pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access
Power-on-reset circuit		- Power-on-reset: 1.51 V (typ.) - Power-down-reset: 1.50 V (typ.)
Voltage detector		- Rising edge : 1.67 V to 4.06 V (14 stages) - Falling edge : 1.63 V to 3.98 V (14 stages)
On-chip debug function		Provided
Power supply voltage		$V_{\text{DD}} = 1.6 \text{ to } 5.5 \text{ V}$ ($T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$) $V_{\text{DD}} = 2.4 \text{ to } 5.5 \text{ V}$ ($T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$)
Operating ambient temperature		$T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$ (A: Consumer applications) $T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$ (G: Industrial applications)

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R> **2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)**

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

R5F140xxAxx

G: Industrial applications when $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

R5F140xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13A User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to $+6.5$	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to $+0.3$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.1$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI16 to ANI20	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ ^{Notes 2, 3}	V
	V_{AI2}	ANI0 to ANI14	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed $AV_{REF}(+) + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. $AV_{REF}(+)$: Positive reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (2/2)

Absolute Maximum Ratings (TA = 25 °C) (1/2)					
Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	−100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	TA	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	Tstg			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
		$1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$	1.0		8.0	MHz
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	MHz
XT1 clock oscillation frequency (f_x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G13A User's Manual.

2.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy			-1.0		+1.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	1.6 V ≤ EV _{DD0} ≤ 5.5 V		–10.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		–55.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		–10.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		–5.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		–2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		–80.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		–19.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		–10.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		–5.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ EV _{DD0} ≤ 5.5 V		–135.0 ^{Note 4}	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V		–0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F140xxGxx) is –100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I_{OL} ^{Note 1}	$\text{I}_{\text{OL}1}$	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		70.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		15.0	mA
			$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		9.0	mA
			$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		80.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		35.0	mA
			$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		20.0	mA
			$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$		10.0	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})			150.0	mA
	$\text{I}_{\text{OL}2}$	Per pin for P20 to P27, P150 to P156			0.4 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $\text{EV}_{\text{SS}0}$, $\text{EV}_{\text{SS}1}$ and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).

- Total output current of pins = $(\text{I}_{\text{OL}} \times 0.7) / (n \times 0.01)$

<Example> Where $n = 80\%$ and $\text{I}_{\text{OL}} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7) / (80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	$0.8\text{EV}_{\text{DD0}}$	EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	2.2	EV_{DD0}	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	2.0	EV_{DD0}	V
			TTL input buffer $1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	1.5	EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156	0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63	$0.7\text{EV}_{\text{DD0}}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0	$0.2\text{EV}_{\text{DD0}}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20 to P27, P150 to P156	0		0.3V_{DD}	V
	V_{IL4}	P60 to P63	0		$0.3\text{EV}_{\text{DD0}}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 is EV_{DD0} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -10.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 1.5$		V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
			$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 5.5\text{ V}$, $\text{I}_{\text{OH1}} = -1.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	V_{OH2}	P20 to P27, P150 to P156	$1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 20\text{ mA}$		1.3	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
			$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 5.5\text{ V}$, $\text{I}_{\text{OL1}} = 0.3\text{ mA}$		0.4	V
	V_{OL2}	P20 to P27, P150 to P156	$1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	V_{OL3}	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V
			$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 5.5\text{ V}$, $\text{I}_{\text{OL3}} = 1.0\text{ mA}$		0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq V_{DD0} = V_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = V_{SS0} = V_{SS1} = 0\text{ V}$) (5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{DD0}			1	μA	
	I _{LIH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}			1	μA	
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	I _{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0}			−1	μA	
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}			−1	μA	
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input		−1	μA	
				In resonator connection		−10	μA	
On-chip pll-up resistance	R _U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		1.5		mA
						$V_{DD} = 3.0\text{ V}$		1.5		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		3.4	6.8	mA
						$V_{DD} = 3.0\text{ V}$		3.4	6.8	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	5.3	mA
						$V_{DD} = 3.0\text{ V}$		2.7	5.3	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2	3.8	mA
						$V_{DD} = 3.0\text{ V}$		2	3.8	mA
			LS (low-speed main) mode Note 5	$f_{IH} = 8\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 3.0\text{ V}$		1.1	1.9	mA
						$V_{DD} = 2.0\text{ V}$		1.1	1.9	mA
			LV (low-voltage main) mode Note 5	$f_{IH} = 4\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 3.0\text{ V}$		0.7	1.2	mA
						$V_{DD} = 2.0\text{ V}$		0.7	1.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		2.2	4.4	mA
						Resonator connection		2.3	4.5	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		2.2	4.4	mA
						Resonator connection		2.3	4.5	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.4	2.6	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.4	2.6	mA
			LS (low-speed main) mode Note 5	$f_{MX} = 8\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		0.9	1.7	mA
						Resonator connection		1	1.8	mA
				$f_{MX} = 8\text{ MHz}$ Note 2, $V_{DD} = 2.0\text{ V}$	Normal operation	Square wave input		0.9	1.7	mA
						Resonator connection		1	1.8	mA
			Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4	5.5	μA
						Resonator connection		4	5.7	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.2	6.7	μA
						Resonator connection		4.3	6.9	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.5	9.3	μA
						Resonator connection		4.7	9.5	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.3	15.8	μA
						Resonator connection		5.6	16	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		6.6	25.8	μA
						Resonator connection		7.1	26	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , EV_{DD1} or V_{SS} , EV_{SS0} , EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @1 MHz to 4 MHz

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.41	1.71	mA	
					V _{DD} = 3.0 V		0.41	1.71	mA	
				f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.34	1.35	mA	
					V _{DD} = 3.0 V		0.34	1.35	mA	
				f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.33	1.04	mA	
					V _{DD} = 3.0 V		0.33	1.04	mA	
			LS (low-speed main) mode Note 7	f _{IH} = 8 MHz Note 4	V _{DD} = 3.0 V		290	650	μA	
					V _{DD} = 2.0 V		290	650	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz Note 4	V _{DD} = 3.0 V		270	540	μA	
					V _{DD} = 2.0 V		270	540	μA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.19	1.05	mA	
					Resonator connection		0.37	1.26	mA	
				f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.19	1.05	mA	
					Resonator connection		0.37	1.26	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.12	0.62	mA	
					Resonator connection		0.22	0.73	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.12	0.62	mA	
					Resonator connection		0.22	0.73	mA	
			LS (low-speed main) mode Note 7	f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V	Square wave input		100	410	μA	
					Resonator connection		200	520	μA	
				f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V	Square wave input		100	410	μA	
					Resonator connection		200	520	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5 T _A = −40°C	Square wave input		0.39	1	μA	
					Resonator connection		0.48	1.3	μA	
				f _{SUB} = 32.768 kHz Note 5 T _A = +25°C	Square wave input		0.55	2.2	μA	
					Resonator connection		0.64	2.5	μA	
				f _{SUB} = 32.768 kHz Note 5 T _A = +50°C	Square wave input		0.98	4.8	μA	
					Resonator connection		1.07	5.1	μA	
				f _{SUB} = 32.768 kHz Note 5 T _A = +70°C	Square wave input		1.73	11.3	μA	
					Resonator connection		1.82	11.6	μA	
				f _{SUB} = 32.768 kHz Note 5 T _A = +85°C	Square wave input		2.73	21.3	μA	
					Resonator connection		2.82	21.6	μA	
	IDD3 Note 6	STOP mode Note 8	T _A = −40°C					0.26	0.7	μA
			T _A = +25°C					0.42	1.9	μA
			T _A = +50°C					0.85	4.5	μA
			T _A = +70°C					1.60	11	μA
			T _A = +85°C					2.60	21	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , EV_{DD1} or V_{SS} , EV_{SS0} , EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$
LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH} : High-speed on-chip oscillator clock frequency
3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

Peripheral Functions (Common to all products)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} ^{Note 1}				0.2		μA
RTC operating current	I_{RTC} ^{Notes 1, 2, 3}				0.02		μA
12-bit interval timer operating current	I_{IT} ^{Notes 1, 2, 4}				0.02		μA
Watchdog timer operating current	I_{WDT} ^{Notes 1, 2, 5}	$f_{IL} = 15\text{ kHz}$			0.22		μA
A/D converter operating current	I_{ADC} ^{Notes 1, 6}	When conversion at maximum speed	Normal mode, $AV_{REFP} = V_{DD} = 5.0\text{ V}$		1.3	1.7	mA
			Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} ^{Note 1}				100		μA
Temperature sensor operating current	I_{TMPS} ^{Note 1}				100		μA
LVD operating current	I_{LVI} ^{Notes 1, 7}				0.02		μA
Self-programming operating current	I_{FSP} ^{Notes 1, 9}				2.5	12.2	mA
BGO operating current	I_{BGO} ^{Notes 1, 8}				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ} ^{Note 1}	ADC operation	The mode is performed ^{Note 10}		0.5	0.6	mA
			The A/D conversion operations are performed, Low voltage mode, $AV_{REFP} = V_{DD} = 3.0\text{ V}$		0.9	1.1	mA
		CSI/UART operation			0.5	0.62	mA

Notes 1. Current flowing to V_{DD} .

- When high speed on-chip oscillator and high-speed system clock are stopped.
- Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
- Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2} , and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
- Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

- Notes**
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13A User's Manual.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

2.4 AC Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125	1	μs
				$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.0625	1	μs
			LS (low-speed main) mode	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.125	1	μs
			LV (low-voltage main) mode	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.25	1	μs
		Subsystem clock (f_{SUB}) operation		$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	28.5	30.5	μs
		In the self programming mode	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125	1	μs
				$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.0625	1	μs
			LS (low-speed main) mode	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.125	1	μs
			LV (low-voltage main) mode	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.25	1	μs
External system clock frequency	f_{EX}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.0		16.0	MHz
		$1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$		1.0		8.0	MHz
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		1.0		4.0	MHz
	f_{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		24			ns
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		30			ns
		$1.8\text{ V} \leq V_{DD} < 2.4\text{ V}$		60			ns
		$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$		120			ns
	t_{EXHS}, t_{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI13 input high-level width, low-level width	t_{TIH}, t_{TIL}			$1/f_{MCK}+10$			ns ^{Note}
TO00 to TO07, TO10 to TO13 output frequency	f_{TO}	HS (high-speed main) mode	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			8	MHz
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$			4	MHz
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			2	MHz
		LS (low-speed main) mode	$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			4	MHz
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			2	MHz
		LV (low-voltage main) mode	$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$			8	MHz
			$1.8\text{ V} \leq EV_{DD0} < 2.7\text{ V}$			4	MHz
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			2	MHz
		LS (low-speed main) mode	$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			4	MHz
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			2	MHz
		LV (low-voltage main) mode	$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$			4	MHz
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1			μs
		INTP1 to INTP11	$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	250			ns
			$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$	1			μs
RESET low-level width	t_{RSL}			10			μs

(Note and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$

$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MIN. 125 ns

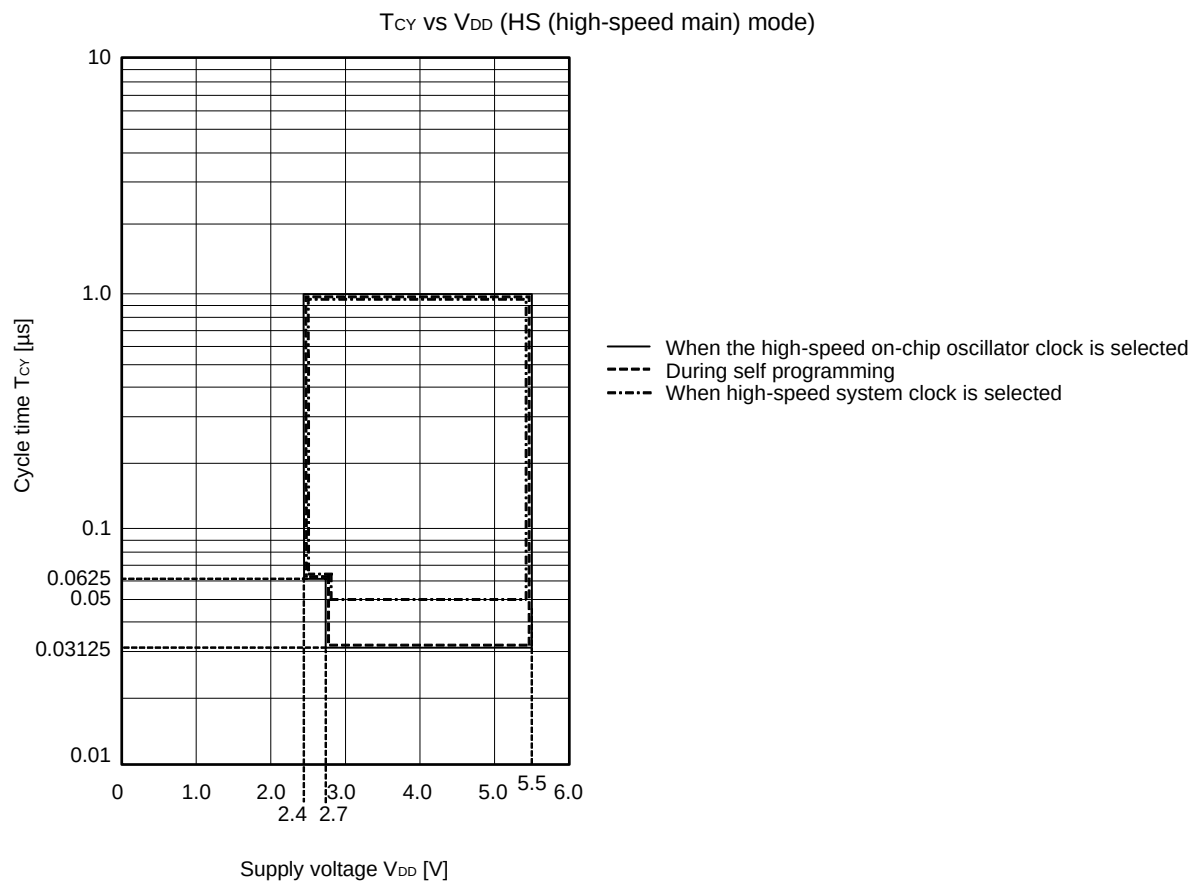
$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$: MIN. 250 ns

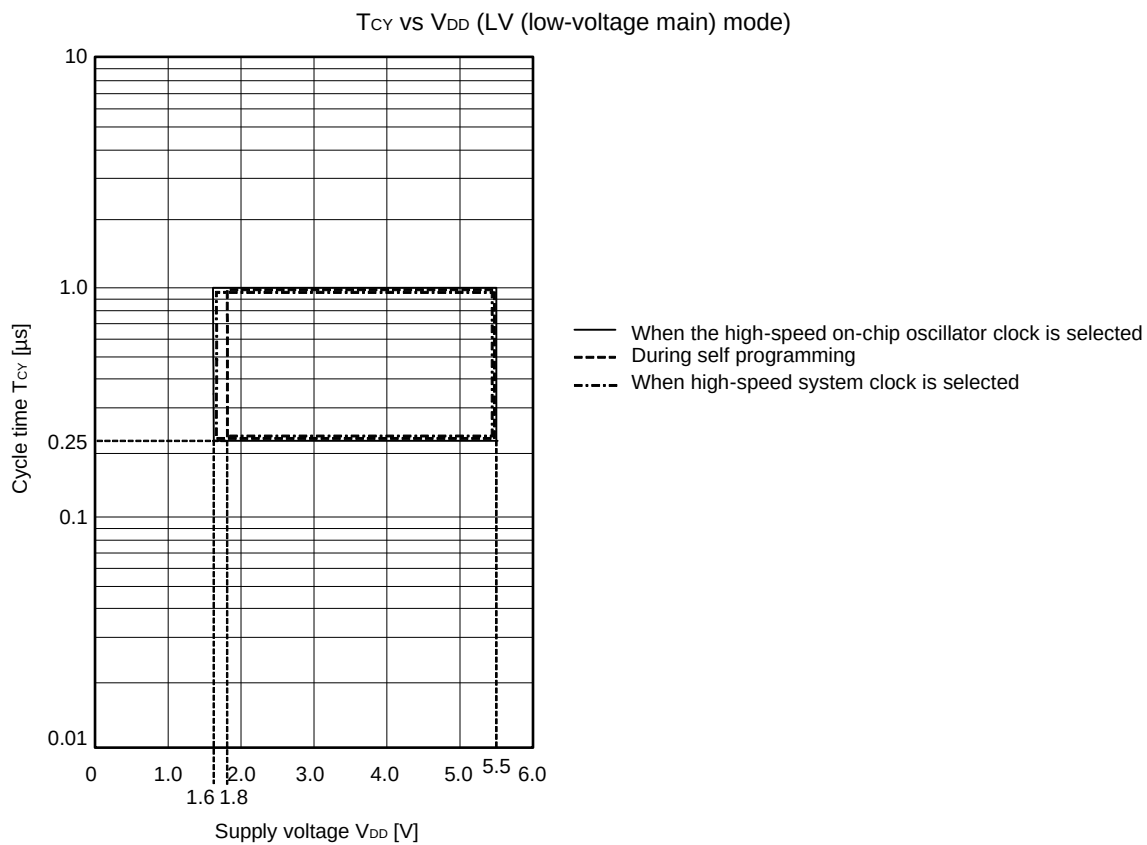
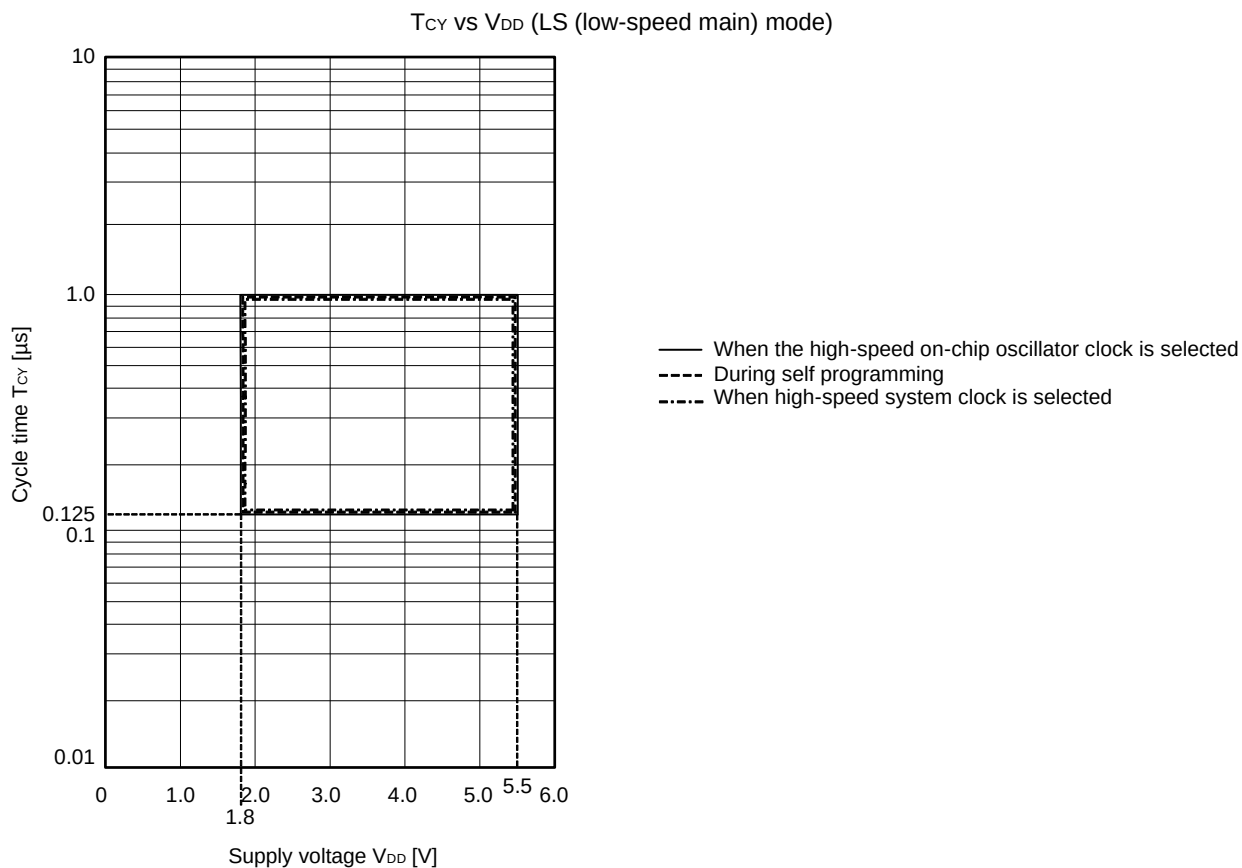
Remark f_{MCK} : Timer array unit operation clock frequency

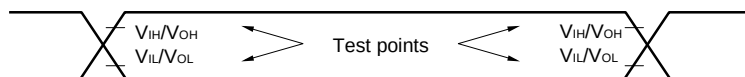
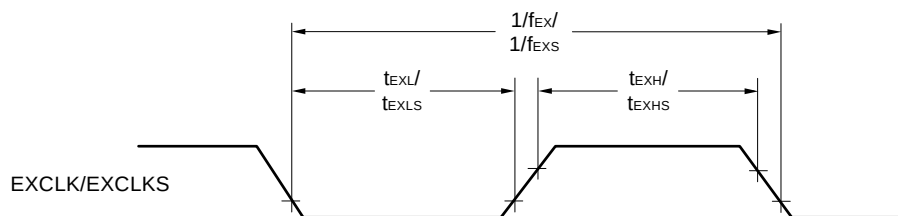
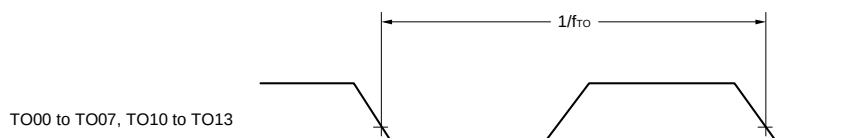
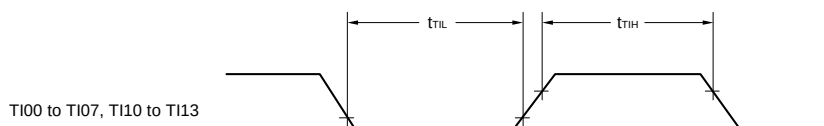
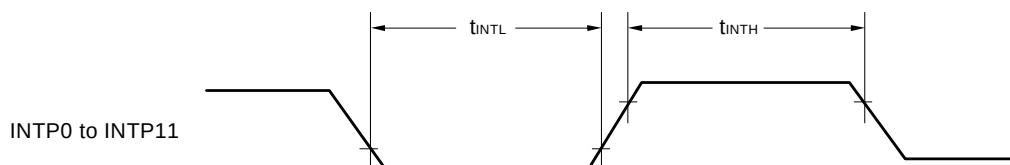
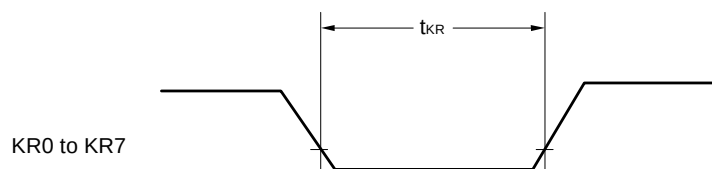
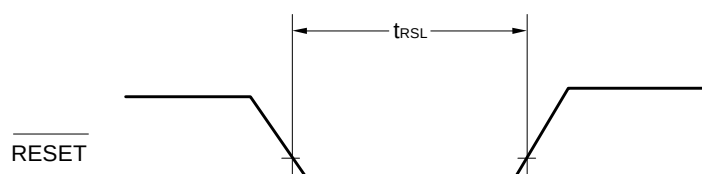
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number ($m = 0, 1$), n: Channel number ($n = 0$ to 7))

Minimum Instruction Execution Time during Main System Clock Operation

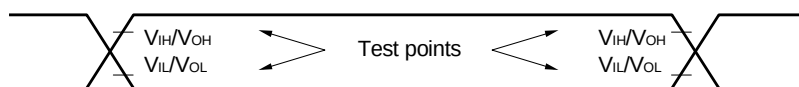




AC Timing Test Points**External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate ^{Note 1}		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$f_{MCK}/6$ ^{Note 2}		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 3}		5.3		1.3		0.6	Mbps
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$f_{MCK}/6$ ^{Note 2}		$f_{MCK}/6$		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 3}		5.3		1.3		0.6	Mbps
		$1.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$f_{MCK}/6$ ^{Note 2}		$f_{MCK}/6$ ^{Note 2}		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 3}		5.3		1.3		0.6	Mbps
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	—			$f_{MCK}/6$ ^{Note 2}		$f_{MCK}/6$	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ ^{Note 3}	—			1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps

$1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps

$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

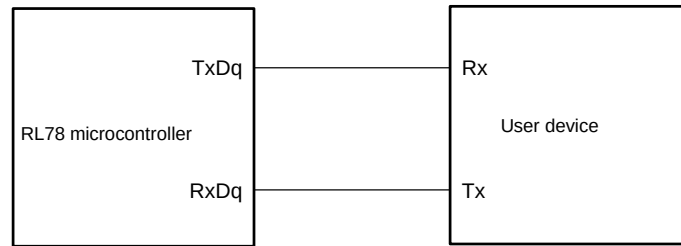
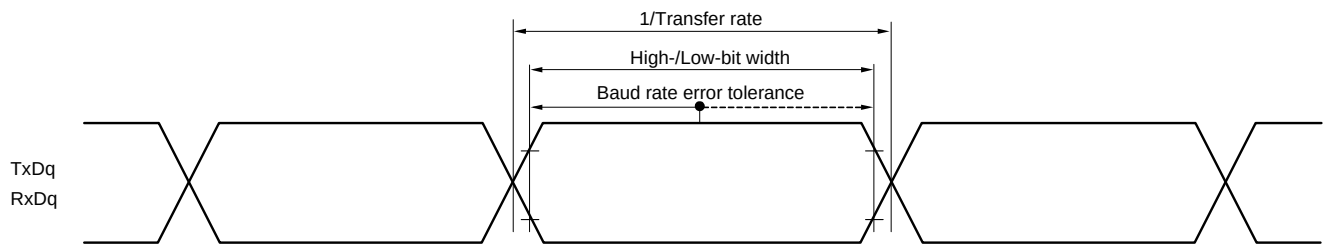
HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

16 MHz ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

- Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- 2.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
 n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK}	4.0 V ≤ EV _{DD0} ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EV _{DD0} ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V		t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V		t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V		33		110		110		ns
Slp hold time (from SCKp↑) Note 2	t _{KS1}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOP output Note 3	t _{KSO1}	C = 20 pF Note 4			10		10		10	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOP output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SCKp and SOP output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOP pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. This value is valid only when CSI00's peripheral I/O redirect function is not used.
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	125		500		1000		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	250		500		1000		ns
			$1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	500		500		1000		ns
			$1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	1000		1000		1000		ns
			$1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	–		1000		1000		ns
SCKp high-/low-level width	$t_{\text{KH1}}, t_{\text{KL1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY1}}/2 - 12$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY1}}/2 - 18$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY1}}/2 - 38$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY1}}/2 - 100$		$t_{\text{KCY1}}/2 - 100$		$t_{\text{KCY1}}/2 - 100$		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		–		$t_{\text{KCY1}}/2 - 100$		$t_{\text{KCY1}}/2 - 100$		ns
Slp setup time (to SCKp↑) Note 1	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		44		110		110		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		44		110		110		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		75		110		110		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		110		110		110		ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		220		220		220		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		–		220		220		ns
Slp hold time (from SCKp↑) Note 2	t_{KSI1}	$1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		19		19		19		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		–		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	$1.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ Note 4			25		25		25	ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ $C = 30\text{ pF}$ Note 4			–		25		25	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp↓” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp↓” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp↑” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
- 2.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		—		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		—		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 500		$6/f_{MCK}$ and 500		$6/f_{MCK}$ and 500		ns
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 750		$6/f_{MCK}$ and 750		$6/f_{MCK}$ and 750		ns
		$1.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$6/f_{MCK}$ and 1500		$6/f_{MCK}$ and 1500		$6/f_{MCK}$ and 1500		ns
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		—		$6/f_{MCK}$ and 1500		$6/f_{MCK}$ and 1500		ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$t_{KCY2}/2 - 7$		$t_{KCY2}/2 - 7$		$t_{KCY2}/2 - 7$		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$t_{KCY2}/2 - 8$		$t_{KCY2}/2 - 8$		$t_{KCY2}/2 - 8$		ns
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$t_{KCY2}/2 - 18$		$t_{KCY2}/2 - 18$		$t_{KCY2}/2 - 18$		ns
		$1.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		ns
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		—		$t_{KCY2}/2 - 66$		$t_{KCY2}/2 - 66$		ns

(Notes, Caution, and Remarks are listed on the next page.)

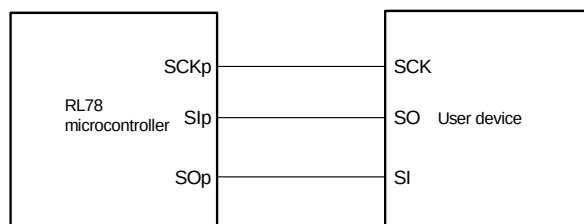
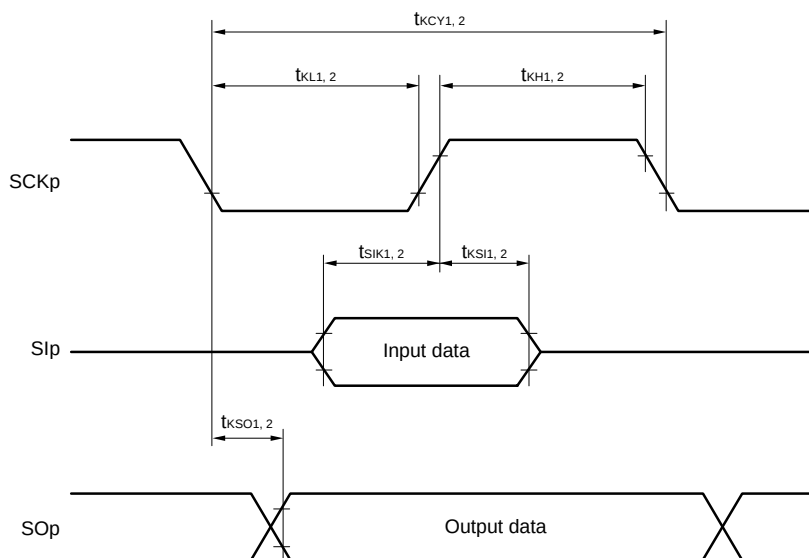
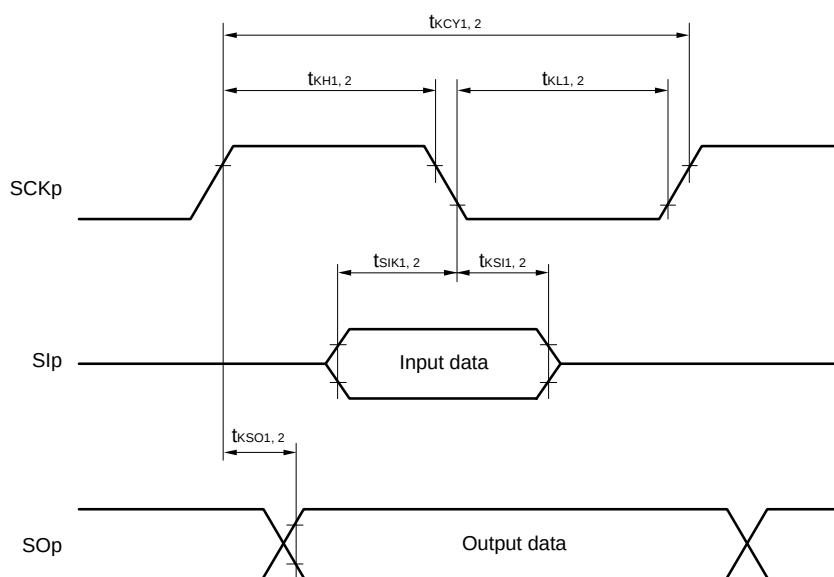
(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main)		LS (low-speed main)		LV (low-voltage main)		Unit	
				Mode		Mode		Mode			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +20		1/f _{MCK} +30		1/f _{MCK} +30		ns	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +40		1/f _{MCK} +40		1/f _{MCK} +40		ns	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +40		1/f _{MCK} +40		ns	
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		ns	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} + 250		1/f _{MCK} + 250		1/f _{MCK} + 250		ns	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} + 250		1/f _{MCK} + 250		ns	
Delay time from SCKp↓ to SOP output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ EV _{DD0} ≤ 5.5 V			2/f _{MCK} + 44		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			2.4 V ≤ EV _{DD0} ≤ 5.5 V			2/f _{MCK} + 75		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.8 V ≤ EV _{DD0} ≤ 5.5 V			2/f _{MCK} + 110		2/f _{MCK} + 110		2/f _{MCK} + 110	ns
			1.7 V ≤ EV _{DD0} ≤ 5.5 V			2/f _{MCK} + 220		2/f _{MCK} + 220		2/f _{MCK} + 220	ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V			—		2/f _{MCK} + 220		2/f _{MCK} + 220	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)
CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential)
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) During communication at same potential (simplified I²C mode) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		1000 Note 1		400 Note 1		400 Note 1	kHz
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		400 Note 1		400 Note 1		400 Note 1	kHz
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$		300 Note 1		300 Note 1		300 Note 1	kHz
		$1.7\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$		250 Note 1		250 Note 1		250 Note 1	kHz
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1150		1150		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	1150		1150		1150		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1550		1550		1550		ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1850		1850		1850		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	—		1850		1850		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	475		1150		1150		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	1150		1150		1150		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1550		1550		1550		ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	1850		1850		1850		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

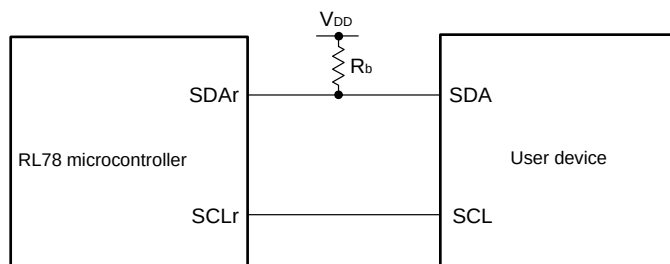
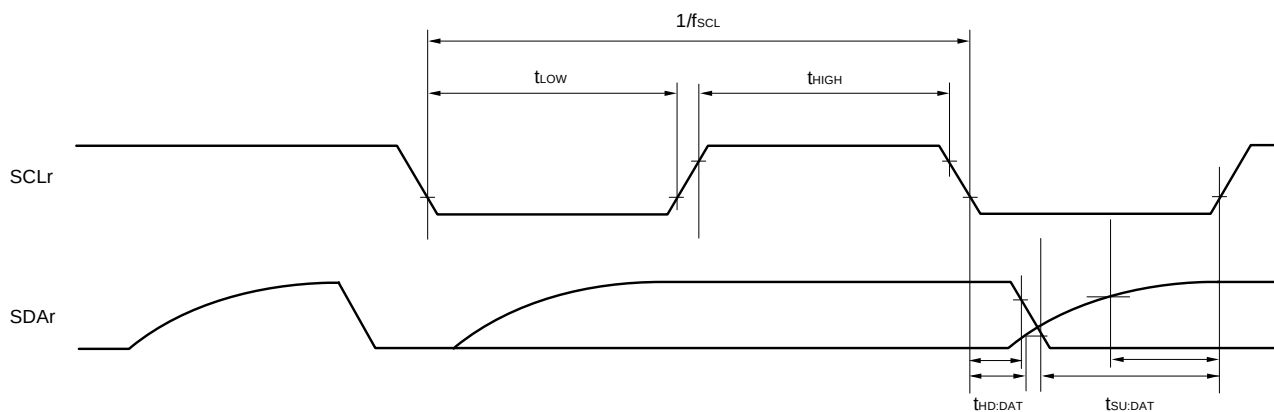
(5) During communication at same potential (simplified I²C mode) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 85$ Note2		$1/f_{\text{MCK}} + 145$ Note2		$1/f_{\text{MCK}} + 145$ Note2		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 145$ Note2		$1/f_{\text{MCK}} + 145$ Note2		$1/f_{\text{MCK}} + 145$ Note2		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	$1/f_{\text{MCK}} + 230$ Note2		$1/f_{\text{MCK}} + 230$ Note2		$1/f_{\text{MCK}} + 230$ Note2		ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	$1/f_{\text{MCK}} + 290$ Note2		$1/f_{\text{MCK}} + 290$ Note2		$1/f_{\text{MCK}} + 290$ Note2		ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	—		$1/f_{\text{MCK}} + 290$ Note2		$1/f_{\text{MCK}} + 290$ Note2		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	355	0	355	0	355	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	0	405	0	405	0	405	ns
		$1.7\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	0	405	0	405	0	405	ns
		$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5\text{ k}\Omega$	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.			
Transfer rate		Reception	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
						5.3		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4								
						5.3		1.3		0.6	Mbps
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
						5.3		1.3		0.6	Mbps
Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4											
			5.3		1.3		0.6	Mbps			
1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 Notes 1 to 3		f _{MCK} /6 Notes 1, 2		f _{MCK} /6 Notes 1, 2	bps			
			5.3		1.3		0.6	Mbps			
Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4											

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with $\text{EV}_{\text{DD}0} \geq \text{V}_b$.**3.** The following conditions are required for low voltage interface when $\text{EV}_{\text{DD}0} < \text{V}_{\text{DD}}$. $2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$: MAX. 2.6 Mbps $1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.4\text{ V}$: MAX. 1.3 Mbps**4.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)16 MHz ($2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)LS (low-speed main) mode: 8 MHz ($1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)LV (low-voltage main) mode: 4 MHz ($1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $\text{V}_b[\text{V}]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Note 1		Note 1		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.8 Note 2		2.8 Note 2		Mbps
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Note 3		Note 3		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 Note 4		1.2 Note 4		Mbps
			1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Notes 5, 6		Notes 5, 6		bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 Note 7		0.43 Note 7		Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

Notes 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq E_{VDD0} < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with $E_{VDD0} \geq V_b$.
6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq E_{VDD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

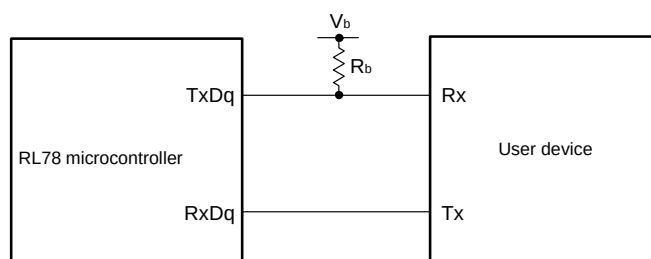
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

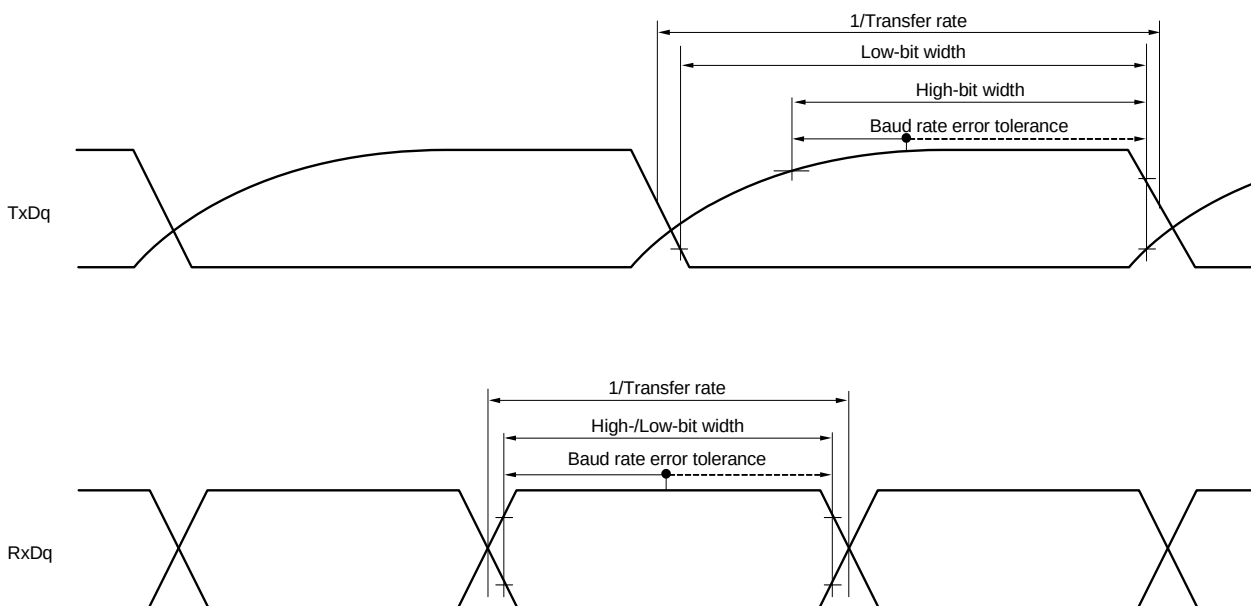
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/E_{VDD} tolerance (When 64- and 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
- 4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 2/f_{\text{CLK}}$ $4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		200		1150		1150		ns
				300		1150		1150		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 120$		$t_{\text{KCY1}}/2 - 120$		$t_{\text{KCY1}}/2 - 120$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 7$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 10$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		58		479		479		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		121		479		479		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		10		10		10		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		10		10		10		ns
Delay time from SCKp $\downarrow$ to SOP output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$			60		60		60	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$			130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	23		110		110		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	33		110		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	10		10		10		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	10		10		10		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		10		10		10	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
 g: PIM and POM number (g = 1)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	300		1150		1150		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	500		1150		1150		ns
			$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}^{\text{Note}}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 75$		$t_{\text{KCY1}}/2 - 75$		$t_{\text{KCY1}}/2 - 75$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 170$		$t_{\text{KCY1}}/2 - 170$		$t_{\text{KCY1}}/2 - 170$		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}^{\text{Note}}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 458$		$t_{\text{KCY1}}/2 - 458$		$t_{\text{KCY1}}/2 - 458$		ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 12$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 18$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}^{\text{Note}}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		$t_{\text{KCY1}}/2 - 50$		ns

Note Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	81		479		479		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	177		479		479		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	479		479		479		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	19		19		19		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	19		19		19		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	19		19		19		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		100		100		100	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		195		195		195	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		483		483		483	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

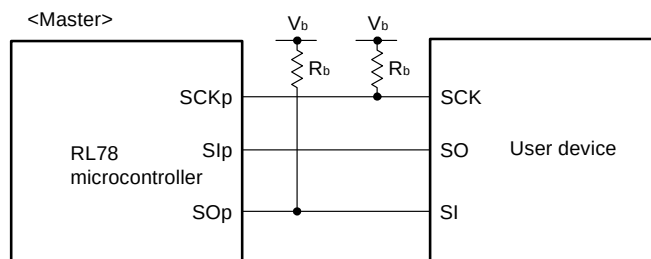
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	44		110		110		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	44		110		110		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	19		19		19		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	19		19		19		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		25		25		25	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		25		25		25	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		25		25		25	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. Use it with $\text{EV}_{\text{DD0}} \geq \text{V}_b$.

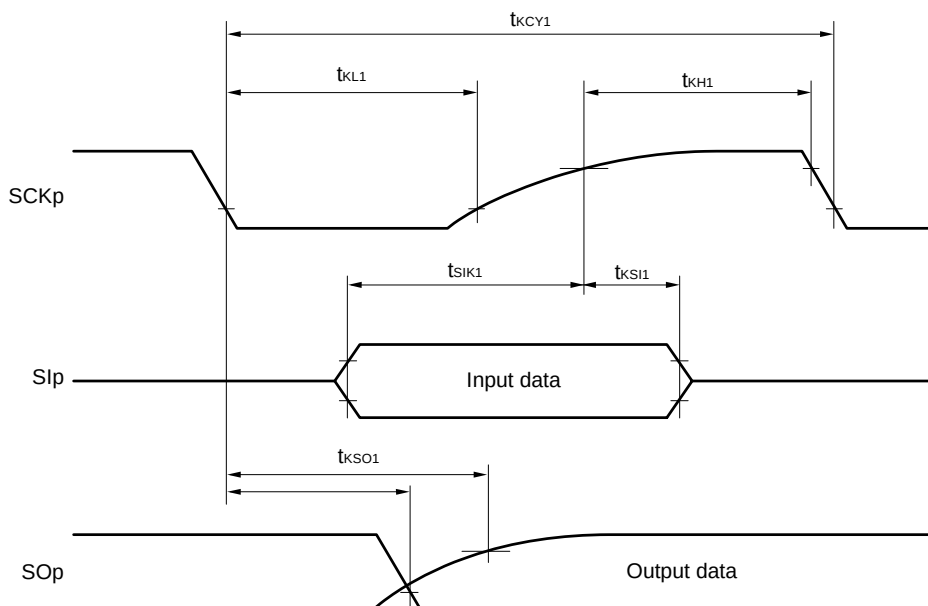
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 44- and 48-pin products)/ EV_{DD} tolerance (When 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

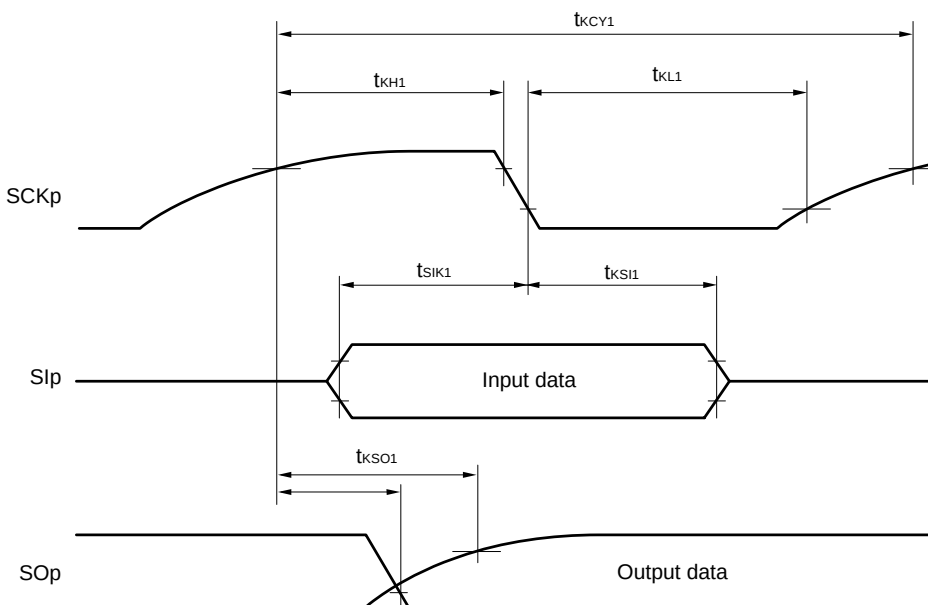
CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number ($p = 00, 01, 10, 20, 30, 31$), m: Unit number, n: Channel number ($mn = 00, 01, 02, 10, 12, 13$), g: PIM and POM number ($g = 0, 1, 4, 5, 8, 14$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 4. CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	14/ f_{MCK}		–		–		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	12/ f_{MCK}		–		–		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	10/ f_{MCK}		–		–		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	8/ f_{MCK}		16/ f_{MCK}		–		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	6/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	20/ f_{MCK}		–		–		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	16/ f_{MCK}		–		–		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	14/ f_{MCK}		–		–		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	12/ f_{MCK}		–		–		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	8/ f_{MCK}		16/ f_{MCK}		–		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	6/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$24\text{ MHz} < f_{\text{MCK}}$	48/ f_{MCK}		–		–		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	36/ f_{MCK}		–		–		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	32/ f_{MCK}		–		–		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	26/ f_{MCK}		–		–		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	16/ f_{MCK}		16/ f_{MCK}		–		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	10/ f_{MCK}		10/ f_{MCK}		10/ f_{MCK}		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

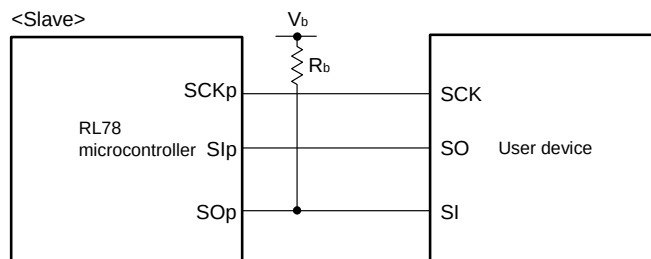
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	$t_{\text{KH}2}$, $t_{\text{KL}2}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$t_{\text{KCY}2}/2 - 12$		$t_{\text{KCY}2}/2 - 50$		$t_{\text{KCY}2}/2 - 50$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$t_{\text{KCY}2}/2 - 18$		$t_{\text{KCY}2}/2 - 50$		$t_{\text{KCY}2}/2 - 50$		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$t_{\text{KCY}2}/2 - 50$		$t_{\text{KCY}2}/2 - 50$		$t_{\text{KCY}2}/2 - 50$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 3}	$t_{\text{SIK}2}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$1/f_{\text{MCK}} + 20$		$1/f_{\text{MCK}} + 30$		$1/f_{\text{MCK}} + 30$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$1/f_{\text{MCK}} + 20$		$1/f_{\text{MCK}} + 30$		$1/f_{\text{MCK}} + 30$		ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$1/f_{\text{MCK}} + 30$		$1/f_{\text{MCK}} + 30$		$1/f_{\text{MCK}} + 30$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 4}	$t_{\text{KSI}2}$		$1/f_{\text{MCK}} + 31$		$1/f_{\text{MCK}} + 31$		$1/f_{\text{MCK}} + 31$		ns
Delay time from SCKp $\downarrow$ to SOP output ^{Note 5}	$t_{\text{KSO}2}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{\text{MCK}} + 120$		$2/f_{\text{MCK}} + 573$		$2/f_{\text{MCK}} + 573$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{\text{MCK}} + 214$		$2/f_{\text{MCK}} + 573$		$2/f_{\text{MCK}} + 573$	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{\text{MCK}} + 573$		$2/f_{\text{MCK}} + 573$		$2/f_{\text{MCK}} + 573$	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with $\text{EV}_{\text{DD}0} \geq \text{V}_b$.3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes "to SCKp $\downarrow$ " when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.4. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes "from SCKp $\downarrow$ " when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.5. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOP output becomes "from SCKp $\uparrow$ " when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

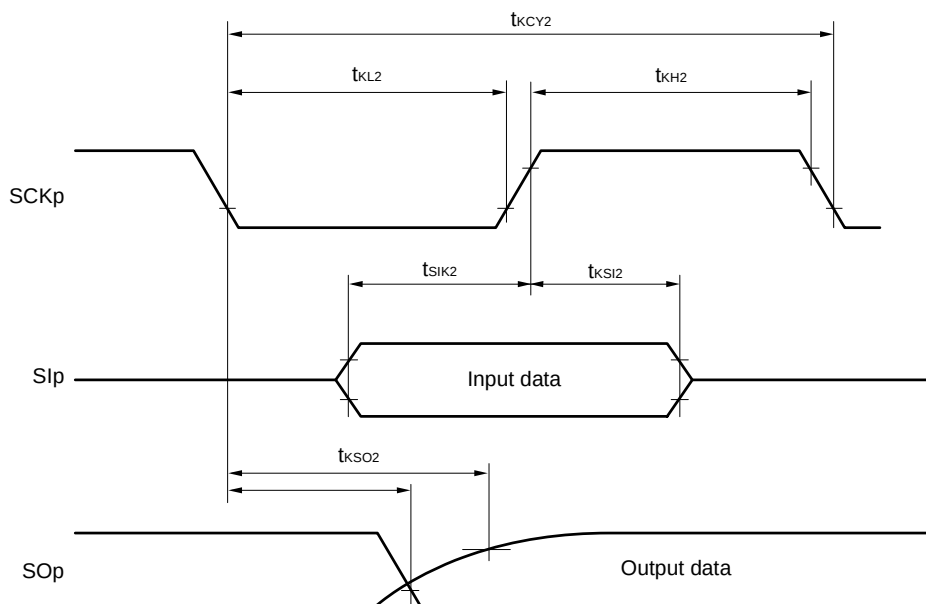
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SOP pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

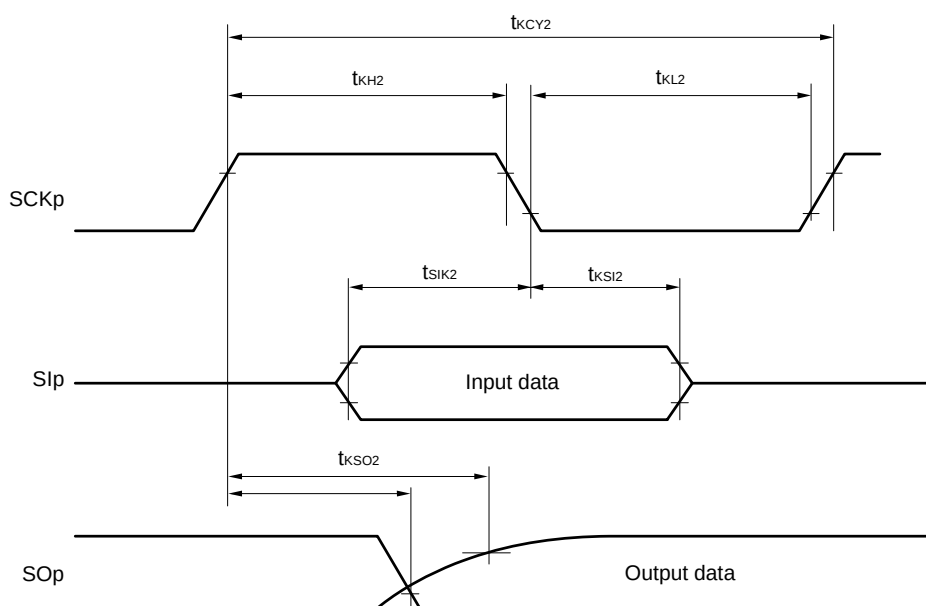
CSI mode connection diagram (during communication at different potential)

- Remarks**
- $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
 - p : CSI number ($p = 00, 01, 10, 20, 30, 31$), m : Unit number, n : Channel number ($mn = 00, 01, 02, 10, 12, 13$), g : PIM and POM number ($g = 0, 1, 4, 5, 8, 14$)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}).
 m : Unit number, n : Channel number ($mn = 00, 01, 02, 10, 12, 13$))
 - CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
2. CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		ns

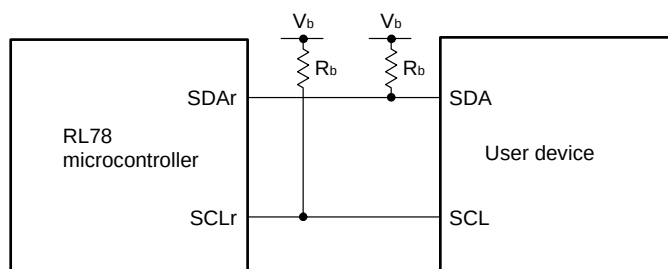
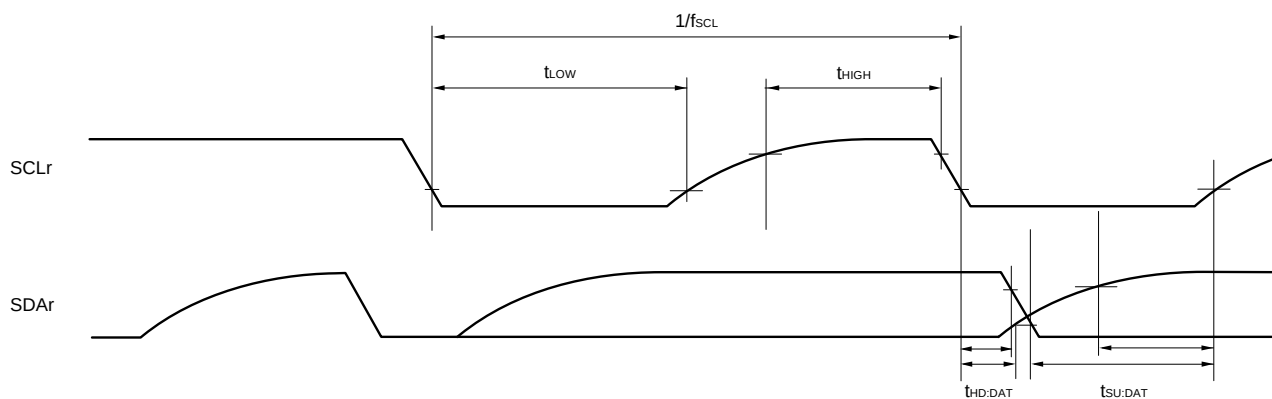
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 135$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		kHz
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 135$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		kHz
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		kHz
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		kHz
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		$1/f_{\text{MCK}} + 190$ ^{Note 3}		kHz
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	305	0	305	0	305	ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	0	355	0	355	0	355	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	355	0	355	0	355	ns
		$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2} , $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**2.** Use it with $\text{EV}_{\text{DD}0} \geq \text{V}_b$.**3.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t _{SU:STA}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs
Hold time ^{Note 1}	t _{HD:STA}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs
Data setup time (reception)	t _{SU:DAT}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	3.45	0	3.45	μs
Setup time of stop condition	t _{SU:STO}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs
Bus-free time	t _{BUF}		2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs

(Notes, Caution and Remark are listed on the next page.)

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1} , I_{OL1} , V_{OH1} , V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b = 400 \text{ pF}$, $R_b = 2.7 \text{ k}\Omega$

(2) I²C fast mode(T_A = -40 to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		100		100		100		μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

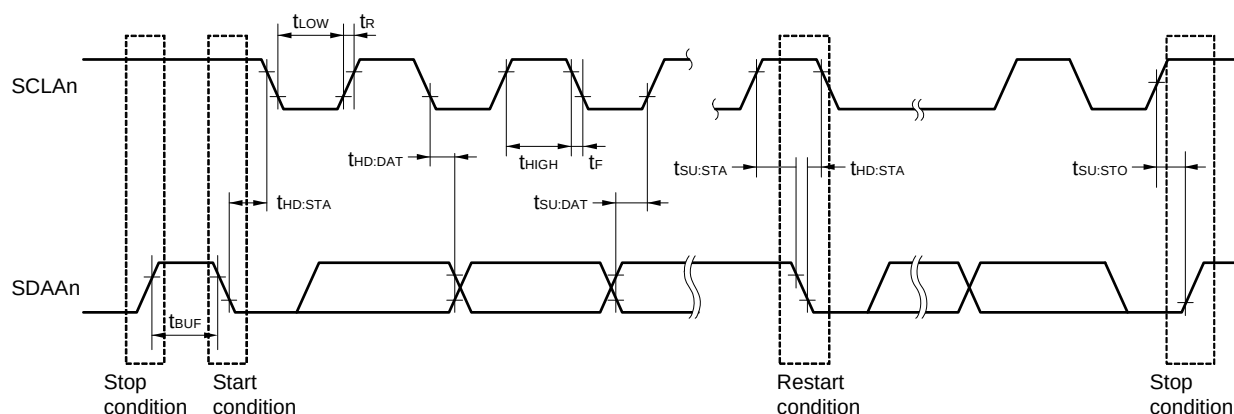
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: $f_{\text{CLK}} \geq 10\text{ MHz}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	0	1000	—	—	—	—	kHz
Setup time of restart condition	$t_{\text{SU:STA}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Hold time ^{Note 1}	$t_{\text{HD:STA}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0	0.45	—	—	—	—	μs
Setup time of stop condition	$t_{\text{SU:STO}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.26		—	—	—	—	μs
Bus-free time	t_{BUF}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		0.5		—	—	—	—	μs

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of $t_{\text{HD:DAT}}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{\text{OH}1}$, $I_{\text{OL}1}$, $V_{\text{OH}1}$, $V_{\text{OL}1}$) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: $C_b = 120\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

I²C serial transfer timing

Remark $n = 0, 1$

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (−) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (−) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (−) = AV_{REFM}
ANI0 to ANI14	Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI20	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (−) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (−) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}			± 0.50	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}			± 0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 2.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}			± 5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 1.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ ^{Note 4}			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14		0		AV_{REFP}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 5}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

- Notes**
1. Excludes quantization error ($\pm 1/2$ LSB).
 2. This value is indicated as a ratio (%FSR) to the full-scale value.
 3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 4. Values when the conversion time is set to $57\ \mu\text{s}$ (min.) and $95\ \mu\text{s}$ (max.).
 5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI16 to ANI20

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5	1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57	95	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 6.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $EV_{DD0} = AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		± 2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3		1.2	± 10.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Conversion time	t_{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3			± 0.85	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3			± 0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3			± 6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ Note 3			± 2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14	0			V_{DD}	V
		ANI16 to ANI20	0			EV_{DD0}	V
		Internal reference voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{BGR} Note 4				V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{TMPS25} Note 4				V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI20

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = $AV_{REFM} = 0\text{ V}$ ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

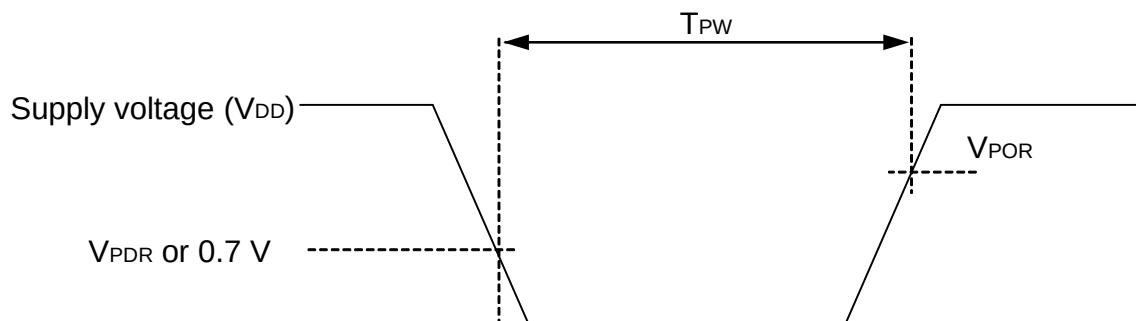
2.6.2 Temperature sensor/internal reference voltage characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.14		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature dependence of the temperature sensor		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	The power supply voltage is rising.	1.47	1.51	1.55	V
	V_{PDR}	The power supply voltage is falling.	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{LVD0}	The power supply voltage is rising.	3.98	4.06	4.14	V
		The power supply voltage is falling.	3.90	3.98	4.06	V
	V_{LVD1}	The power supply voltage is rising.	3.68	3.75	3.82	V
		The power supply voltage is falling.	3.60	3.67	3.74	V
	V_{LVD2}	The power supply voltage is rising.	3.07	3.13	3.19	V
		The power supply voltage is falling.	3.00	3.06	3.12	V
	V_{LVD3}	The power supply voltage is rising.	2.96	3.02	3.08	V
		The power supply voltage is falling.	2.90	2.96	3.02	V
	V_{LVD4}	The power supply voltage is rising.	2.86	2.92	2.97	V
		The power supply voltage is falling.	2.80	2.86	2.91	V
	V_{LVD5}	The power supply voltage is rising.	2.76	2.81	2.87	V
		The power supply voltage is falling.	2.70	2.75	2.81	V
	V_{LVD6}	The power supply voltage is rising.	2.66	2.71	2.76	V
		The power supply voltage is falling.	2.60	2.65	2.70	V
	V_{LVD7}	The power supply voltage is rising.	2.56	2.61	2.66	V
		The power supply voltage is falling.	2.50	2.55	2.60	V
	V_{LVD8}	The power supply voltage is rising.	2.45	2.50	2.55	V
		The power supply voltage is falling.	2.40	2.45	2.50	V
	V_{LVD9}	The power supply voltage is rising.	2.05	2.09	2.13	V
		The power supply voltage is falling.	2.00	2.04	2.08	V
	V_{LVD10}	The power supply voltage is rising.	1.94	1.98	2.02	V
		The power supply voltage is falling.	1.90	1.94	1.98	V
	V_{LVD11}	The power supply voltage is rising.	1.84	1.88	1.91	V
		The power supply voltage is falling.	1.80	1.84	1.87	V
	V_{LVD12}	The power supply voltage is rising.	1.74	1.77	1.81	V
		The power supply voltage is falling.	1.70	1.73	1.77	V
	V_{LVD13}	The power supply voltage is rising.	1.64	1.67	1.70	V
		The power supply voltage is falling.	1.60	1.63	1.66	V
Minimum pulse width	t_{LW}		300			μs
Detection delay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVDA0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V _{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V _{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V _{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVDB0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V _{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V _{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V _{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V _{LVDC0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V _{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V _{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V _{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

2.6.5 Power supply voltage rising slope characteristics**($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

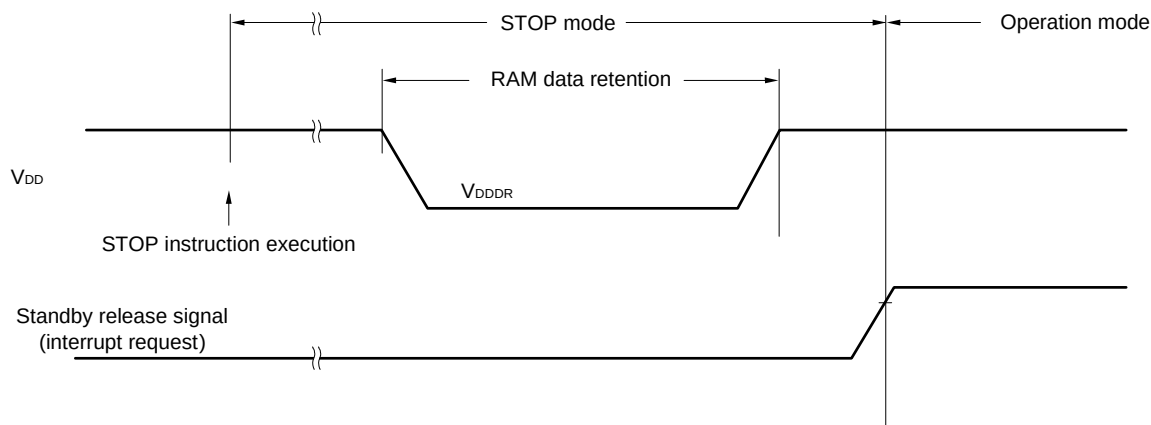
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{enwr}	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

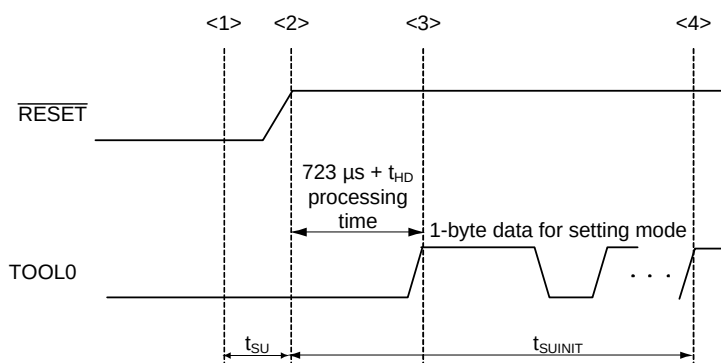
($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

<R> 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F140xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
 3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product in the RL78/G13A User's Manual.
 4. Please contact Renesas Electronics sales office for derating of operation under $T_A = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13A is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$).

There are following differences between the products "G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)" and the products "A: Consumer applications".

Parameter	Application	
	A: Consumer applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 32 MHz $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 16 MHz LS (low-speed main) mode: $1.8\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 8 MHz LV (low-voltage main) mode: $1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 4 MHz	HS (high-speed main) mode only: $2.7\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 32 MHz $2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ @1 MHz to 16 MHz
Serial array unit	UART CSI: $f_{\text{CLK}}/2$ (supporting 16 Mbps), $f_{\text{CLK}}/4$ Simplified I ² C communication	UART CSI: $f_{\text{CLK}}/4$ Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(Remark is listed on the next page.)

Remark The electrical characteristics of the products G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) are different from those of the products “A: Consumer applications”. For details, refer to **3.1** to **3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to $+6.5$	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to $+6.5$	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to $+0.3$	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to $+2.1$ and -0.3 to $V_{DD} + 0.3$ ^{Note 1}	V
Input voltage	V_{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to $+6.5$	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Output voltage	V_{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to $V_{DD} + 0.3$ ^{Note 2}	V
Analog input voltage	V_{AI1}	ANI16 to ANI20	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ ^{Notes 2, 3}	V
	V_{AI2}	ANI0 to ANI14	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3$ ^{Notes 2, 3}	V

- Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed $AV_{REF}(+) + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** $AV_{REF}(+)$: Positive reference voltage of the A/D converter.
- 3.** V_{SS} : Reference voltage

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Absolute Maximum Ratings (TA = 25 °C) (1/2)					
Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	−100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	TA	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	Tstg			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
XT1 clock oscillation frequency (f_x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G13A User's Manual.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}		1		32	MHz
High-speed on-chip oscillator clock frequency accuracy			-1.0		+1.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-3.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-10.0	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-60.0	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-0.1 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = $(I_{\text{OH}} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{\text{OH}} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I_{OL} ^{Note 1}	I _{OL1}	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		15.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$		35.0	mA
			$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$		20.0	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})			80.0	mA
	I _{OL2}	Per pin for P20 to P27, P150 to P156			0.4 ^{Note 2}	mA
		Total of all pins (When duty $\leq 70\%$ ^{Note 3})	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} , EV_{SS1} and V_{SS} pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor $\leq 70\%$.

The output current value that has changed to the duty factor $> 70\%$ the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to $n\%$).

- Total output current of pins = $(I_{OL} \times 0.7)/(n \times 0.01)$

<Example> Where $n = 80\%$ and $I_{OL} = 10.0\text{ mA}$

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	$0.8\text{EV}_{\text{DD0}}$	EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	2.2	EV_{DD0}	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	2.0	EV_{DD0}	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	1.5	EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156	0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63	$0.7\text{EV}_{\text{DD0}}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0	$0.2\text{EV}_{\text{DD0}}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20 to P27, P150 to P156	0		0.3V_{DD}	V
	V_{IL4}	P60 to P63	0		$0.3\text{EV}_{\text{DD0}}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 is EV_{DD0} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -3.0\text{ mA}$	$EV_{DD0} - 0.7$		V
			$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -2.0\text{ mA}$	$EV_{DD0} - 0.6$		V
			$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OH1} = -1.5\text{ mA}$	$EV_{DD0} - 0.5$		V
	V _{OH2}	P20 to P27, P150 to P156	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OH2} = -100\text{ }\mu\text{A}$	$V_{DD} - 0.5$		V
Output voltage, low	V _{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL1} = 0.6\text{ mA}$		0.4	V
	V _{OL2}	P20 to P27, P150 to P156	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $I_{OL2} = 400\text{ }\mu\text{A}$		0.4	V
	V _{OL3}	P60 to P63	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $I_{OL3} = 2.0\text{ mA}$		0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LIH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{DD0}			1	μA	
	I _{LIH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}			1	μA	
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	I _{LIL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0}			−1	μA	
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}			−1	μA	
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input		−1	μA	
				In resonator connection		−10	μA	
On-chip pll-up resistance	R _U	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} = E_{VDD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		1.5		mA
						$V_{DD} = 3.0\text{ V}$		1.5		mA
				Normal operation		$V_{DD} = 5.0\text{ V}$		3.4	6.8	mA
						$V_{DD} = 3.0\text{ V}$		3.4	6.8	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	5.3	mA
						$V_{DD} = 3.0\text{ V}$		2.7	5.3	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2	3.8	mA
						$V_{DD} = 3.0\text{ V}$		2	3.8	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		2.2	4.4	mA
						Resonator connection		2.3	4.5	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		2.2	4.4	mA
						Resonator connection		2.3	4.5	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.4	2.6	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.2	2.4	mA
						Resonator connection		1.4	2.6	mA
		Subsystem clock operation	Subsystem clock operation	$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4	5.5	μA
						Resonator connection		4	5.7	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.2	6.7	μA
						Resonator connection		4.3	6.9	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.5	9.3	μA
						Resonator connection		4.7	9.5	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.3	15.8	μA
						Resonator connection		5.6	16	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		6.6	25.8	μA
						Resonator connection		7.1	26	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		10.6	54.8	μA
						Resonator connection		11.4	55	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , EV_{DD1} or V_{SS} , EV_{SS0} , EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.41	1.71	mA	
					V _{DD} = 3.0 V		0.41	1.71	mA	
				f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.34	1.35	mA	
					V _{DD} = 3.0 V		0.34	1.35	mA	
				f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.33	1.04	mA	
					V _{DD} = 3.0 V		0.33	1.04	mA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.19	1.05	mA	
					Resonator connection		0.37	1.26	mA	
				f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.19	1.05	mA	
					Resonator connection		0.37	1.26	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.12	0.62	mA	
					Resonator connection		0.22	0.73	mA	
				f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.12	0.62	mA	
					Resonator connection		0.22	0.73	mA	
				Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5 T _A = −40°C	Square wave input		0.39	1	μA
						Resonator connection		0.48	1.3	μA
			f _{SUB} = 32.768 kHz Note 5 T _A = +25°C		Square wave input		0.55	2.2	μA	
					Resonator connection		0.64	2.5	μA	
			f _{SUB} = 32.768 kHz Note 5 T _A = +50°C		Square wave input		0.98	4.8	μA	
					Resonator connection		1.07	5.1	μA	
			f _{SUB} = 32.768 kHz Note 5 T _A = +70°C		Square wave input		1.73	11.3	μA	
					Resonator connection		1.82	11.6	μA	
			f _{SUB} = 32.768 kHz Note 5 T _A = +85°C		Square wave input		2.73	21.3	μA	
					Resonator connection		2.82	21.6	μA	
			f _{SUB} = 32.768 kHz Note 5 T _A = +105°C	Square wave input		5.33	50.3	μA		
				Resonator connection		5.42	50.6	μA		
	IDD3 Note 6	STOP mode Note 8	T _A = −40°C					0.26	0.7	μA
			T _A = +25°C					0.42	1.9	μA
			T _A = +50°C					0.85	4.5	μA
			T _A = +70°C					1.6	11	μA
			T _A = +85°C					2.6	21	μA
			T _A = +105°C					5.2	50	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , EV_{DD1} or V_{SS} , EV_{SS0} , EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

Peripheral Functions (Common to all products)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.2		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	$f_{\text{IL}} = 15\text{ kHz}$			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = V_{\text{DD}} = 5.0\text{ V}$		1.3	1.7	mA
			Low voltage mode, $\text{AV}_{\text{REFP}} = V_{\text{DD}} = 3.0\text{ V}$		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				100		μA
Temperature sensor operating current	I_{TMPS} Note 1				100		μA
LVD operating current	I_{LVD} Notes 1, 7				0.02		μA
Self programming operating current	I_{FSP} Notes 1, 9				2.5	12.2	mA
BGO operating current	I_{BGO} Notes 1, 8				2.5	12.2	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed ^{Note 10}		0.5	0.6	mA
			The A/D conversion operations are performed, low-voltage mode, $\text{AV}_{\text{REFP}} = V_{\text{DD}} = 3.0\text{ V}$		0.9	1.1	mA
		CSI/UART operation			0.5	0.62	mA

Notes 1. Current flowing to the V_{DD} .

- When high speed on-chip oscillator and high-speed system clock are stopped.
- Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. $I_{\text{DD}2}$ subsystem clock operation includes the operational current of the real-time clock.
- Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
- Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{WDT} when the watchdog timer operates.
- Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{\text{DD}1}$ or $I_{\text{DD}2}$ and I_{ADC} when the A/D converter is in operation.

- Notes**
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
 8. Current flowing only during data flash rewrite.
 9. Current flowing only during self programming.
 10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13A User's Manual.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

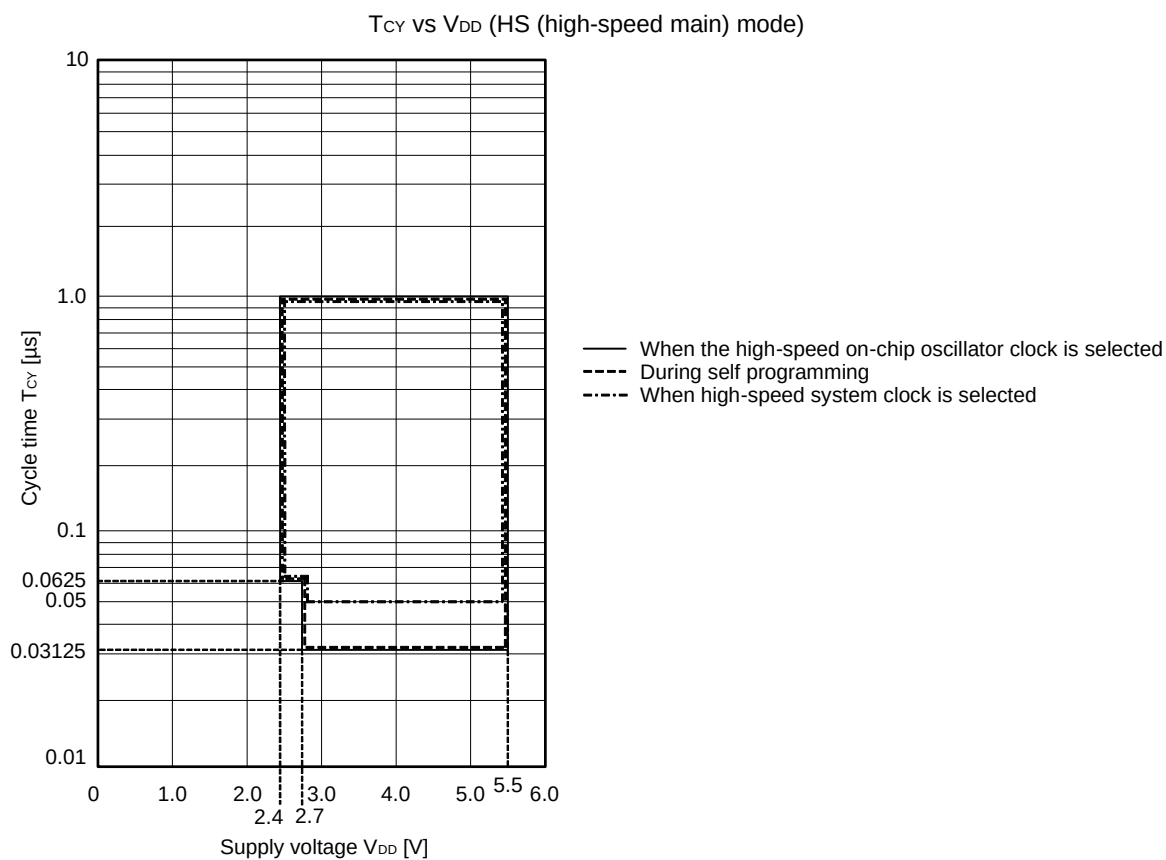
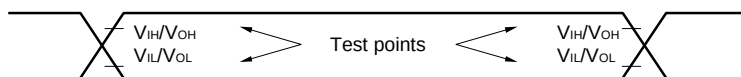
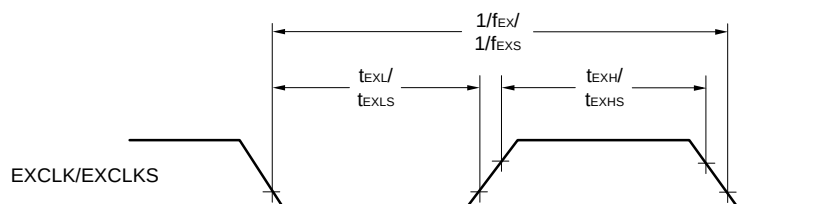
3.4 AC Characteristics

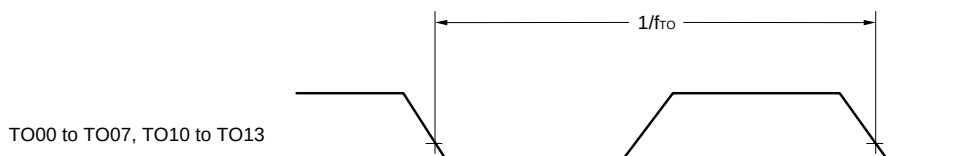
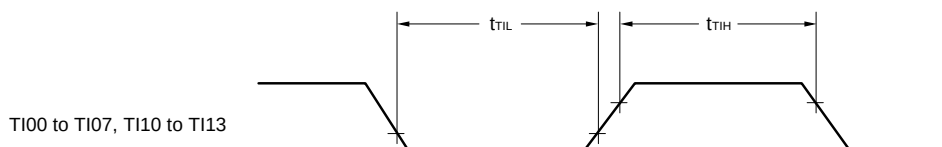
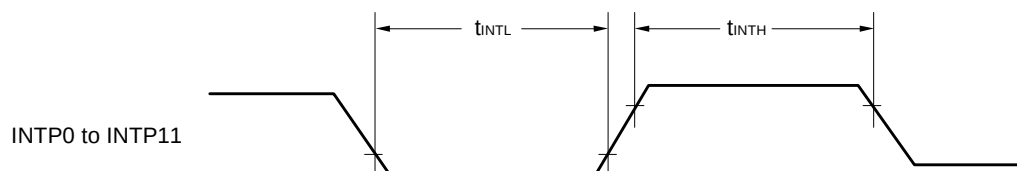
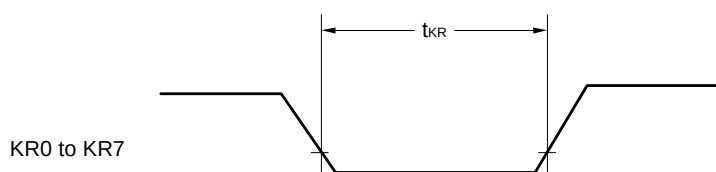
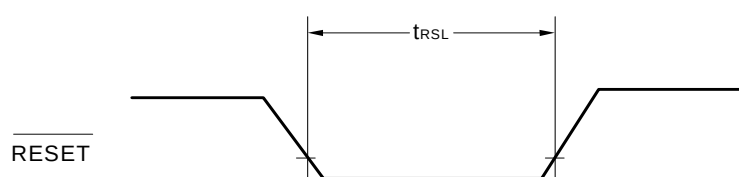
(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} = E_{VDD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{CY}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125		1 μs
				$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.0625	1	μs
		Subsystem clock (f _{SUB}) operation		$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	28.5	30.5	31.3 μs
		In the self programming mode	HS (high-speed main) mode	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0.03125	1	μs
				$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	0.0625	1	μs
External system clock frequency	f _{EX}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		1.0		16.0	MHz
	f _{EXS}			32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		24			ns
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$		30			ns
	t _{EXHS} , t _{EXLS}			13.7			μs
TI00 to TI07, TI10 to TI13 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}
TO00 to TO07, TO10 to TO13 output frequency	f _{TO}	HS (high-speed main) mode	$4.0\text{ V} \leq E_{VDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq E_{VDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	$4.0\text{ V} \leq E_{VDD0} \leq 5.5\text{ V}$			16	MHz
			$2.7\text{ V} \leq E_{VDD0} < 4.0\text{ V}$			8	MHz
			$2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$			4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1			μs
		INTP1 to INTP11	$2.4\text{ V} \leq E_{VDD0} \leq 5.5\text{ V}$	1			μs
Key interrupt input low-level width	t _{KR}	KR0 to KR7	$2.4\text{ V} \leq E_{VDD0} \leq 5.5\text{ V}$	250			ns
RESET low-level width	t _{RSL}			10			μs

Note The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$
 $2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MIN. 125 ns

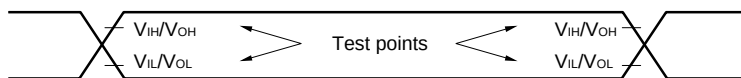
Remark f_{MCK}: Timer array unit operation clock frequency
 (Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
 m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} = E_{VDD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate ^{Note 1}		Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$		$f_{MCK}/12$ ^{Note 2}	bps
				2.6	Mbps

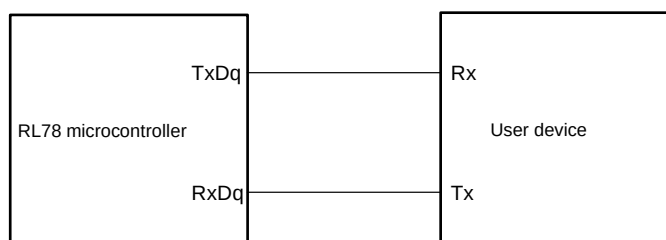
Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.

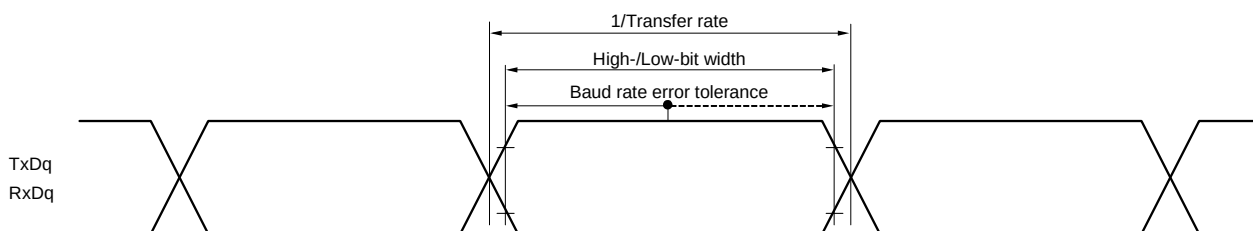
$2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	250		ns
			2.4 V ≤ EV _{DD0} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V		t _{KCY1} /2 – 24		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V		t _{KCY1} /2 – 36		ns
		2.4 V ≤ EV _{DD0} ≤ 5.5 V		t _{KCY1} /2 – 76		ns
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V		66		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V		66		ns
		2.4 V ≤ EV _{DD0} ≤ 5.5 V		113		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI1}			38		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO1}	C = 30 pF ^{Note 4}			50	ns

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

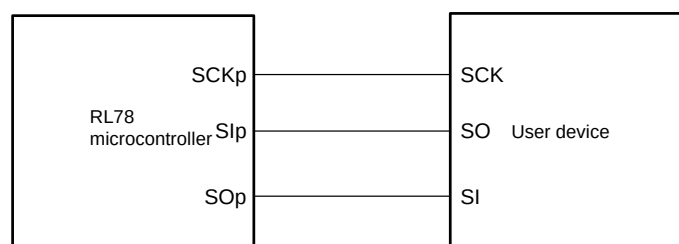
(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 5}	$t_{\text{KCY}2}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 20\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$16/f_{\text{MCK}}$		ns
				$12/f_{\text{MCK}}$ and 1000		ns
SCKp high-/low-level width	$t_{\text{KH}2}, t_{\text{KL}2}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY}2}/2 - 14$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY}2}/2 - 16$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$t_{\text{KCY}2}/2 - 36$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	$t_{\text{SIK}2}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 2}	$t_{\text{KSI}2}$	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 3}	$t_{\text{KSO}2}$	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$2/f_{\text{MCK}} + 66$	ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		$2/f_{\text{MCK}} + 113$	ns

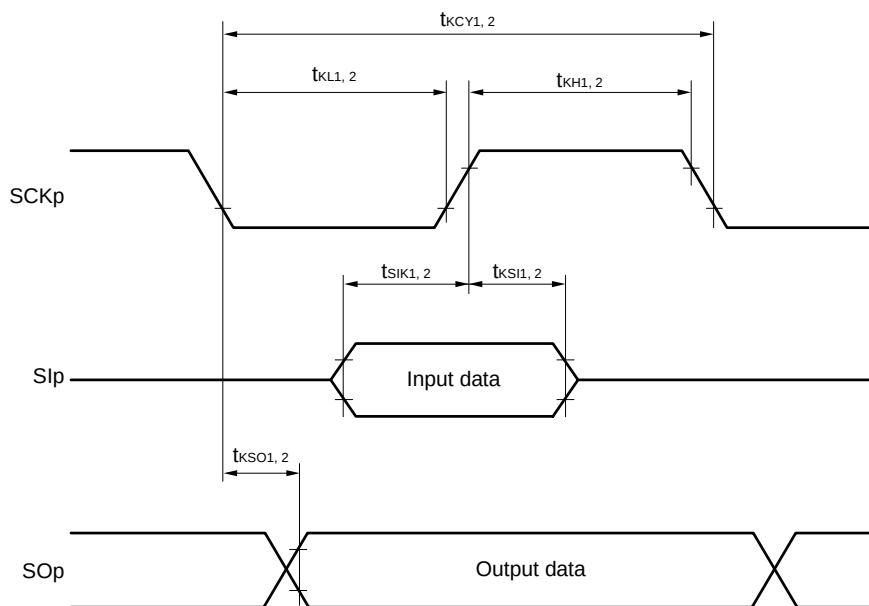
- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp $\downarrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp $\uparrow$ ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

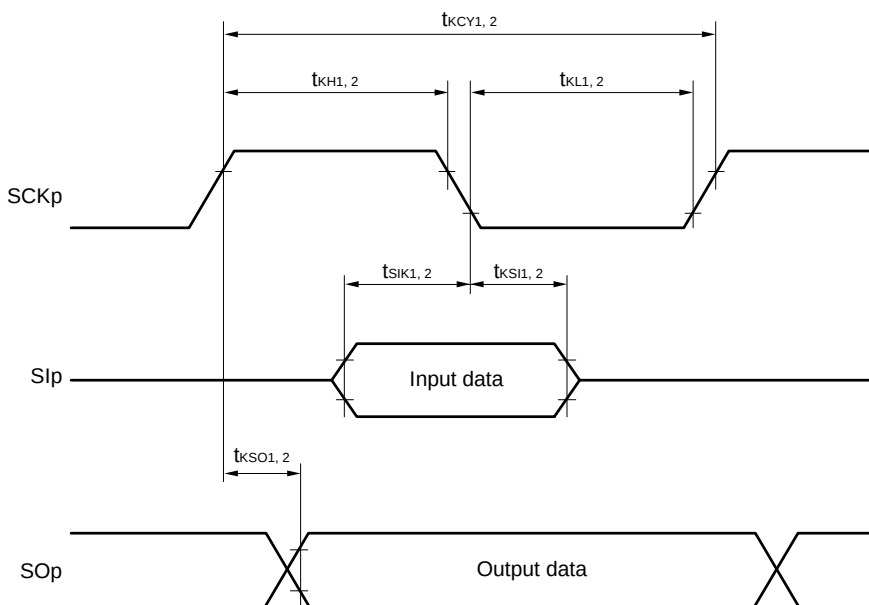
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

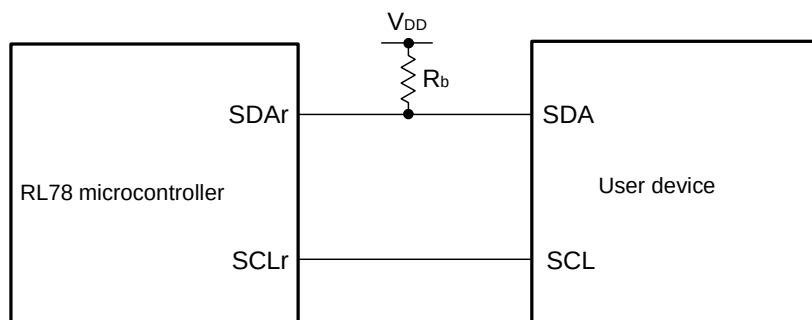
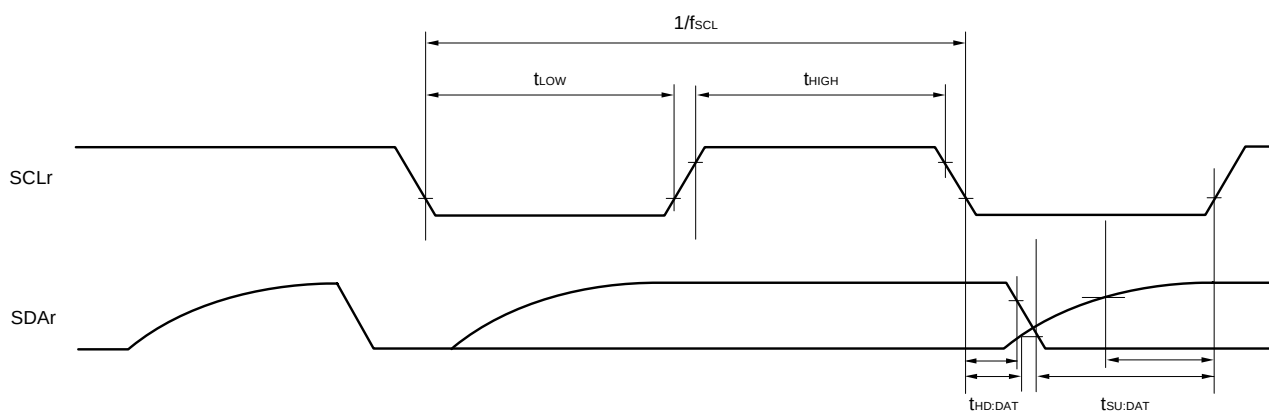
(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note1}	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ ^{Note2}		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note2}		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Reception			
		4.0 V $\leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, 2.7 V $\leq V_b \leq 4.0\text{ V}$		$f_{\text{MCK}}/12$ ^{Note 1}	bps
		Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$		2.6	Mbps
		2.7 V $\leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, 2.3 V $\leq V_b \leq 2.7\text{ V}$		$f_{\text{MCK}}/12$ ^{Note 1}	bps
		Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$		2.6	Mbps
		2.4 V $\leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, 1.6 V $\leq V_b \leq 2.0\text{ V}$		$f_{\text{MCK}}/12$ ^{Notes 1,2}	bps
		Theoretical value of the maximum transfer rate $f_{\text{CLK}} = 32\text{ MHz}$, $f_{\text{MCK}} = f_{\text{CLK}}$		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.**2.** The following conditions are required for low voltage interface when $\text{EV}_{\text{DD}0} < V_{\text{DD}}$.2.4 V $\leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 44 and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks 1. $V_b[\text{V}]$: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	Note 1	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$, $R_b = 1.4\text{ k}\Omega$, $\text{V}_b = 2.7\text{ V}$	2.6 ^{Note 2}	Mbps
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	Note 3	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$, $\text{V}_b = 2.3\text{ V}$	1.2 ^{Note 4}	Mbps
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	Note 5	bps
			Theoretical value of the maximum transfer rate $C_b = 50\text{ pF}$, $R_b = 5.5\text{ k}\Omega$, $\text{V}_b = 1.6\text{ V}$	0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ and $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ and $2.4\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Notes 5. The smaller maximum transfer rate derived by using $f_{\text{MCK}}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

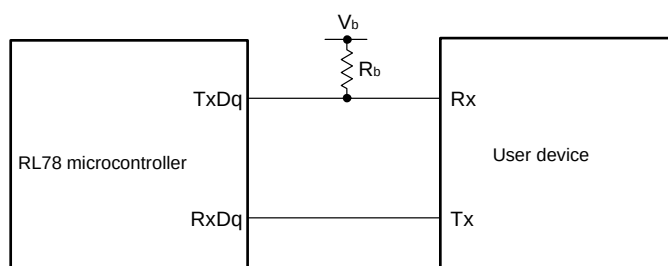
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

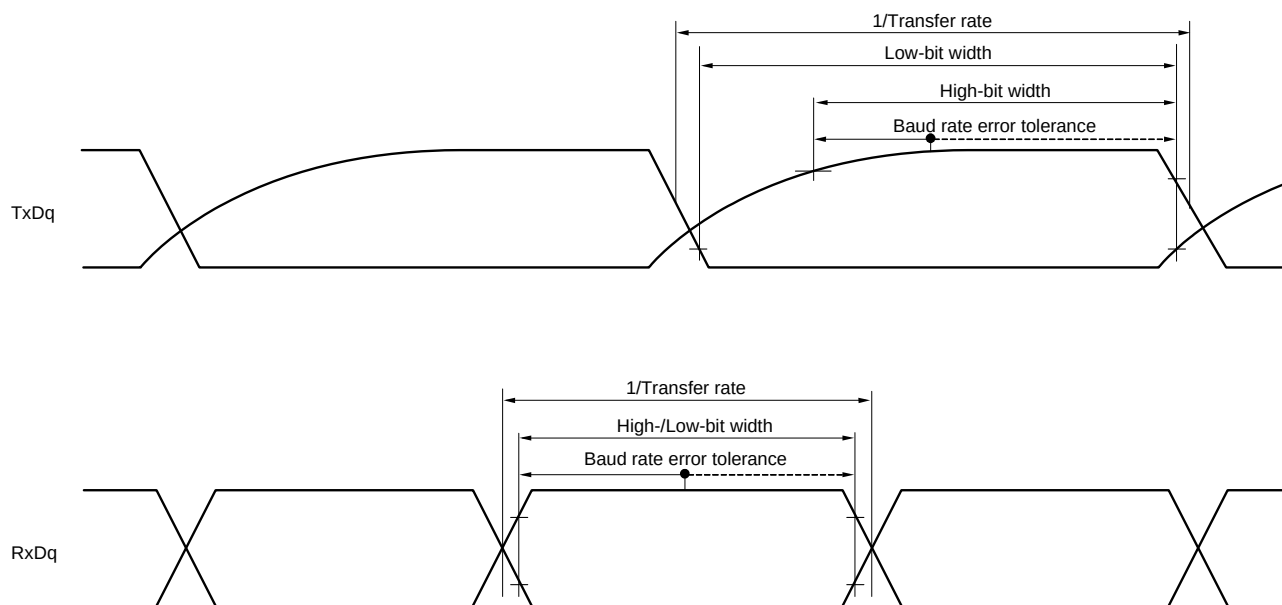
* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)

- Remarks 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	600		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1000		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	2300		ns
SCKp high-level width	t_{KH1}		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 150$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 340$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 916$		ns
SCKp low-level width	t_{KL1}		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 24$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 36$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 100$		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	$t_{\text{SIK}1}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	$t_{\text{KS}11}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	$t_{\text{KS}01}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		966	ns

Note When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

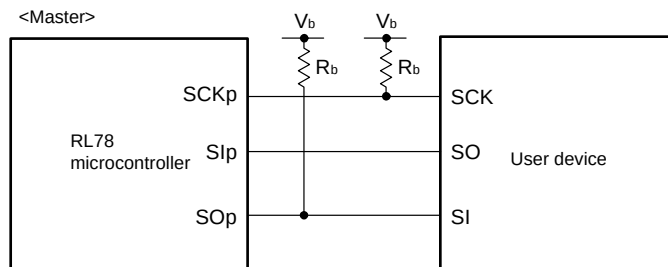
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) ^{Note}	t_{SH1}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	t_{KS01}	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		50	ns

Note When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

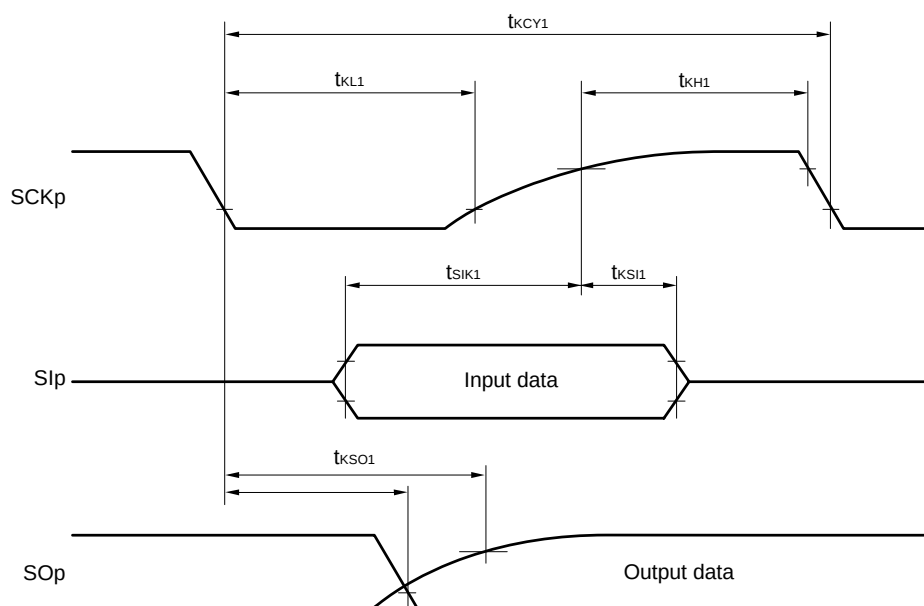
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

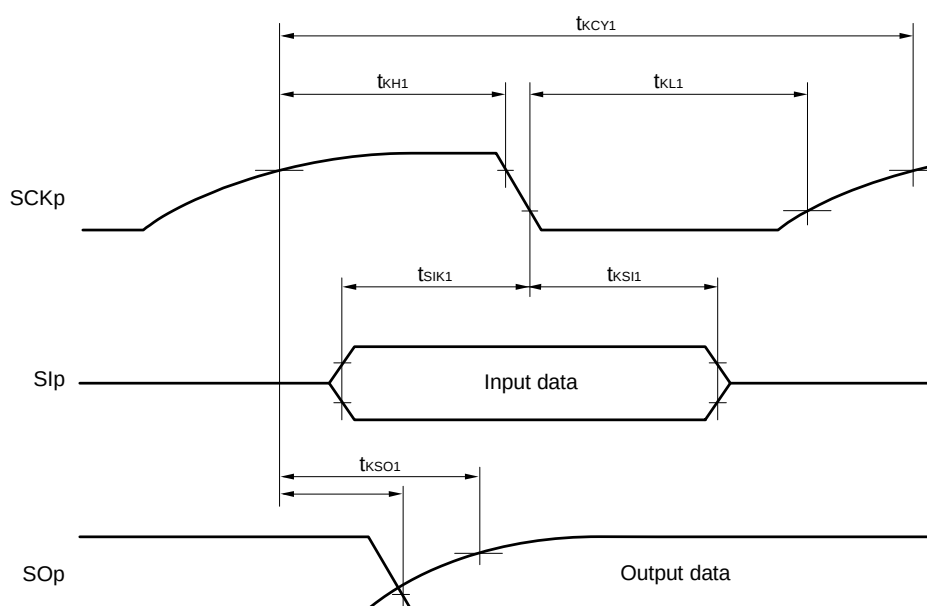
CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time ^{Note 1}	t_{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$28/f_{\text{MCK}}$	ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$24/f_{\text{MCK}}$	ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$20/f_{\text{MCK}}$	ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$	ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$40/f_{\text{MCK}}$	ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$32/f_{\text{MCK}}$	ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$28/f_{\text{MCK}}$	ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$24/f_{\text{MCK}}$	ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$	ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$96/f_{\text{MCK}}$	ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$72/f_{\text{MCK}}$	ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$64/f_{\text{MCK}}$	ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$52/f_{\text{MCK}}$	ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$32/f_{\text{MCK}}$	ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$20/f_{\text{MCK}}$	ns
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$t_{\text{KCY2}}/2 - 24$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$t_{\text{KCY2}}/2 - 36$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}	$t_{\text{KCY2}}/2 - 100$		ns
Slp setup time (to SCKp $\uparrow$) ^{Note 2}	t_{SIK2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$1/f_{\text{MCK}} + 40$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp $\uparrow$) ^{Note 3}	t_{KSI2}		$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 4}	t_{KSO2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		$2/f_{\text{MCK}} + 240$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		$2/f_{\text{MCK}} + 428$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		$2/f_{\text{MCK}} + 1146$	ns

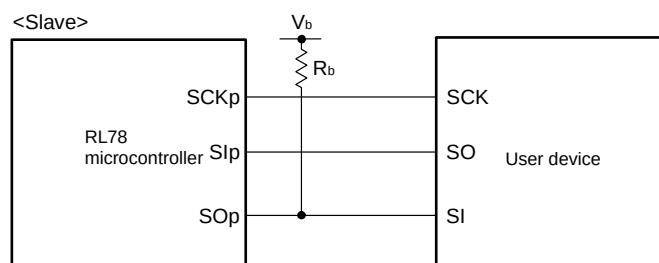
(Notes, Caution and Remarks are listed on the next page.)

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

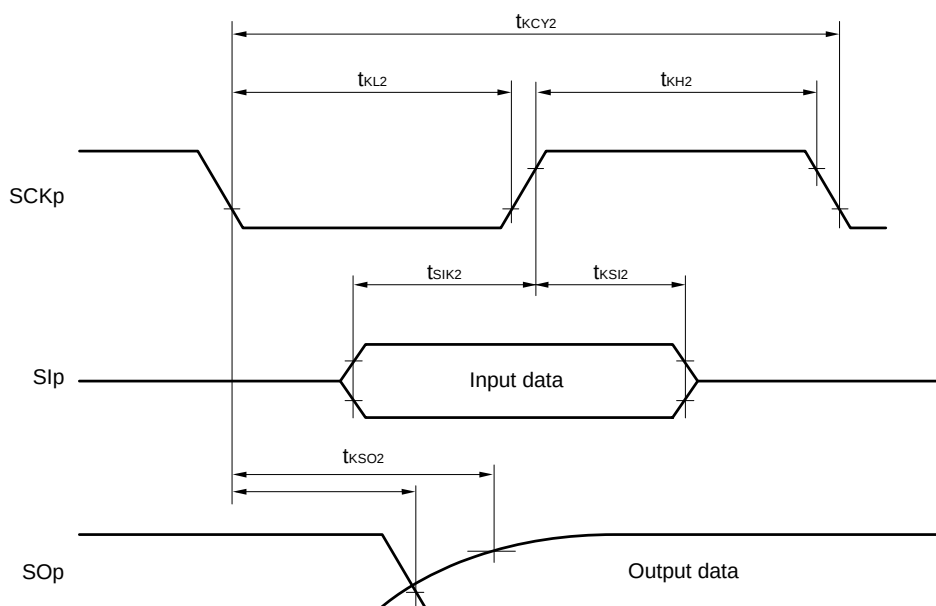
Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

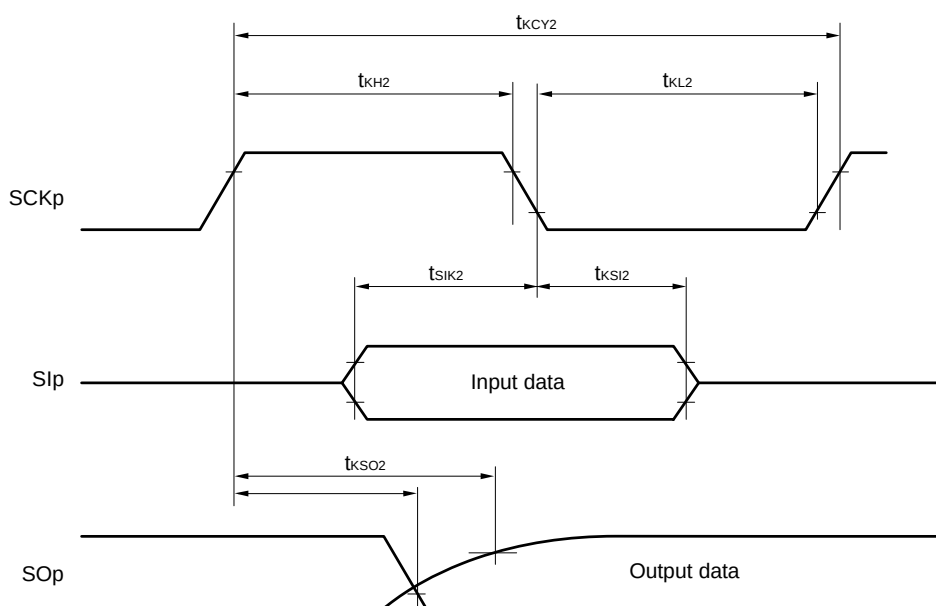


- Remarks** 1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 4. CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48- and 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		400 ^{Note 1}	kHz
		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		100 ^{Note 1}	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$		100 ^{Note 1}	kHz
Hold time when SCLr = "L"	t_{LOW}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	1200		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	1200		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	4600		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	4600		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	4650		ns
Hold time when SCLr = "H"	t_{HIGH}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	620		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	500		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	2700		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	2400		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	1830		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

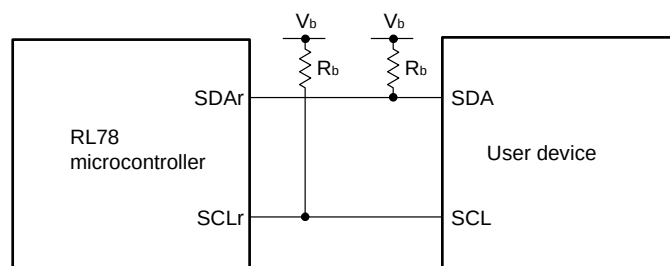
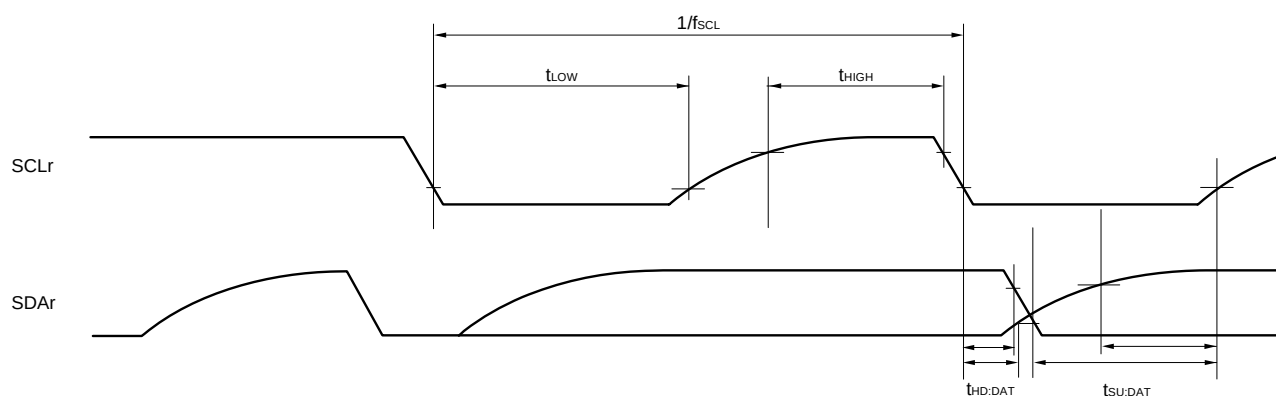
(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ Note 2		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ Note 2		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ Note 2		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ Note 2		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 570$ Note 2		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 50\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 100\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	0	1215	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 44- and 48-pin products)/ EV_{DD} tolerance (for the 64- and 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks

1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

3.5.2 Serial interface IICA

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

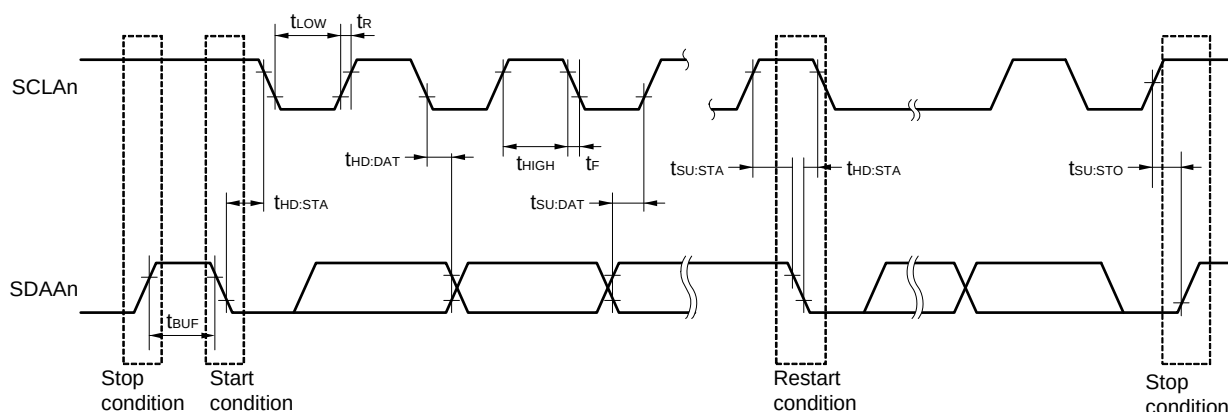
Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩFast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing

**Remark** n = 0, 1

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI20	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		–

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	± 3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14		0		AV_{REFP}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI16 to ANI20

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin : ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI20		0		EV_{DD0}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI20

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM} ^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

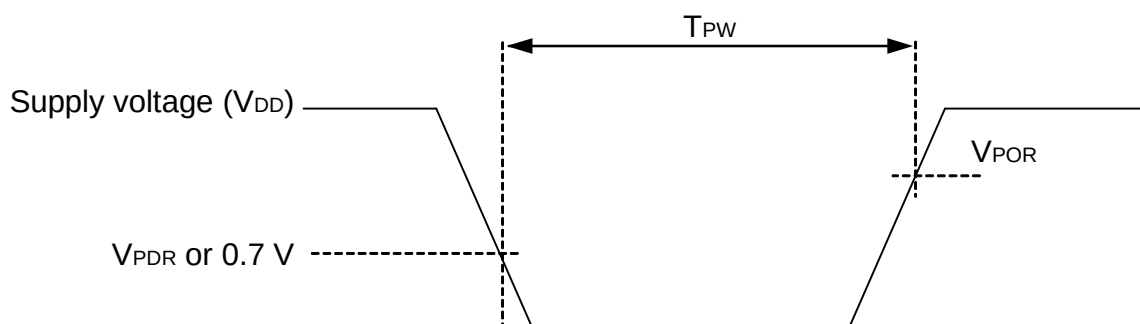
3.6.2 Temperature sensor/internal reference voltage characteristics**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TSPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.14		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMP}	Temperature dependence of the temperature sensor		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics**($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	The power supply voltage is rising.	1.45	1.51	1.57	V
	V_{PDR}	The power supply voltage is falling.	1.44	1.50	1.56	V
Minimum pulse width ^{Note}	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HISTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = -40 to $+105^\circ\text{C}$, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVD0}	The power supply voltage is rising.	3.90	4.06	4.22	V
		The power supply voltage is falling.	3.83	3.98	4.13	V
	V _{LVD1}	The power supply voltage is rising.	3.60	3.75	3.90	V
		The power supply voltage is falling.	3.53	3.67	3.81	V
	V _{LVD2}	The power supply voltage is rising.	3.01	3.13	3.25	V
		The power supply voltage is falling.	2.94	3.06	3.18	V
	V _{LVD3}	The power supply voltage is rising.	2.90	3.02	3.14	V
		The power supply voltage is falling.	2.85	2.96	3.07	V
	V _{LVD4}	The power supply voltage is rising.	2.81	2.92	3.03	V
		The power supply voltage is falling.	2.75	2.86	2.97	V
	V _{LVD5}	The power supply voltage is rising.	2.70	2.81	2.92	V
		The power supply voltage is falling.	2.64	2.75	2.86	V
	V _{LVD6}	The power supply voltage is rising.	2.61	2.71	2.81	V
		The power supply voltage is falling.	2.55	2.65	2.75	V
Minimum pulse width	t _{LW}		300			μs
					300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = -40 to $+105^\circ\text{C}$, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
Falling interrupt voltage			3.83	3.98	4.13	V	

3.6.5 Power supply voltage rising slope characteristics

(T_A = -40 to $+105^\circ\text{C}$, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S _{VDD}				54	V/ms

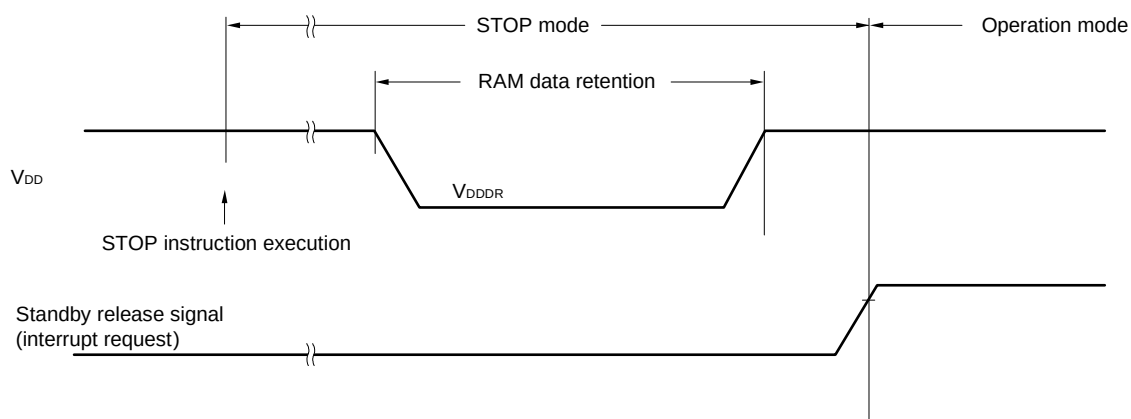
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{enwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ ^{Note 4}	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ ^{Note 4}	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ ^{Note 4}	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

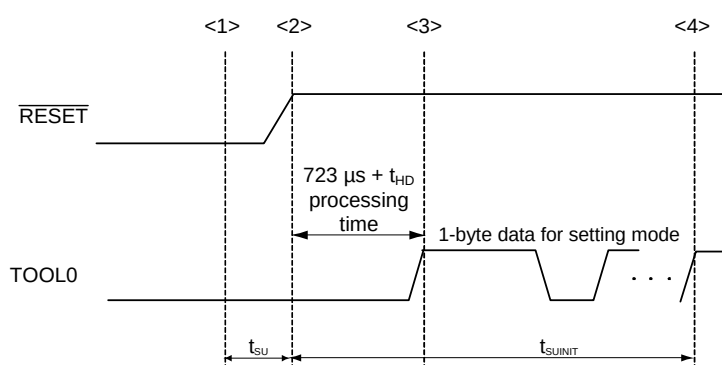
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq V_{\text{DD}} \leq 5.5\text{ V}$, $V_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUNIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUNIT} : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU} : Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD} : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

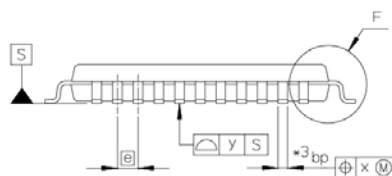
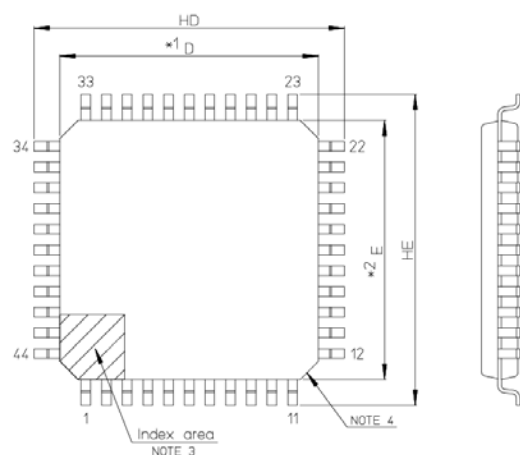
4. PACKAGE DRAWINGS

4.1 44-pin Products

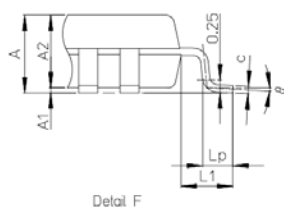
R5F140FKAFP, R5F140FLAFP

R5F140FKGFP, R5F140FLGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP44-10x10-0.80	PLQP0044GC-D	—	0.36g



- NOTE)
1. DIMENSIONS *1 AND *2 DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION *3 DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



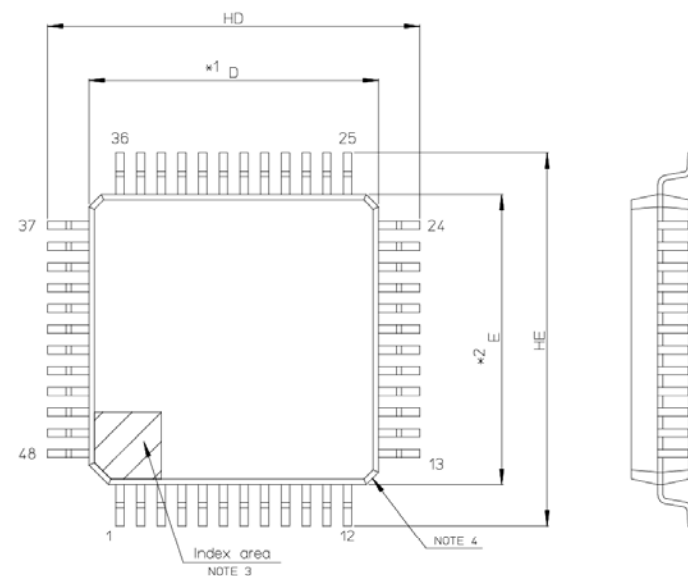
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.8	10.0	10.2
E	9.8	10.0	10.2
A2	—	1.4	—
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	—	—	1.6
A1	0.05	—	0.15
bp	0.22	0.37	0.45
c	0.09	—	0.20
#	0°	3.5°	8°
[e]	—	0.80	—
x	—	—	0.20
y	—	—	0.10
Lp	0.45	0.6	0.75
L1	—	1.0	—

4.2 48-pin Products

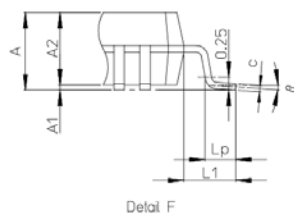
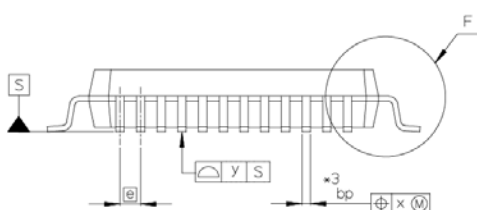
R5F140GKA FB, R5F140GLA FB

R5F140GKG FB, R5F140GLG FB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LF0FP48-7x7-0.50	PLQP0048KB-B	—	0.2g



- NOTE)
1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



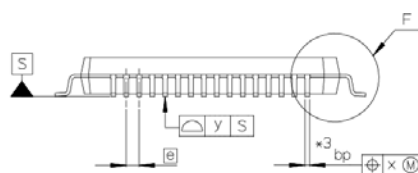
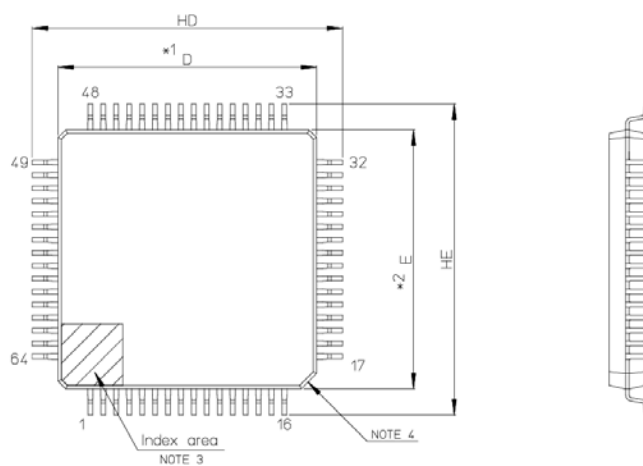
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	—	1.4	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

4.3 64-pin Products

R5F140LKAFB, R5F140LLAFB

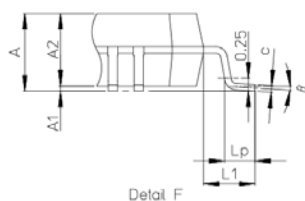
R5F140LKGFB, R5F140LLGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3g



NOTE)

1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



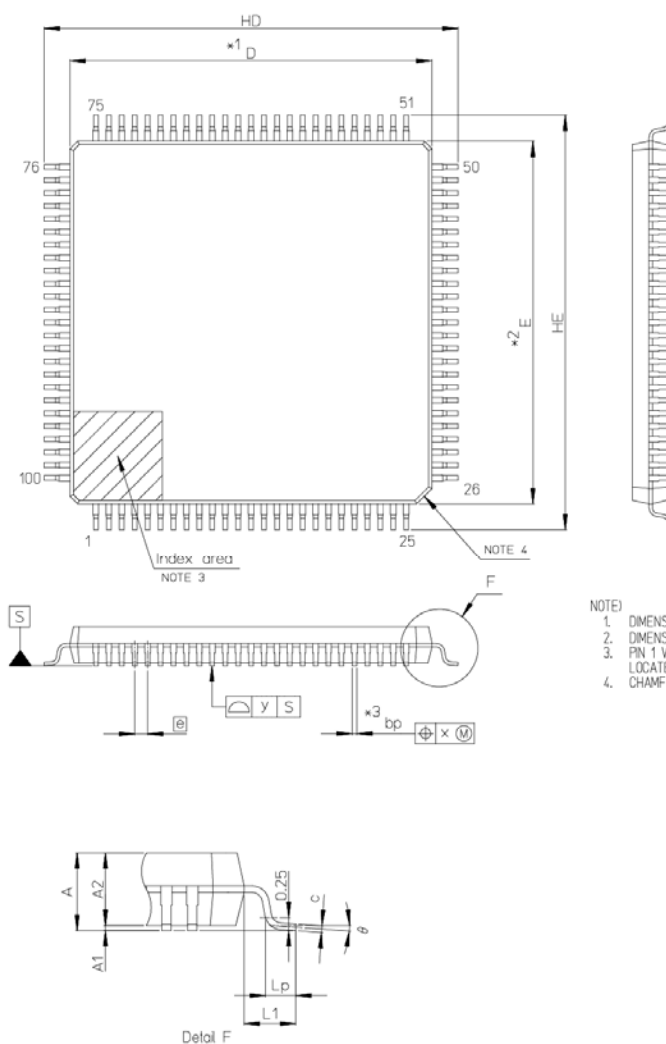
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	—	1.4	—
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

4.4 100-pin Products

R5F140PKAFB, R5F140PLAFB

R5F140PKGFB, R5F140PLGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQFP100KB-B	—	0.6g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A2	—	1.4	—
HD	15.8	16.0	16.2
HE	15.8	16.0	16.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

Revision History	RL78/G13A Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	Mar 06, 2020	-	First edition issued
1.10	Sep 18, 2020	18	Deletion of "(TARGET)" from the title of chapter 2 ELECTRICAL SPECIFICATIONS (T _A = -40 to +85°C)
		79	Deletion of "(TARGET)" from the title of chapter 3 ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T _A = -40 to +105°C)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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